ISI IDEAL SEMICONDUCTOR INC.

"Your Best Defense Against Obsolescence"

592 593

54AHCT 54AHCT
74AHCT 74AHCT

OBJECTIVE SPECIFICATIONS

8-Bit Binary Counter with Input Register and 8-Bit Binary Counter with Bidirectional Input Register/ Counter Outputs

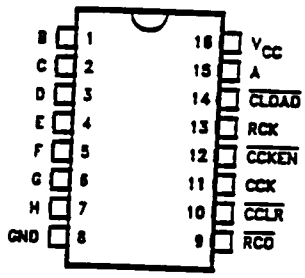
Features

- *Function, pin-out, speed and drive compatability with 54/74ALS logic family*
- *Low power consumption characteristic of CMOS*
- *High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V*
- *Inputs and outputs interface directly with TTL, NMOS and CMOS devices*
- *Wide operating voltage range: 4.5V to 5.5V*
- *Characterized for operation over industial and military temperature ranges:*

  74AHCT: -40°C to +85°C
  54AHCT: -55°C to +125°C

Pin Configurations

'592



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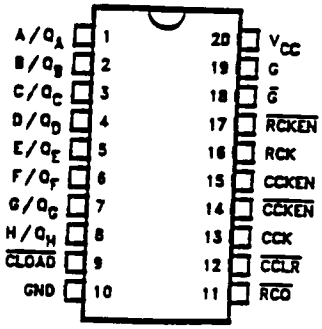
'593



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Description

The '592 and '593 contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO of the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second state. A clear input is also provided which will reset the counter to the all zeros stage.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input, G, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, CCKEN, which is active high and it also has an active low register clock enable, RCKEN.

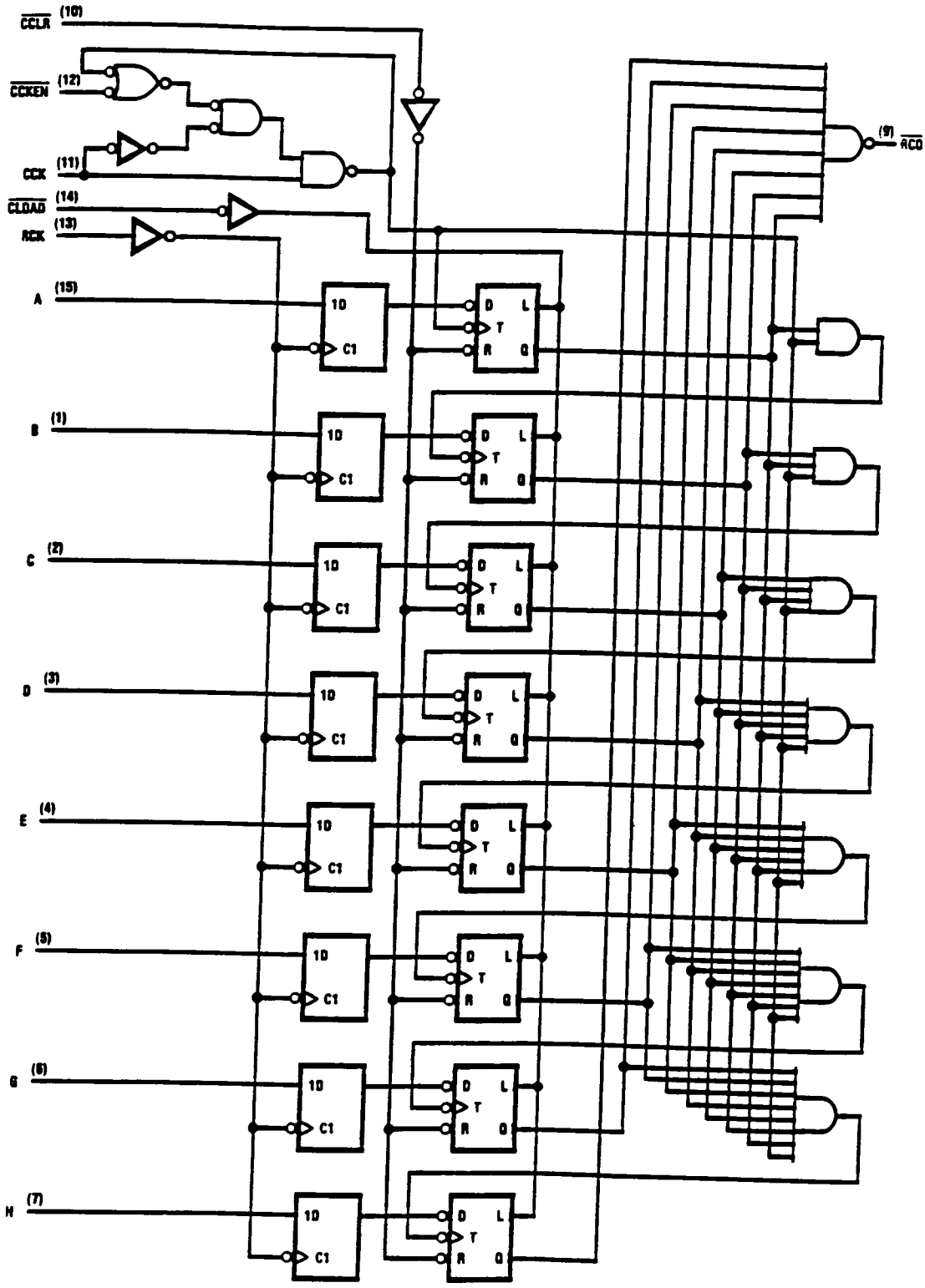
Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

46721 Fremont Blvd. • Fremont, California 94538 • Telephone: (510) 226-7000 • Fax: (510) 226-1564

Logic Diagrams

'592



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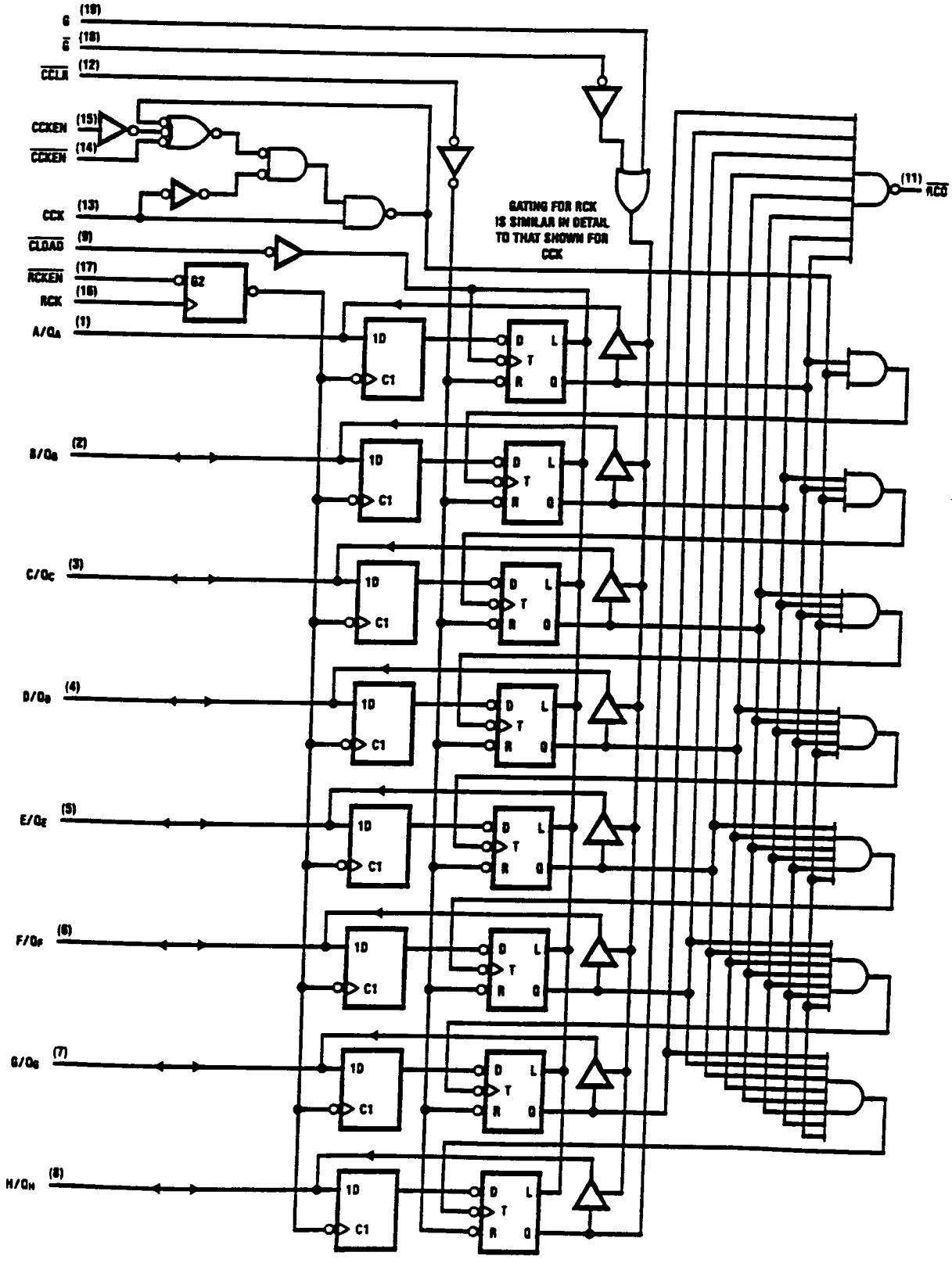
Logic Diagrams (Continued)

'593



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