HB56G236B/SB-6B/7B

2,097,152-word × 36-bit High Density Dynamic RAM Module

HITACHI

ADE-203-545A (Z)
Rev.1.0
Feb. 20, 1996

Description

The HB56G236 is a 2M × 36 dynamic RAM module, mounted 4 pieces of 16-Mbit DRAM (HM5118160BJ) sealed in SOJ package and 4 pieces of 2-Mbit DRAM (HM512200BS) sealed in SOJ package.

An outline of the HB56G236 is 72-pin single in-line package. Therefore, the HB56G236 makes high density mounting possible without surface mount technology.

The HB56G236 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the its module board.

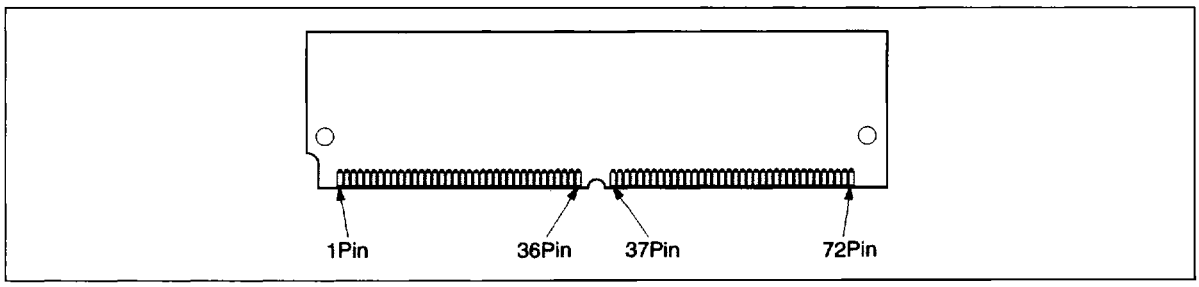
Features

- 72-pin single in-line package
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 60 ns/70 ns (max)
- Low power dissipation
  - — Active mode: 2.73 W/2.42 W (max)
  - — Standby mode (TTL): 84 mW (max)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56G236B-6B	60 ns	72-pin SIP socket type	Gold
HB56G236B-7B	70 ns		
HB56G236SB-6B	60 ns	72-pin SIP socket type	Solder
HB56G236SB-7B	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

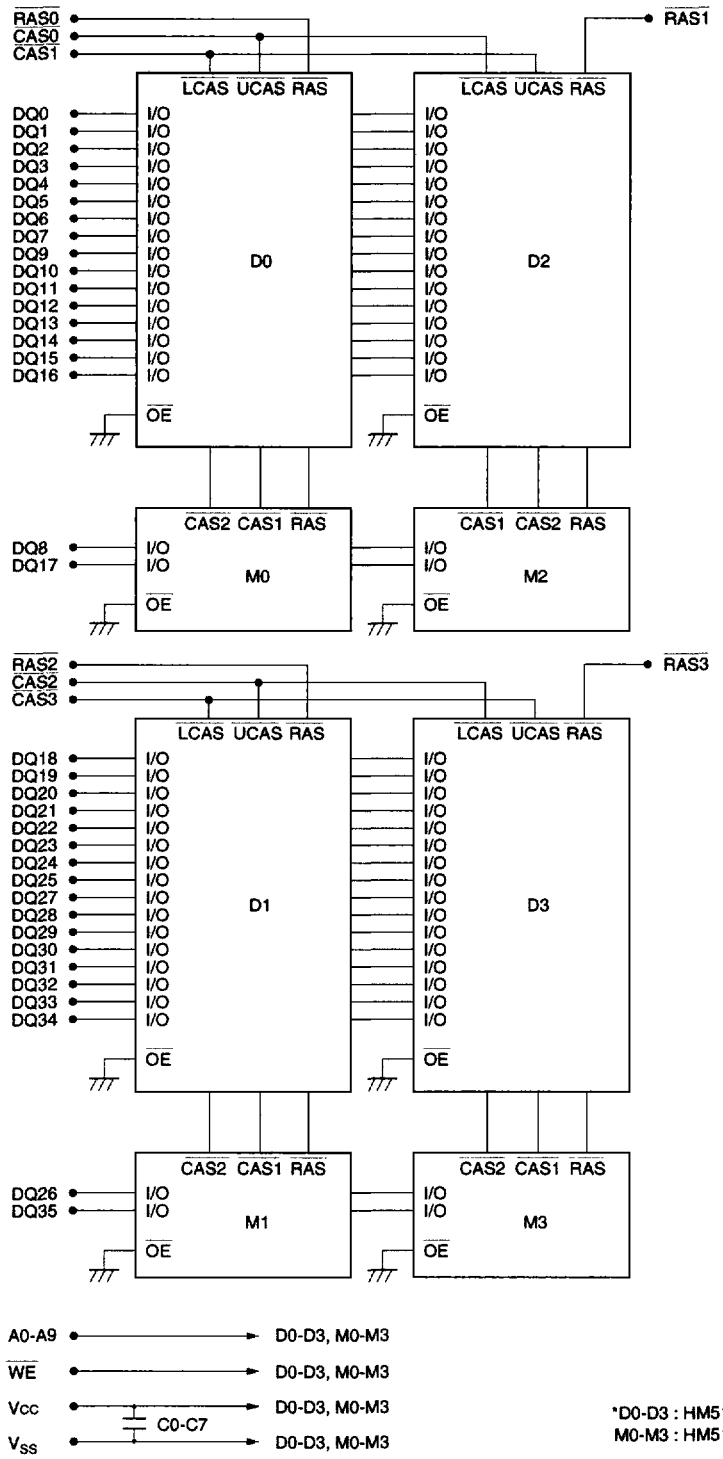
Pin Description

Pin Name	Function
A0 – A9	Address Input: A0 – A9 — Row Address: A0 – A9 — Column Address: A0 – A9 — Refresh Address: A0 – A9
DQ0 – DQ35	Data-in/Data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	Non Connection

Presence Detect Pin Arrangement

		Function	
Pin No.	Pin Name	60 ns	70 ns
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	V_{SS}
70	PD4	NC	NC

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	4	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

Parameter	Symbol	60 ns Min	60 ns Max	70 ns Min	70 ns Max	Unit	Test condition	Note
Operating current	I_{CC1}	—	520	—	460	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	520	—	460	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	520	—	460	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	520	—	460	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	34	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	48	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	34	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ±5%, V_{SS} = 0 V) *1, *2, *17

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	5
Refresh period (1,024 cycles)	t_{REF}	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	7, 8, 15
Access time from address	t_{AA}	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	10
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	—	35	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	20	ns	11
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	12
Write command hold time	t_{WCH}	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	13
Data-in hold time	t_{DH}	15	—	15	—	ns	13

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	

Fast Page Mode Cycle

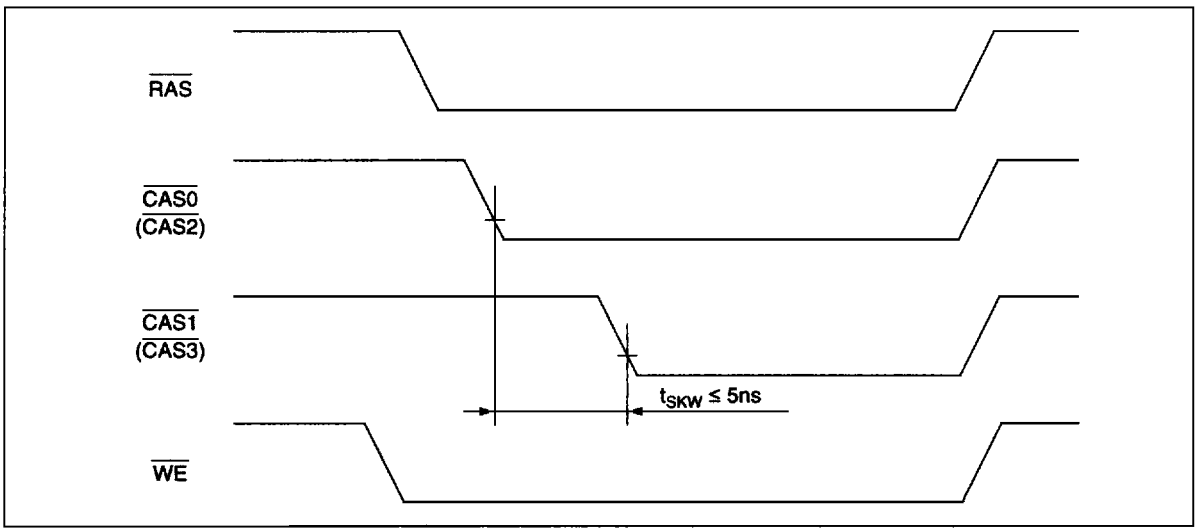
Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
12. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
15. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
16. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min/ V_{IL} max level.
17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.

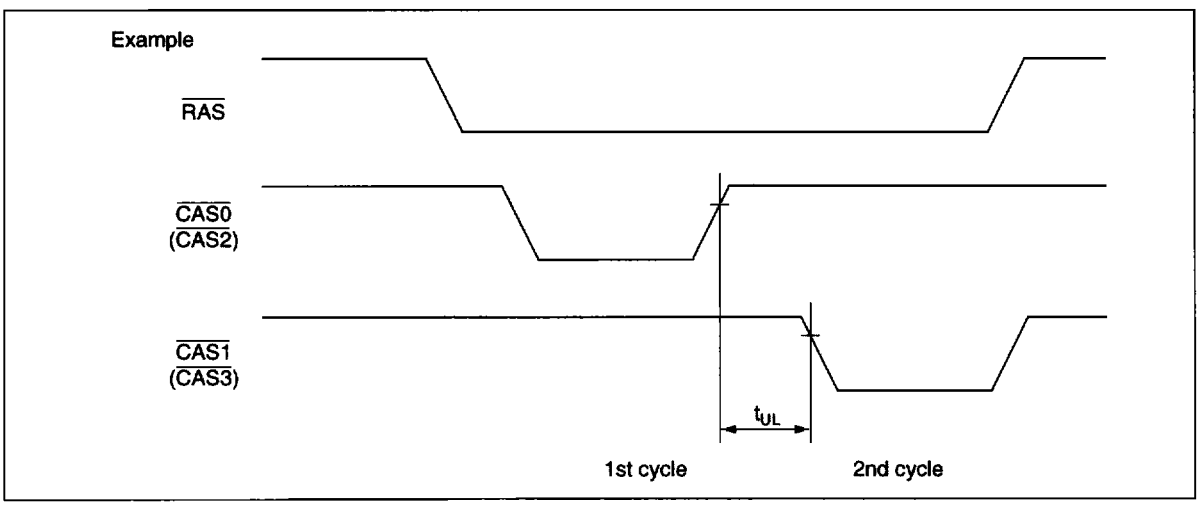
Notes concerning 2$\overline{CAS}$ control

(1) In one memory cycle, activate both of 2$\overline{CAS}$s ($\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$ and $\overline{CAS3}$)) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$ and $\overline{CAS3}$)) 5 ns or less.

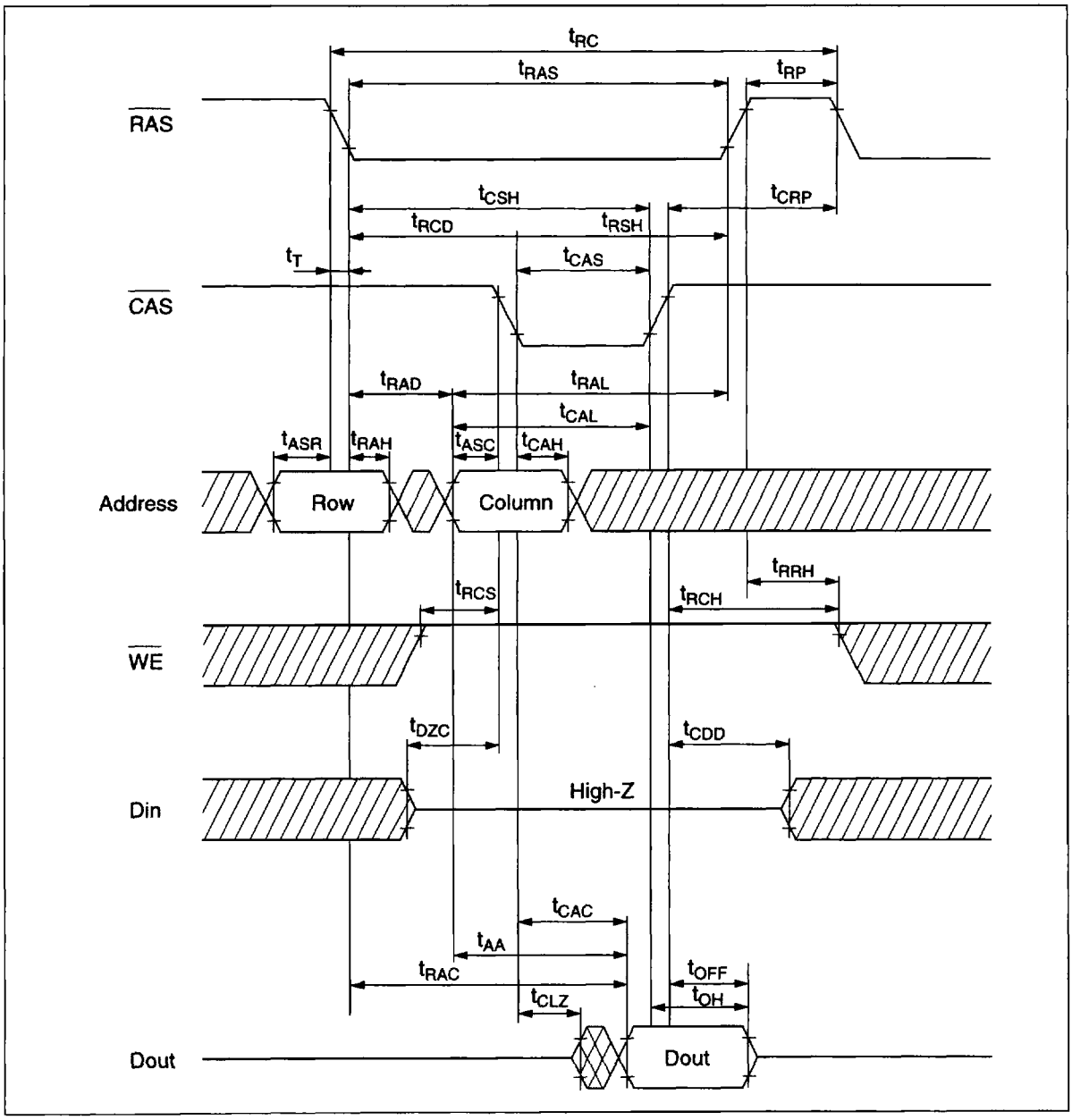


(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL} the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).



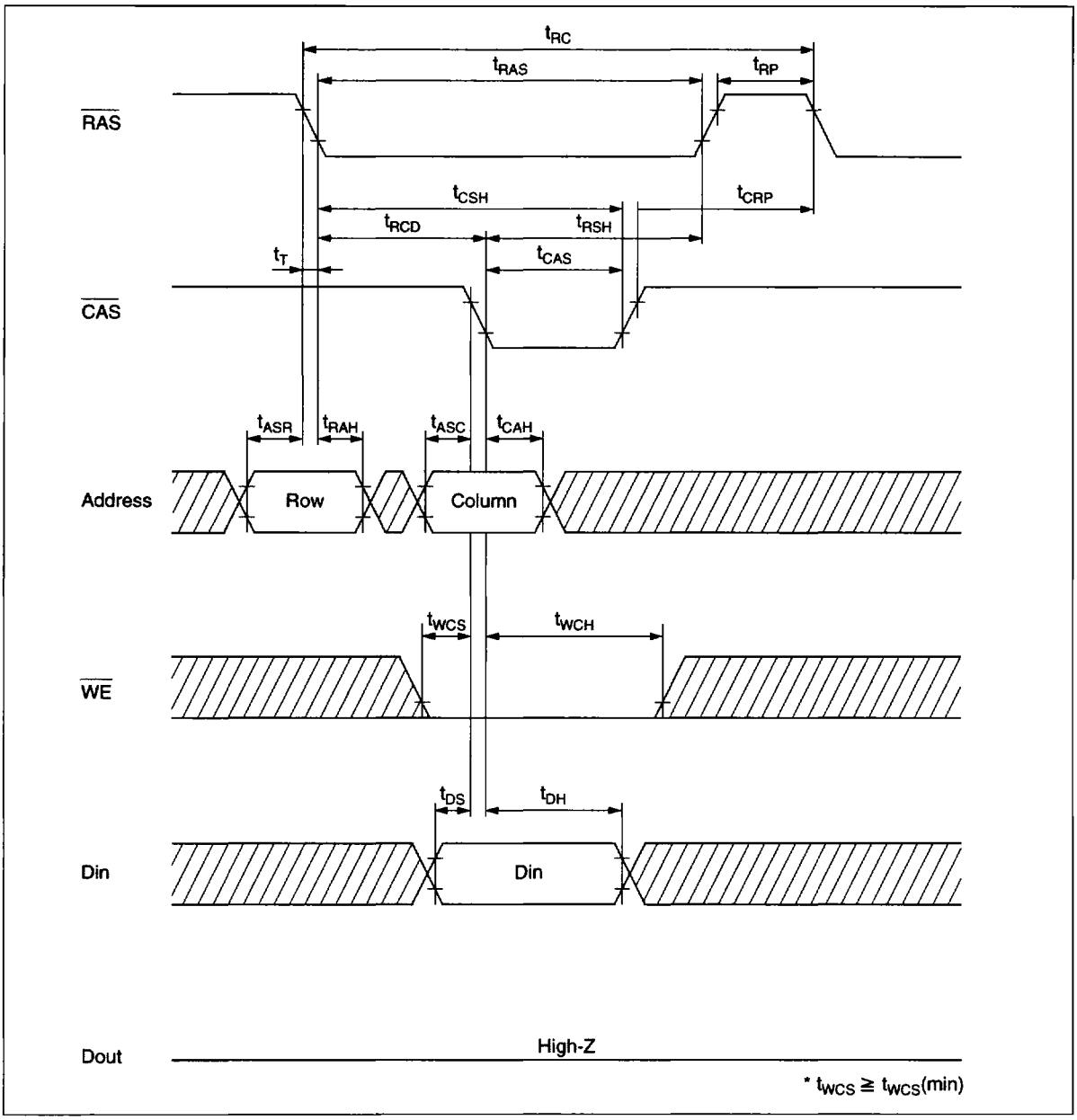
Timing Waveform

Read Cycle

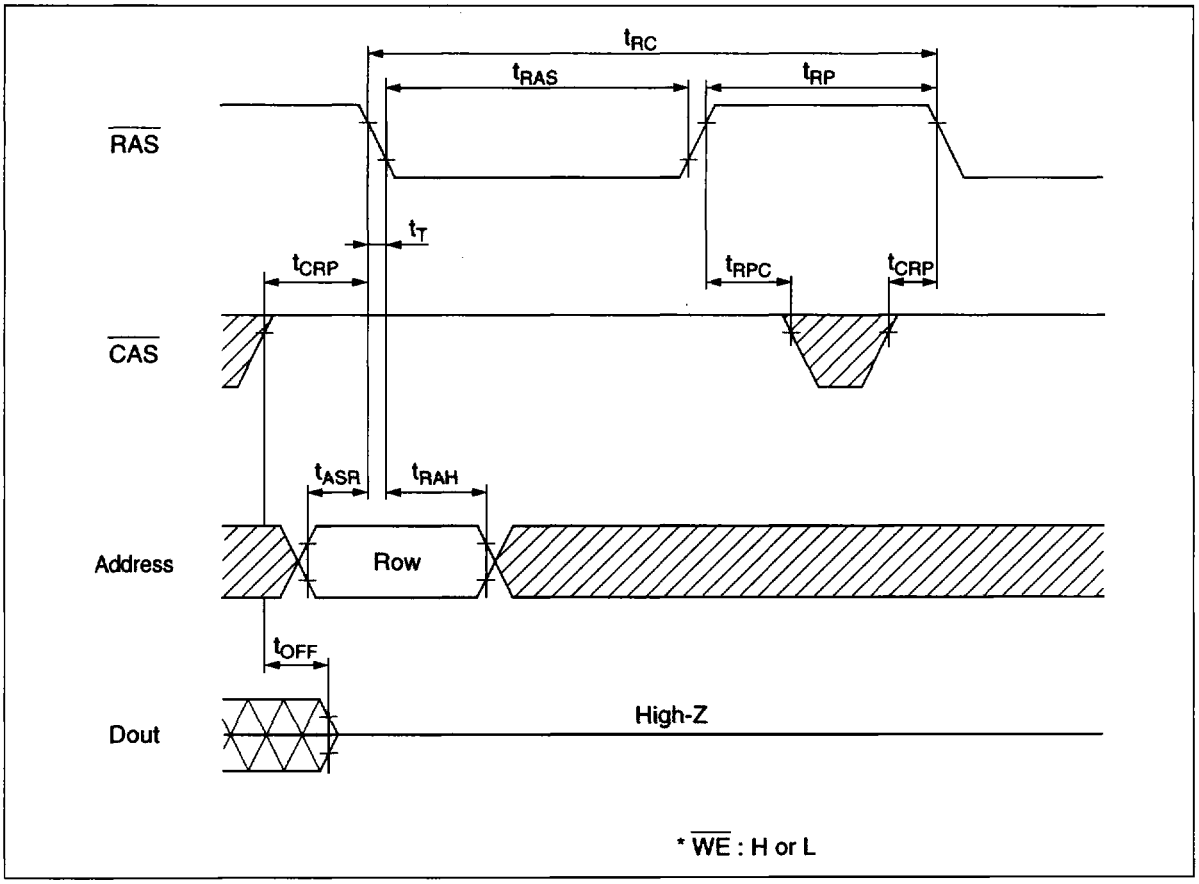


Note : ////////: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))
XXXXX: Invalid Dout

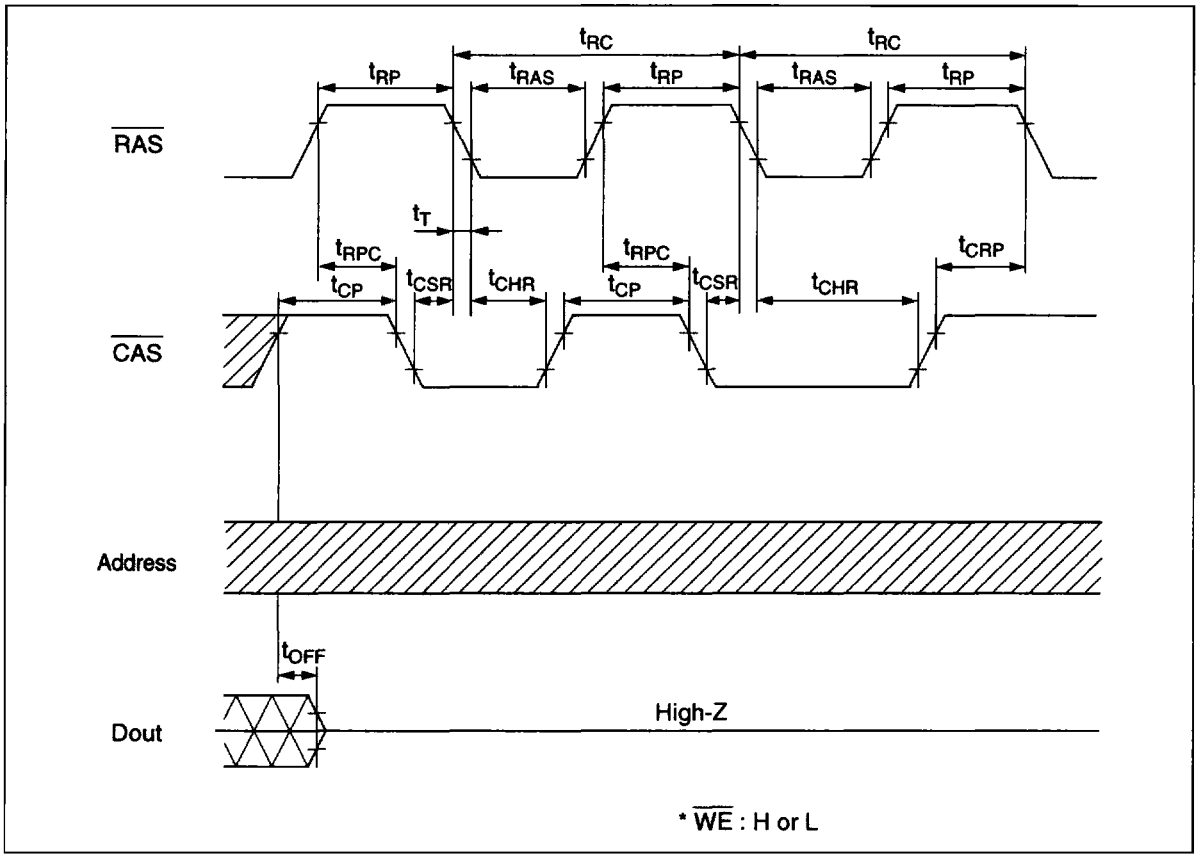
Early Write Cycle



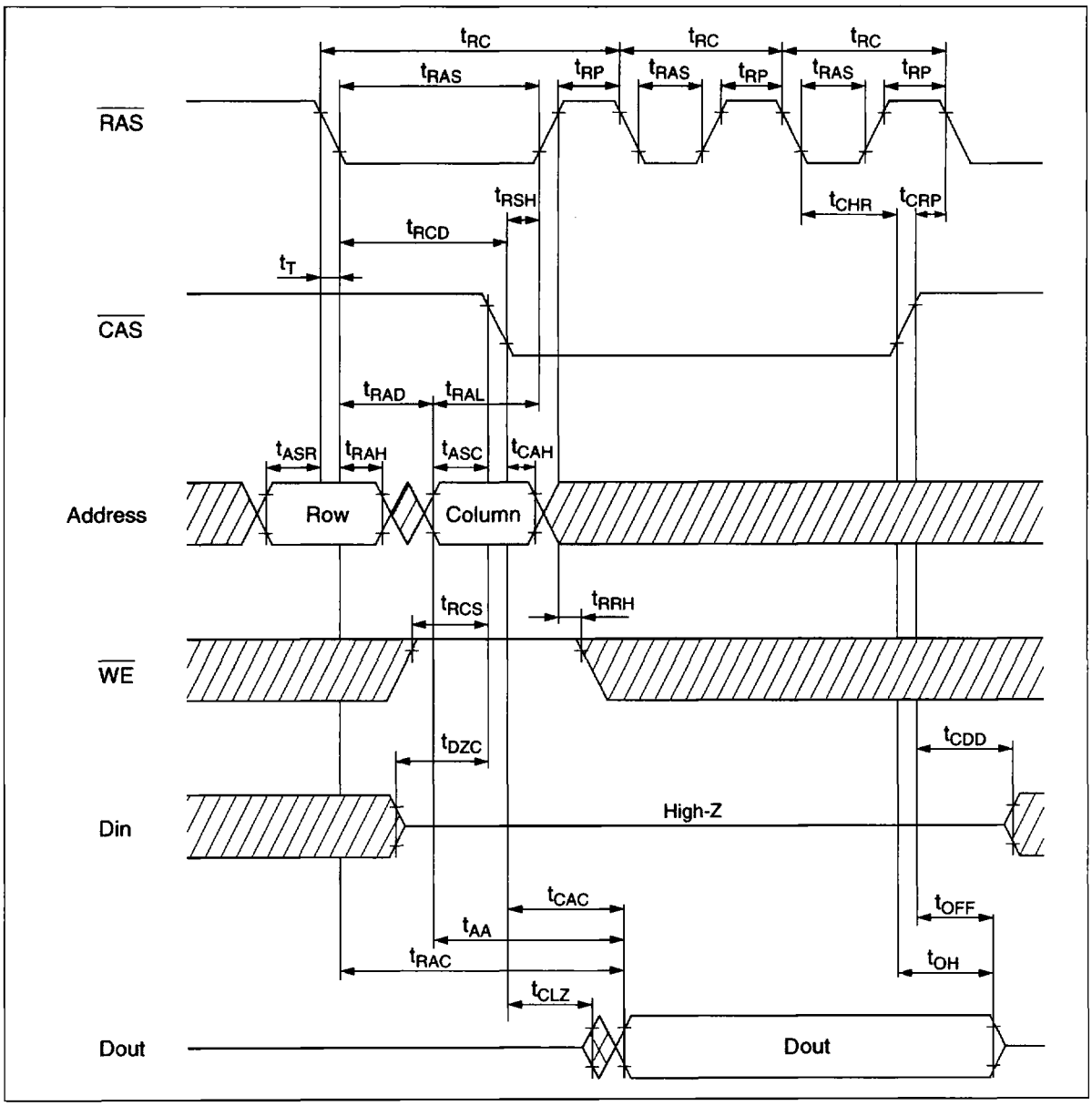
$\overline{RAS}$-Only Refresh Cycle



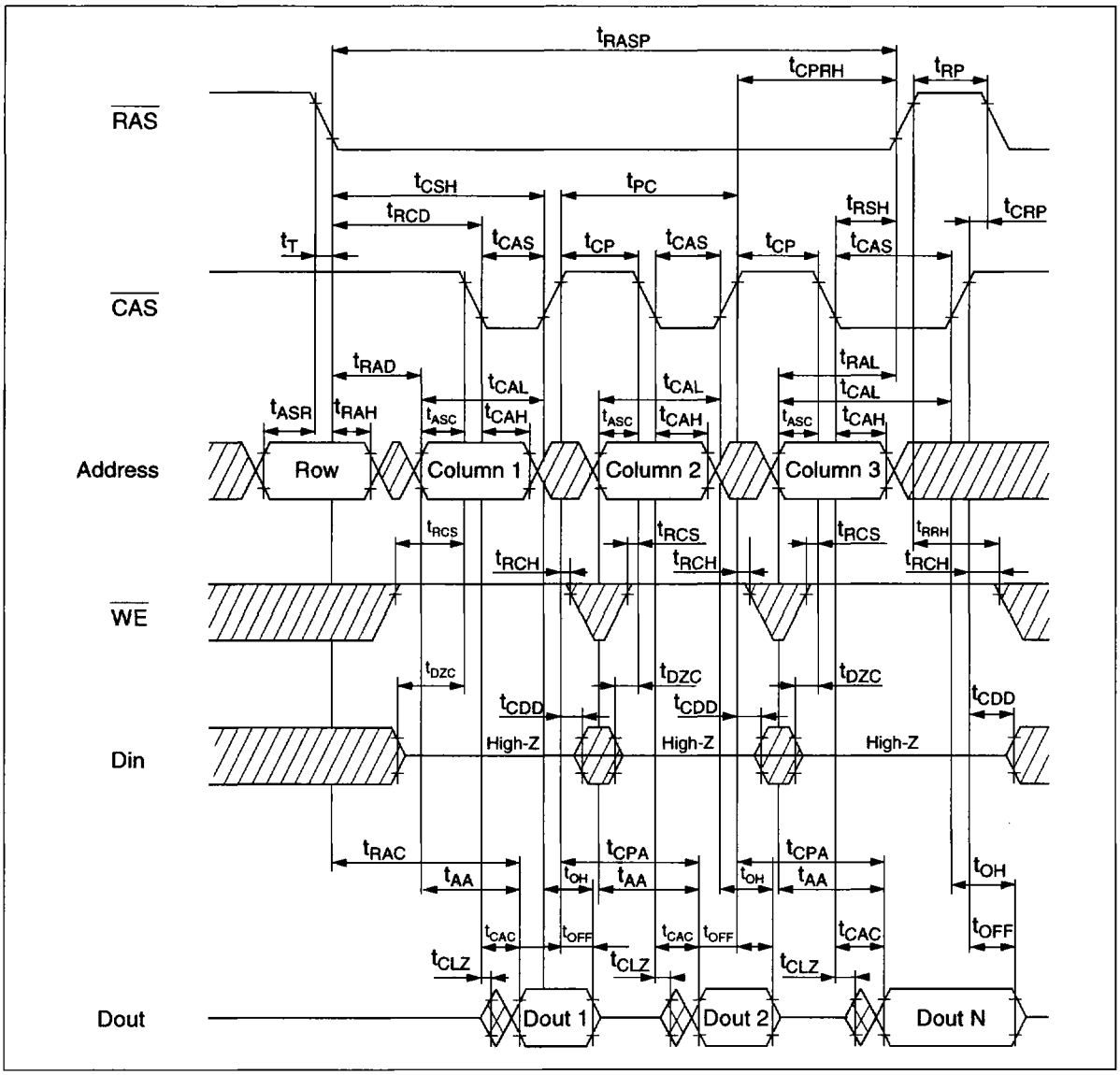
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



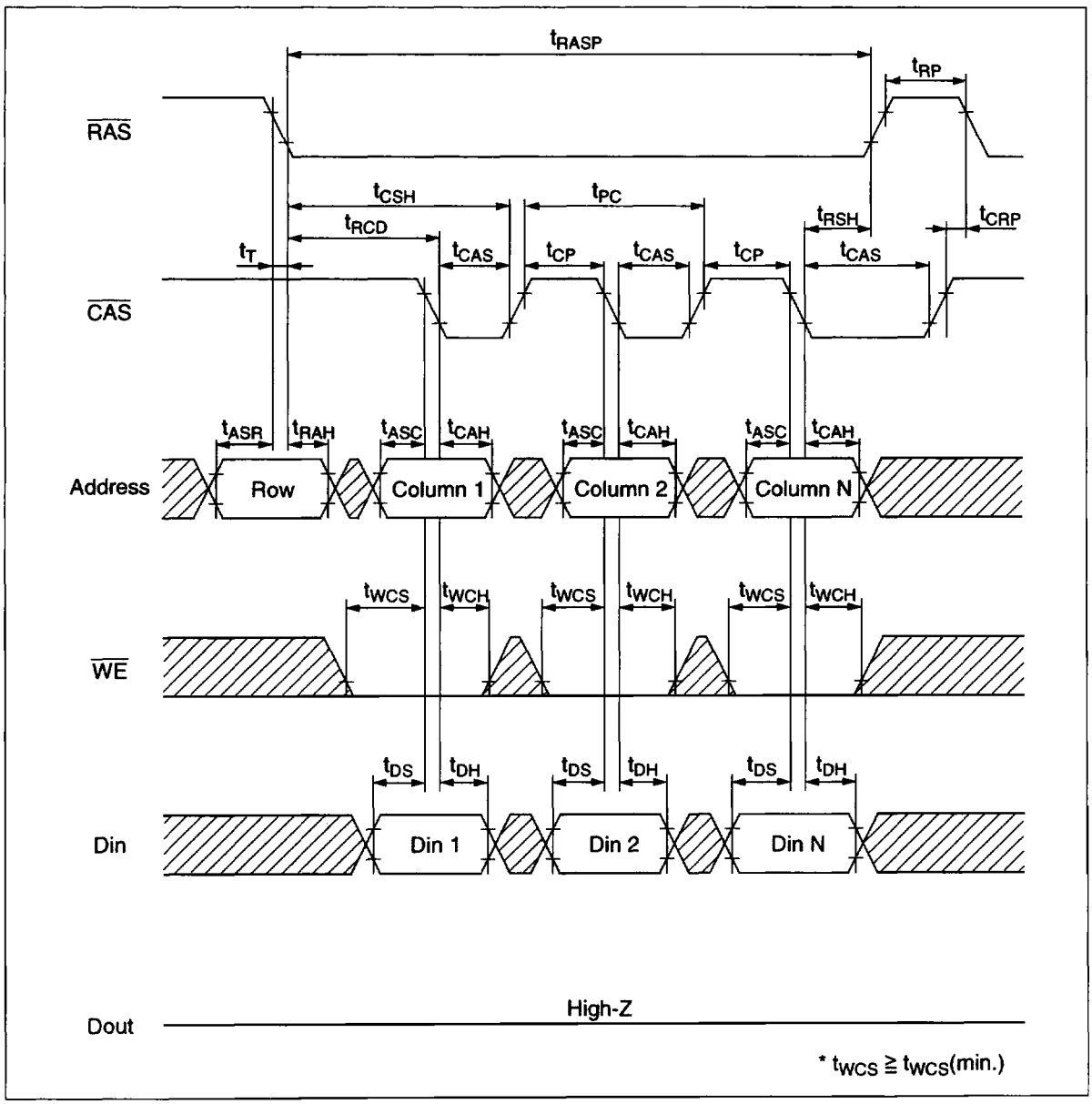
Hidden Refresh Cycle



Fast Page Mode Read Cycle

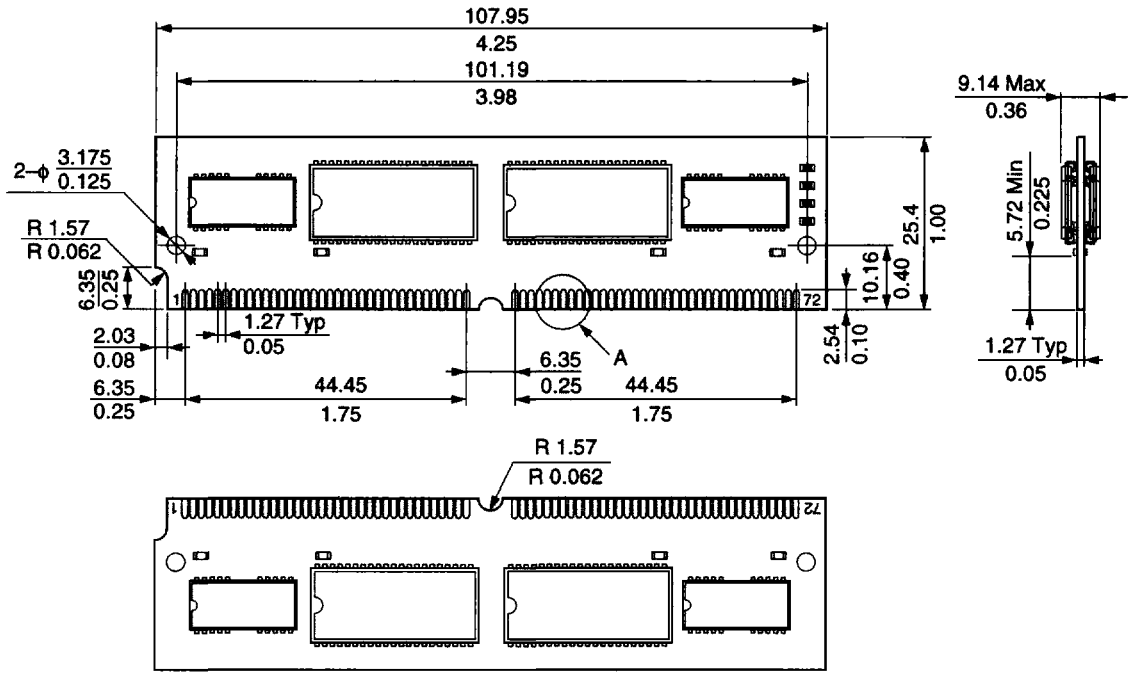


Fast Page Mode Early Write Cycle

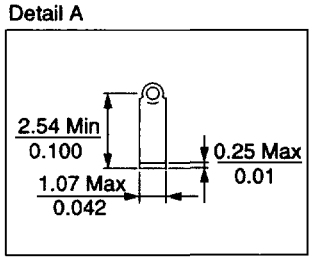


Physical Outline

Unit: mm/inch



Detail A



Notes : Following the specification of the contact pads.

Type code	Contact pad
HB56G236B-xx	Gold
HB56G236SB-xx	Solder