HA13568T

CD-ROM Combo Driver

HITACHI

ADE-207-247E (Z)
6th Edition
May 1, 1998

Description

The HA13568T is combination of Spindle, Forcus, Tracking, Slide, Tray designed for CD-ROM and have following function and features.

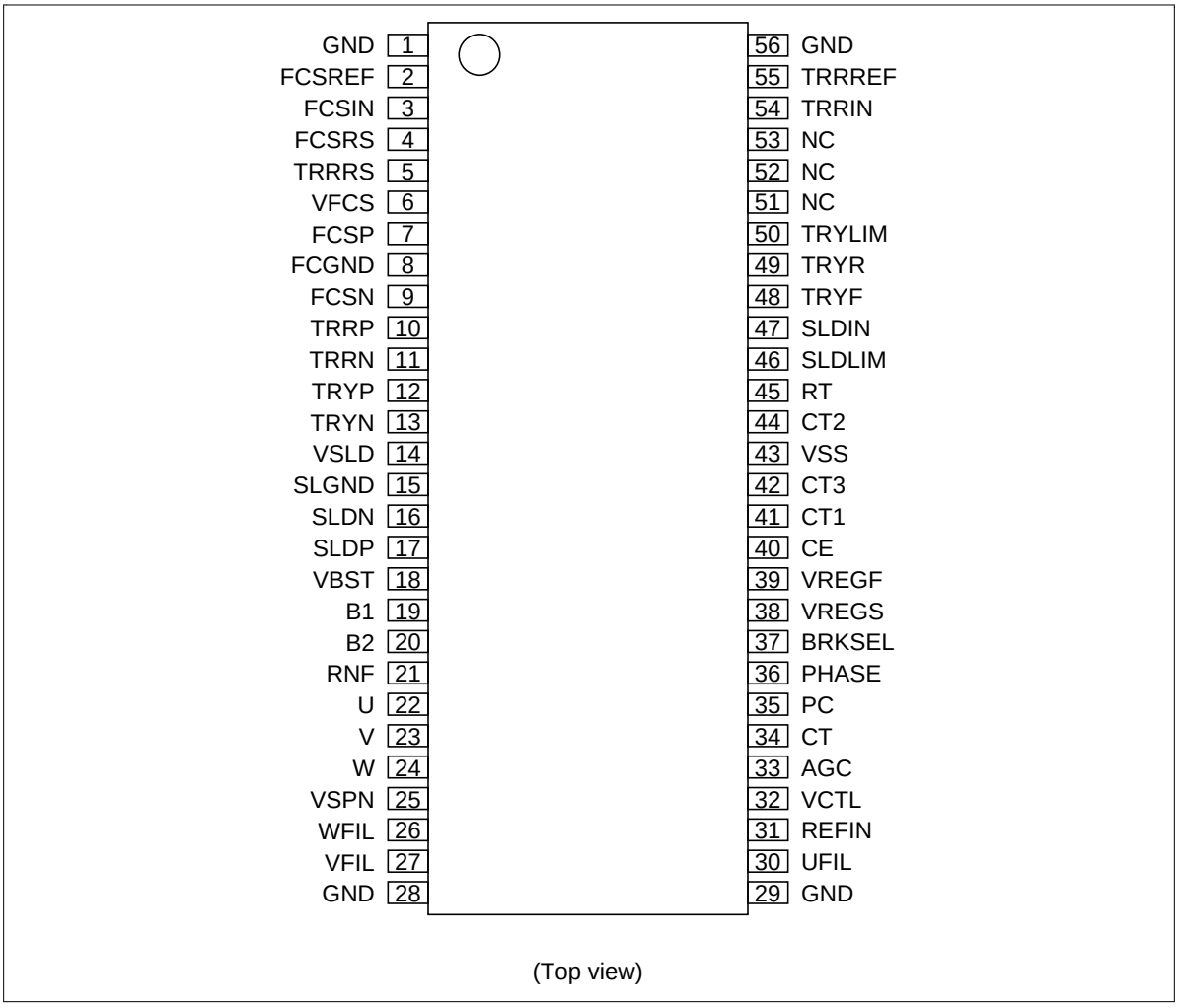
Features

- 1.5 A sensorless spindle driver
- 0.5 A BTL focus driver
- 0.5 A BTL tracking driver
- 1.5 A H bridge slide motor driver
- 0.5 A H bridge tray motor driver
- PWM filter
- Over temperature shut down (OTSD)
- Voltage regulator control circuit

Functions

- Sensorless driver with self start
- Soft switching drive
- Snubberless
- Low output saturation voltage
- Direct PWM slide driver

Pin Arrangement



(Top view)

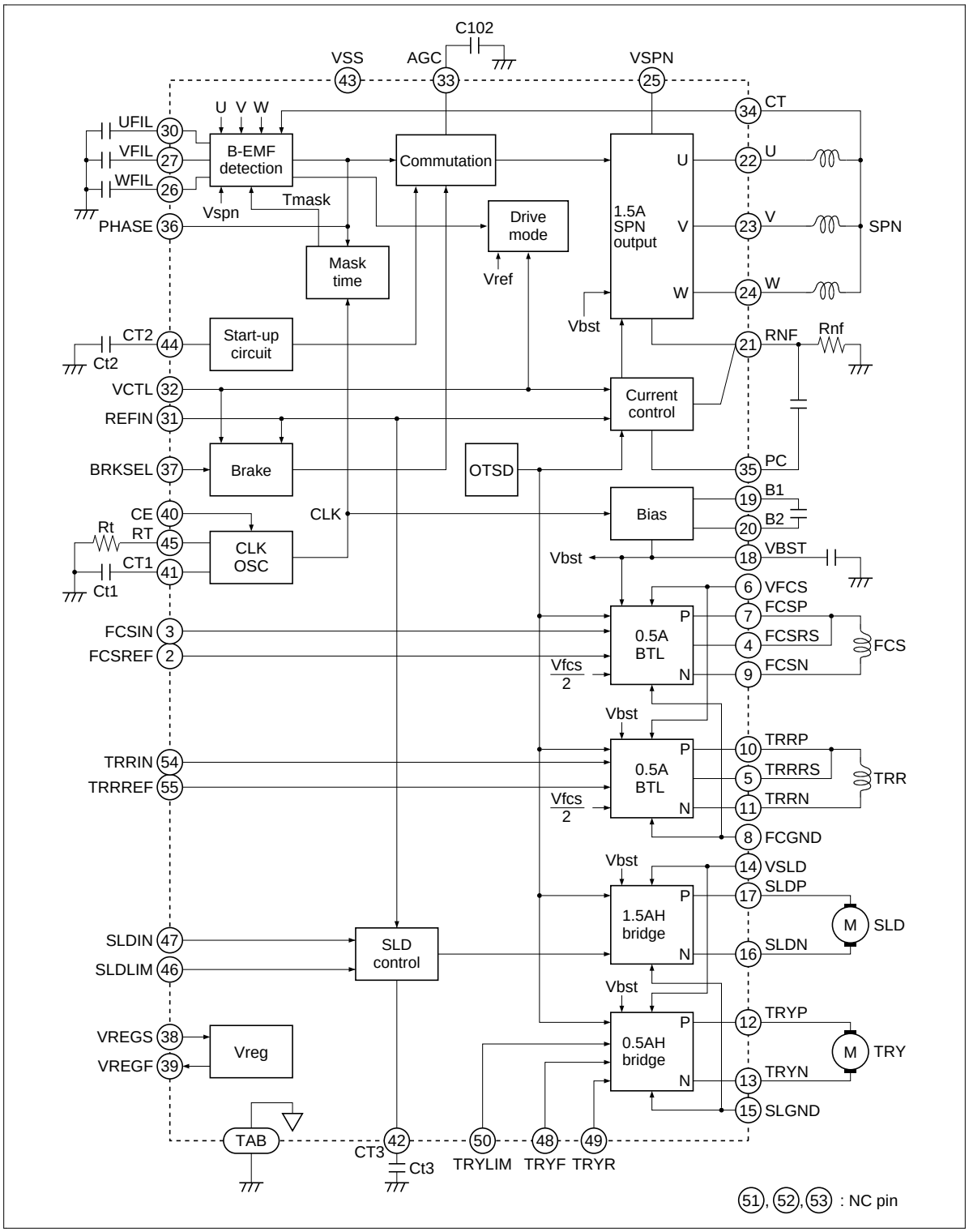
Pin Description

Pin No.	Pin Name	Function
2	FCSREF	FCS driver block reference voltage
3	FCSIN	FCS control input pin
4	FCSRS	FCS sense pin
5	TRRRS	TRR sense pin
6	VFCS	FCS driver and TRR driver power supply
7	FCSP	FCS driver P output
8	FCGND	FCS driver and TRR driver GND
9	FCSN	FCS driver N output
10	TRRP	TRR driver P output
11	TRRN	TRR driver N output
12	TRYP	TRY driver P output
13	TRYN	TRY driver N output
14	VSLD	SLD driver and TRY driver power supply
15	SLGND	SLD driver and TRY driver GND
16	SLDN	SLD driver N output
17	SLDP	SLD driver P output
18	VBST	Booster output pin. This circuit generates a voltage about 1.5 V above that of the VSPN pin.
19	B1	Booster pumping capacitor connection
20	B2	
21	RNF	Spindle driver current detection
22	U	U phase output
23	V	V phase output
24	W	W phase output
25	VSPN	Spindle and booster power supply
26	WFIL	W phase low pass filter. Connect a filter C to this pin during GND.
27	VFIL	V phase low pass filter. Connect a filter C to this pin during GND.
30	UFIL	U phase low pass filter. Connect a filter C to this pin during GND.
31	REFIN	Reference voltage of spindle and slide
32	VCTL	Spindle control input. Generates forward torque when a DC voltage higher than REFIN is applied, and brake when a DC voltage lower than REF is applied.
33	AGC	For AGC. Holds the level used for IC internal processing fixed even if the B-EMF level fluctuates due to the rotation speed.
34	CT	Spindle center tap
35	PC	Spindle driver phase compensation

Pin Description (cont)

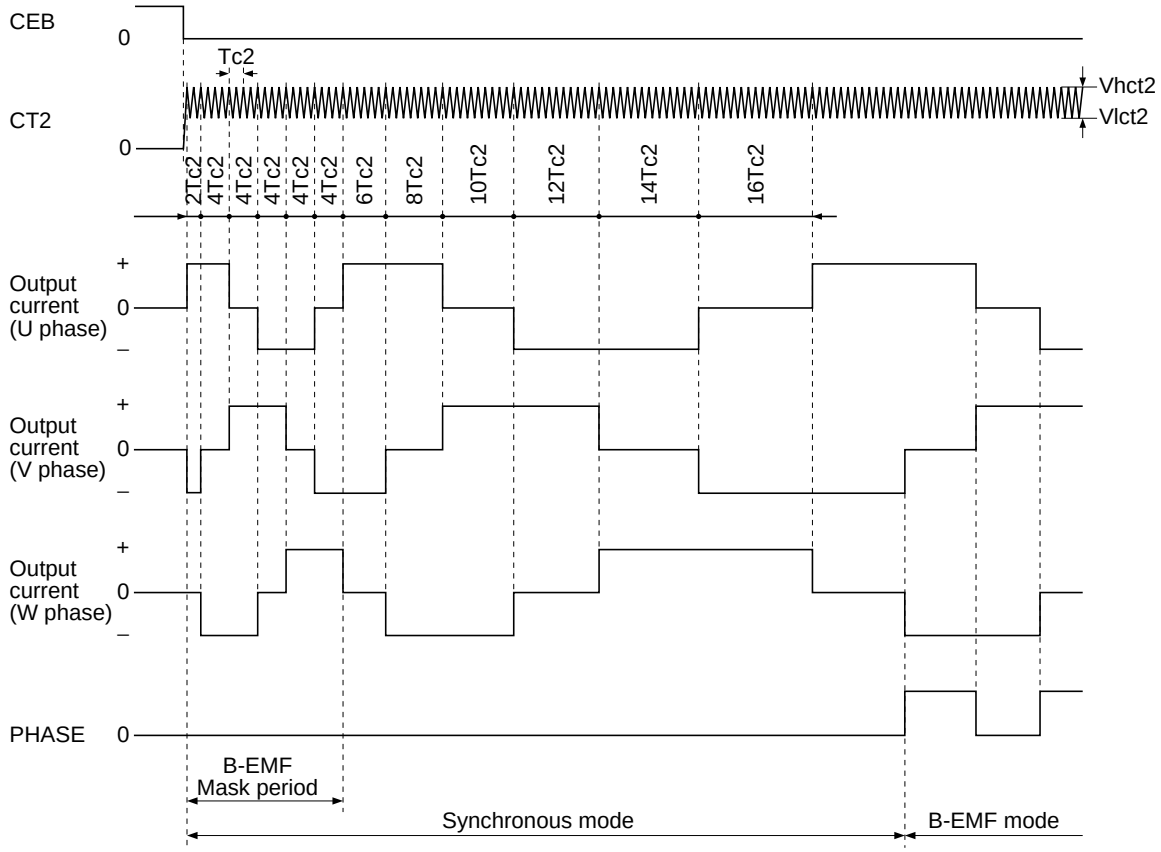
Pin No.	Pin Name	Function
36	PHASE	Outputs the B-EMF zero cross phase. Open corrector. (See the timing chart)
37	BRKSEL	To select the brake mode. Lo: Short brake, Hi: Reverse full brake (when forward torque input: BRKSEL = H)
38	VREGS	Voltage regulator sense pin (VREGS ≈ 3.3 V output)
39	VREGF	Voltage regulator force pin
40	CE	Chip enable. Input Hi: active
41	CT1	Time constant for clock oscillator circuit. The clock oscillator frequency is determined by the external capacitor and resistor Ct1 and Rt.
42	CT3	Time constant for PWM carrier oscillator. The carrier frequency is determined by the external capacitor and resistor Ct3 and Rt.
43	VSS	Control block power supply. 5 V
44	CT2	Time constant for start-up oscillator. The start-up oscillator frequency is determined by the external capacitor and resistor Ct2 and Rt.
45	RT	Reference voltage (3.3 V). The IC's internal reference current is determined by this voltage and the external resistor Rt.
46	SLDLIM	SLD output maximum duty setting
47	SLDIN	SLD control input pin
48	TRYF	TRY driver forward input
49	TRYR	TRY driver reverse input
50	TRYLIM	TRY output voltage setting pin
51	NC	No connection
52	NC	
53	NC	
54	TRRIN	TRR control input pin
55	TRRREF	TRR driver block reference voltage
1, 28, 29, 56, TAB		GND

Block Diagram



Timing Chart

1. Start-up

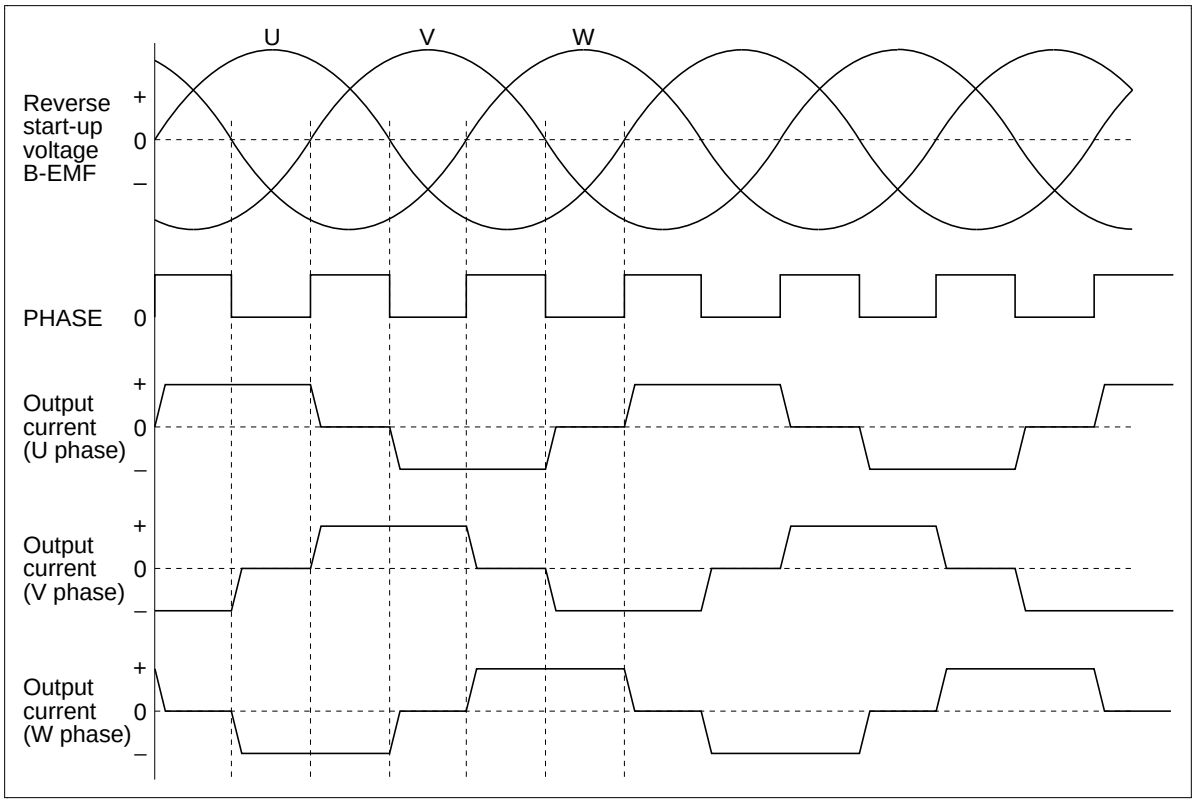


Note: Tc2 is as follows.

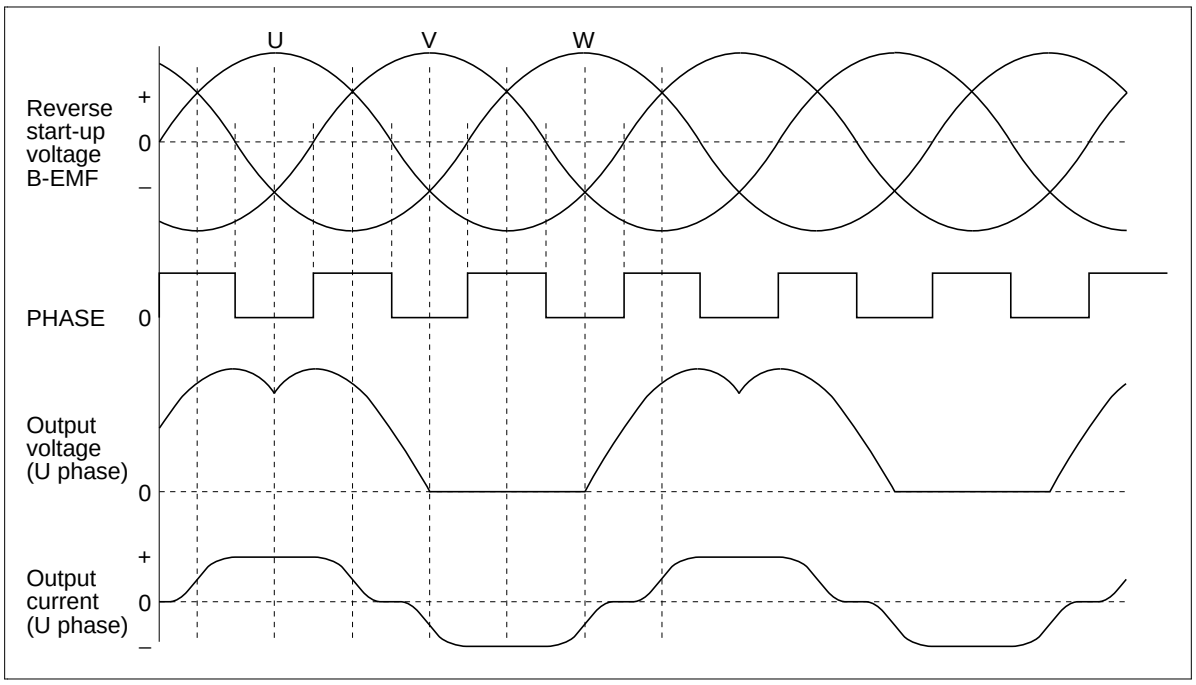
$$Tc2 = \frac{8\,(Vhct2 - Vlct2)\,Rt\,Ct2}{Vrt}$$

Where, Vhct2 : CT2 pin high voltage (See electrical characteristics)
Vlct2 : CT2 pin low voltage (See electrical characteristics)

2. Acceleration (switching mode)



3. Running (soft switching mode)



Truth Table

Table 1 Overall

CE	OTSD	SPN Driver	FCS Driver	TRR Driver	SLD Driver	TRY Driver
L	X	Z	Z	Z	Z	Z
H	ON	Z	Z	Z	Z	Z
	OFF	ON	ON	ON	ON	ON

Note: X: Option, Z: Hi impedance

Table 2 SPN Driver

BRKSEL	VCTL	SPN Driver
X	> REFIN	Forward torque
	REFIN	Z
L	< REFIN	Short brake
H	REFIN – 0.6 V	Reverse brake

Note: X: Option, Z: Hi impedance

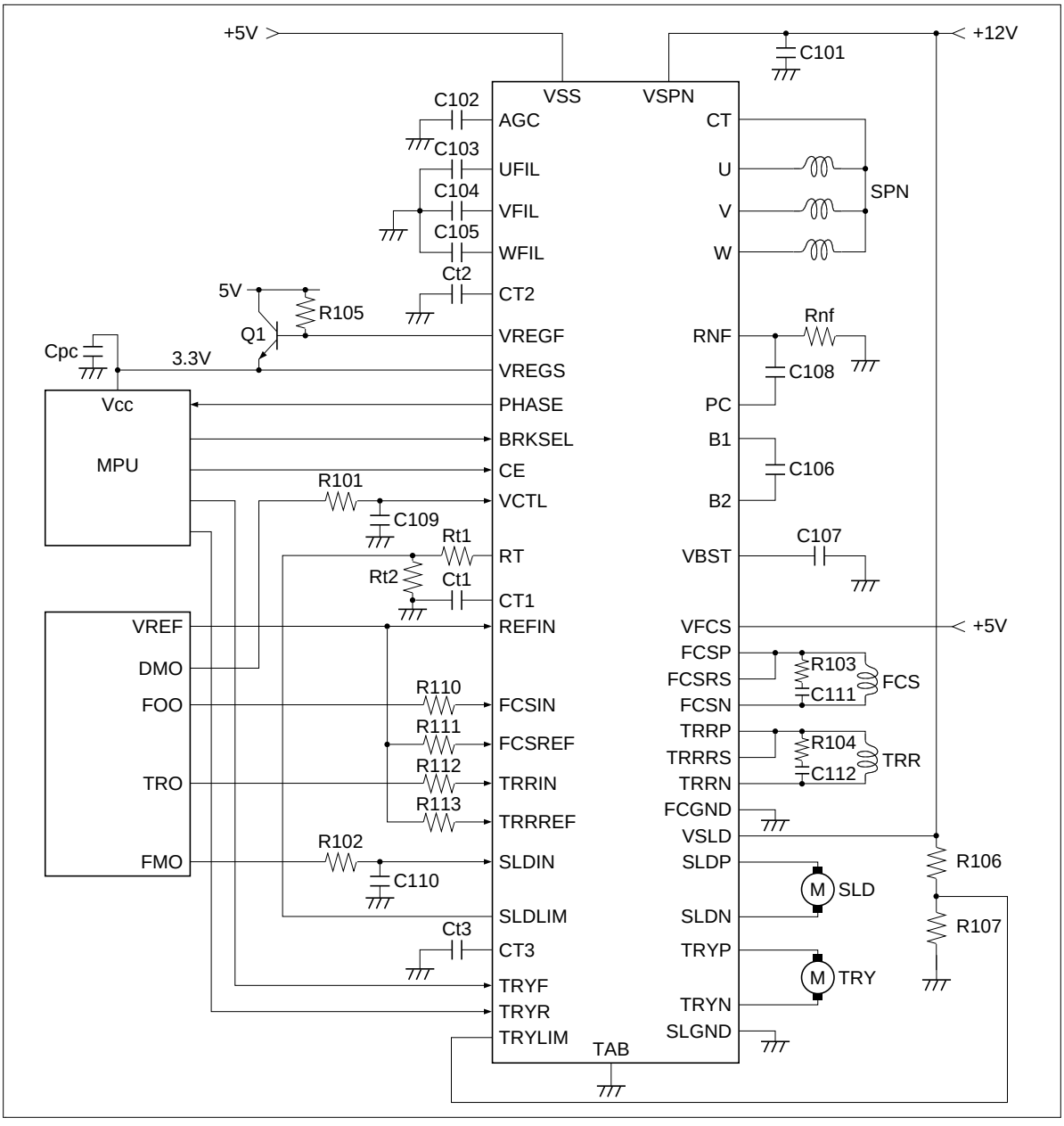
Table 3 TRY Driver

TRYF	TRYR	P Output	N Output
L	L	Z	Z
L	H	L	H
H	L	H	L
H	H	H	H

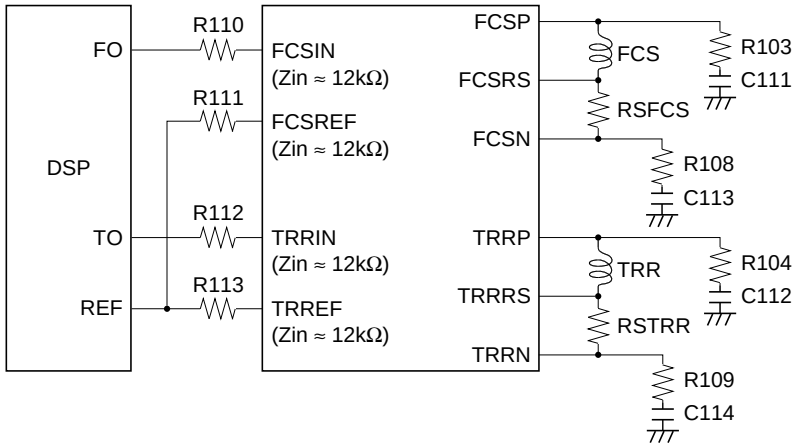
Note: Z: Hi impedance

Application

1. FCS, TRR voltage drive

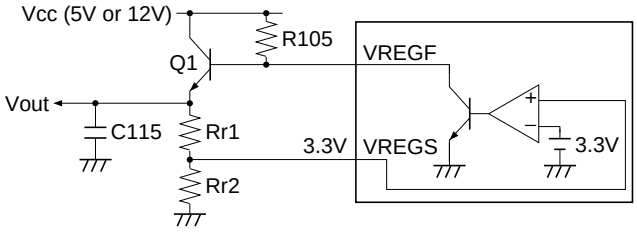


2. FCS, TRR voltage drive



Note: Other pins have the same connections as those used in application 1.

3. When used at a voltage other than 3.3 V with a voltage regulator (Vout = 3.3 to Vcc – 1 V)



Note: Other pins have the same connections as those used in application 1.

External Components

Parts No.	Recommended Value	Recommended Range	Purpose	Note
R101	47 kΩ	≤ 47 kΩ	Filter for SPN driver control input	
R102	47 kΩ	≤ 47 kΩ	Filter for SLD driver control input	
R103	6.8 Ω	—	To stop FCS block oscillation	
R104	6.8 Ω	—	To stop TRR block oscillation	
R105	500 Ω	≥ 100 Ω	for Q1 bias	
R106	20 kΩ	—	for TRY driver output voltage setting	
R107	27 kΩ	—		
R108	6.8 Ω	—	To stop FCS block oscillation	
R109	6.8 Ω	—	To stop TRR block oscillation	
R110 to R113	20 kΩ	—	for BTL gain setting	7
Rnf	0.25 Ω	≥ 0.25 Ω	SPN driver current detection resistor	1
Rt1	1.8 kΩ	Rt1 + Rt2 = 10 kΩ	Reference current setting and SLD driver maximum duty setting	2 to 5
Rt2	8.2 kΩ			
RSFCS	1 Ω	≥ 0.33 Ω	for FCS driver current sense	7
RSTRR	1 Ω	≥ 0.33 Ω	for TRR driver current sense	
Rr1	—	—	Voltage regulator division resistor	8
Rr2	—	—		
C101	0.1 µF	≥ 0.1 µF	for Power supply by passing	
C102	0.047 µF		for B-EMF Amplitude AGC	
C103	0.01 µF		for B-EMF filter	6
C104				
C105				
C106	0.22 µF	≥ 0.22 µF	for Booster pumping	
C107	0.47 µF	≥ 0.47 µF	for Booster output smoothing	
C108	0.1 µF		for SPN driver phase compensation	
C109	0.01 µF		Filter for SPN control input	
C110	3300 pF		Filter for SLD control input	
C111	0.01 µF	—	To stop FCS block oscillation	
C112	0.01 µF	—	To stop TRR block oscillation	
C113	0.01 µF	—	To stop FCS block oscillation	
C114	0.01 µF	—	To stop TRR block oscillation	
C115	2.2 µF		for Voltage regulator smoothing	

External Components (cont)

Parts No.	Recommended Value	Recommended Range	Purpose	Note
Ct1	150 pF	≥ 120 pF	Time constant for CLK oscillation. Use a capacitor with good temperature characteristics.	3
Ct2	0.033 μF		Time constant for start-up oscillation. Use a capacitor with good temperature characteristics.	4
Ct3	470 pF	≥ 390 pF	PWM carrier oscillation time constant	5
Q1			Transistor for voltage regulator	

Note:

1. The output current maximum value Iospnmax of SPN driver is controlled according to the following equation. However, Vspncl is the current limited reference voltage. (See the electrical characteristics)

$$Iospnmax = \frac{Vspncl}{Rnf}$$

2. The maximum duty Dmax of SLD driver output is controlled according to the following equation.

$$Dmax = \frac{Vrt}{Vhct3 - Vlct3}\left(\frac{Rt2}{Rt} - \frac{Vlct3}{Vrt}\right) \times 100\ (\%)$$

However,

$$Rt = Rt1 + Rt2, \quad \frac{Rt2}{Rt} \geq \frac{Vlct3}{Vrt}$$

Where, Vrt : RT pin voltage (See the electrical characteristics)
Vlct3 : CT3 pin low voltage (≈ 1.3 V)
Vhct3 : CT3 pin high voltage (≈ 3.3 V)

Since Vrt ≈ Vhct3, Dmax is not limited at 100% when Rt1 = 0 Ω.

3. The CLK oscillation frequency is determined by the following equation.

$$fclk = \frac{Vrt}{8\ Ct1\ Rt\ \Delta Vct1}$$

Where, Vrt : RT pin voltage (See the electrical characteristics)
ΔVct1 : CT1 pin voltage amplitude (≈ 1 V)

4. The Ct2 for start-up oscillation is determined by the following equation.

$$Tc2 = \frac{1}{6}\sqrt{\frac{J}{P\ Kt\ Ispnmax}}$$

$$Ct2 = \frac{Tc2\ Vrt}{8\ Rt\ (Vhct2 - Vlct2)}$$

Where, J : Spindle motor inertia (kg · cm · S^2)
P : Number of spindle motor poles (Total number of S poles and N poles)
Kt : Spindle motor torque constant (kg · cm / A)
Vhct2 : CT2 pin high voltage (≈ 3.3 V)
Vlct2 : CT2 pin low voltage (≈ 1.3 V)

5. The PWM oscillation frequency fpwm is determined by the following equation.

$$fpwm = \frac{Vrt}{8\ Ct3\ Rt\ (Vhct3 - Vlct3)}$$

Where, Vhct3 : CT3 pin high voltage (≈ 3.3 V)
Vlct3 : CT3 pin low voltage (≈ 1.3 V)

6. The C103 to C105 for B-EMF filter are determined by the following equation.

$$C103 = \frac{6}{\pi \, Rflt \, No \, P}$$

Where, Rfill : B-EMF detection output resistor (See the electrical characteristics)
No : Maximum rotation speed (rpm)

7. The FCS and TRR is determined by the following equation.

Voltage drive:

$$Gv = \frac{R1}{Rin + R2}$$

Current drive:

$$Gm = \frac{R1}{((Rin + R2) \cdot Rs)}$$

Where, R1 : Resistor of IC inside (≈30kΩ)
R2 : Resistor of IC inside (≈7kΩ)
Rin : Resistor value inserted in the input (Ω)
(R110 to R113)
Rs : Current sense resistor (Ω)

8. The output voltage Vout of voltage regulator is determined by the following equation.

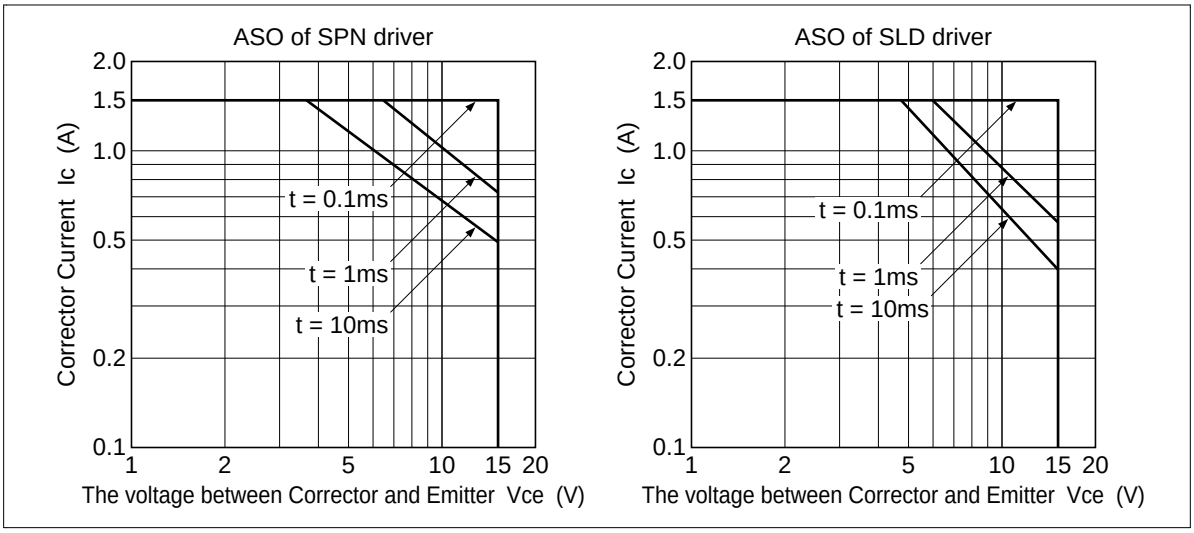
$$Vout = 3.3\left(1 + \frac{Rr1}{Rr2}\right)$$

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Supplu voltage	Vss	7	V	1
SPN supply voltage	Vspn	15	V	1
FCS & TRR supply voltage	Vfcs	15	V	1
SLD & TRY supply voltage	Vsld	15	V	1
Input voltage	Vin	0 to Vss	V	2
SPN output current	Iospn	1.5	A	3
FCS & TRR & TRY output current	Iofcs	0.5	A	3
SLD output current	Iosld	1.5	A	3
Power dissipation	P_T	5	W	4
Junction temperature	Tj	160	°C	1
Storage temperature range	Tstg	–55 to +125	°C	

Note: 1. Operating voltage range is shown below.
Vss = 4.25 to 5.75 V
Vspn = 4.25 to 13.8 V
Vfcs = 4.25 to 13.8 V (However, the output is clamped at 7 V.)
Vsld = 4.25 to 13.8 V
Tjopr = 0 to +135°C
2. Applied to BRKSEL, VCTL, REFIN, CE, FCSIN, FCSREF, TRRIN, TRRREF, SLDIN, SLDLIM, TRYF, TRYR and TRYLIM.

3. ASO (Area of Safety Operation) of each output transistor is shown below (TBD).



4. Thermal resistance is shown below.

   θj-tab ≤ 12°C / W (back side tab soldering area is 70% or more)

   θj-a ≤ 25°C / W (mounted on 4 layer multi glass-epoxy board, back side tab soldering area is 70% or more)

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Quiescent current		Iss0	—	0.7	0.9	mA	CE = L	VSS	
		Ispn0	—	—	0.2	mA		VSPN	
		Ifcs0	—	—	0.01	mA		VFCS	
		Isld0	—	—	0.01	mA		VSLD	
		Iss1	14	20	25	mA	CE = H, VCTL =	VSS	
		Ispn1	11	15	20	mA	FCSIN = TRRIN =	VSPN	
		Ifcs1	6	10	15	mA	SLDIN = REFIN,	VFCS	
		Isld1	—	—	1.0	mA	TRYF = TRYR = L All load open	VSLD	
		Iss2	20	33	60	mA	CE = H, VCTL =	VSS	
		Ispn2	11	30	50	mA	FCSIN = TRRIN =	VSPN	
		Ifcs2	7	10	15	mA	SLDIN = 5 V,	VFCS	
		Isld2	–15	–1.0	1.0	mA	TRYF, TRYR = H, L, All load open	VSLD	
Logic input	Input current	Iince	0	70	100	µA	Vin = 0 to 5 V	BRKSEL, CE, FPWMP, FPWMN, TPWMP, TPWMN, SPWMP, SPWMN, TRYF, TRYR	
		Iin	—	—	±10	µA			
	Low level voltage	Vil	—	—	0.8	V			
	High level voltage	Vih	2.0	—	—	V			
Logic output	Low level voltage	Vol	—	—	0.4	V	Io = 1 mA	PHASE	
	Leak current	Icer1	—	—	±10	µA	Vce = 15 V		
SPN driver	Output saturation voltage	Vsatspn	—	1.25	1.75	V	Iospn = 1.0 A	U, V, W	1
	Leak current	Icer2	1.3	2.2	3	mA	Vce = 15 V		
	Current limiter voltage	Vspncl	238	265	292	mV	Rnf = 0.25 Ω	RNF	2
FCS driver	Input resistance	Rinfcs	9.6	12	14.4	kΩ		FCSIN	
		Rinfcsref	9.6	12	14.4	kΩ			
	Input voltage range	Vinfcs	0	—	5	V			

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
FCS driver	Output quiescent voltage	Vqfcs	2.375	2.5	2.625	V	FCSIN=FCSREF= 2.5 V, VFCS=5 V	FCSP, FCSN	3
	Output offset voltage	Vosfcs	—	—	±20	mV			
	Output saturation voltage	Vsatfcs	—	1.0	1.4	V	Io = 0.33 A		1
	Voltage gain	Gvfcs	11.6	12.6	13.6	dB			4
	Gain band width	Bfcs	100	—	—	kHz	ΔGv = –3 dB		
TRR driver	Input resistance	Rintrr	9.6	12	14.4	kΩ		TRRIN	
		Rintrrref	9.6	12	14.4	kΩ			
	Input voltage range	Vintrr	0	—	5	V			
	Output quiescent voltage	Vqtrr	2.375	2.5	2.625	V	FCSIN=TRRREF= 2.5 V, VFCS=5 V	TRRP, TRRN	3
	Output offset voltage	Vostrr	—	—	±20	mV	FCSIN = REF		
	Output saturation voltage	Vsattrr	—	1.0	1.4	V	Io = 0.33 A		1
	Voltage gain	Gvtrr	11.6	12.6	13.6	dB			4
	Gain band width	Btrr	100	—	—	kHz	ΔGv = –3 dB		
SLD driver	Output saturation voltage	Vsatsld	—	1.5	2.0	V	Iosld = 0.75 A	SLDP, SLDN	1
	Leak current	Icer3	—	—	±100	μA	Vce = 15 V		
	Penetration current	Iovlap	—	—	100	mA		VSLD	8
	Transient response	tplh1	—	—	5	μs		SLDP,	
	time	tphl1	—	—	5	μs		SLDN	
TRY driver	Output saturation voltage	Vsattry	—	1.0	1.4	V	Iotry = 0.33 A	TRYP, TRYN	1
	Leak current	Icer3	—	—	±100	μA	Vce = 15 V		
	Penetration current	Iovlap	—	—	100	mA		VSLD	8
	Transient response	tplh1	—	—	5	μs		TRYP,	
	time	tphl1	—	—	5	μs		TRYN	
	Input current	Iintrylim	—	—	±5	μA	Vtrylim=7 to VSLD		
	Output voltage	Vlimtry	0.1	0.7	1.0	V	R_L = 16Ω, Vtrylim = 7 V		9

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
SPN	Input current	Iinspn	—	—	±5.0	µA	Vctl = 0 to Vss–1V	VCTL,	2
current	REF voltage range	Vref	1.6	—	3.0	V		REFIN	
control	Dead zone voltage	Vdzspn	±50	—	±120	mV	Vref reference		
	Current control gain	Gctl	—	–12	±1.5	dB		RNF	
Drive	Change threshold	Vctl	—	0.5	±0.1	V	Vref reference	VCTL	5
mode	voltage	fbemf	—	≥f_{CT2}	±50%	Hz	SOFT SW mode	U, V, W	5
	SW ↔ SOFT SW		—	<f_{CT2}	–20%	Hz	SW mode		
B-EMF detection	Output resistance	Rflt	—	10	±20%	kΩ		UFIL, VFIL, WFIL	
	Threshold voltage of PHASE occurrence	Viemf	—	40	±50%	mVpp	VSPN ≥ Vss + 3V_F	U, V, W	6
			—	28	±50%	mVpp	VSPN ≤ Vss + 3V_F		
CLK	RT voltage	Vrt	3.135	3.30	3.465	V		RT	
OSC	CLK oscillation frequency	fclk	210	240	270	kHz	Rt = 10 kΩ, Ct1 = 82 pF	CT1	
Start-up circuit	Start-up oscillation frequency	fct2	437	485	534	Hz	Rt = 10 kΩ, Ct2 = 0.033 µF	CT2	
SLD	Input current	Iinsld	—	—	±5.0	µA	Vsld = 0 to Vss–1V	SLDIN	
control	Input voltage range	Vinsld	0	—	4.0	V			
	Limiter input current	Isldlim	—	—	±5.0	µA		SLDLIM	
	PWM oscillation frequency	fpwm	33	38	42.35	kHz	Rt = 10 kΩ, Ct3 = 470 pF		
	Control gain	D/V	80	90	100	%/V			7
	Offset voltage	Vossld	—	—	20	mV	SLDIN = REFIN		
Voltage regulator	Output sink current	Isinkreg	8.5	12.2	—	mA	VREGS = 4 V, VREGF = 4 V		
	Output voltage	Voutreg	3.135	3.30	3.465	V			
OTSD	Operating temperature	Tsd	135	160	—	°C			8
	Hysteresis	Thys	—	50	—	°C			

Note: 1. The output saturation voltage is the sum of the upper and lower saturation voltages.

2. See figure 1. Where,

$$Gctl = 20 \log \frac{\Delta Vrnf}{\Delta Vctl}$$

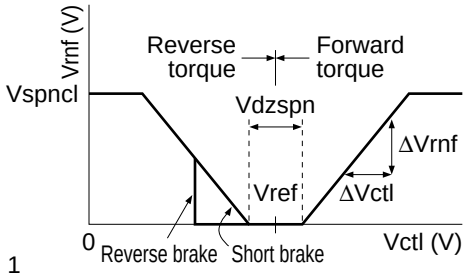


Figure 1

3. Where,

$$Vqfcs = \frac{Vfcsp + Vfcsn}{2}$$

$$Vqtrr = \frac{Vtrrp + Vtrrn}{2}$$

4. See figure 2. Where,

$$Gvfcs = 20 \log \left(\frac{\Delta Vfcsp}{\Delta Vfcsin} \quad \frac{\Delta Vfcsn}{\Delta Vfcsin} \right)$$

$$Gvtrr = 20 \log \left(\frac{\Delta Vtrrp}{\Delta Vtrrin} \quad \frac{\Delta Vtrrn}{\Delta Vtrrin} \right)$$

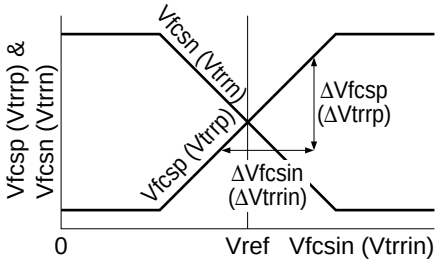


Figure 2

5. The circuit operates in soft switching drive mode only when the control input (Vctl) is lower than f_{CT2} and f_{PHASE} is higher than the threshold voltage. See figure 3.

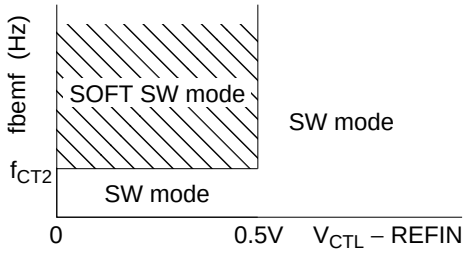


Figure 3

6. PHASE is output only when B-EMF exceeds the threshold voltage.

7. See figure 4. Where,

$$D/V = \frac{\Delta D}{\Delta Vin}$$

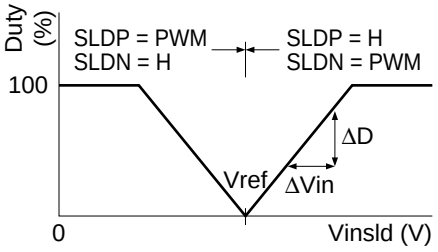
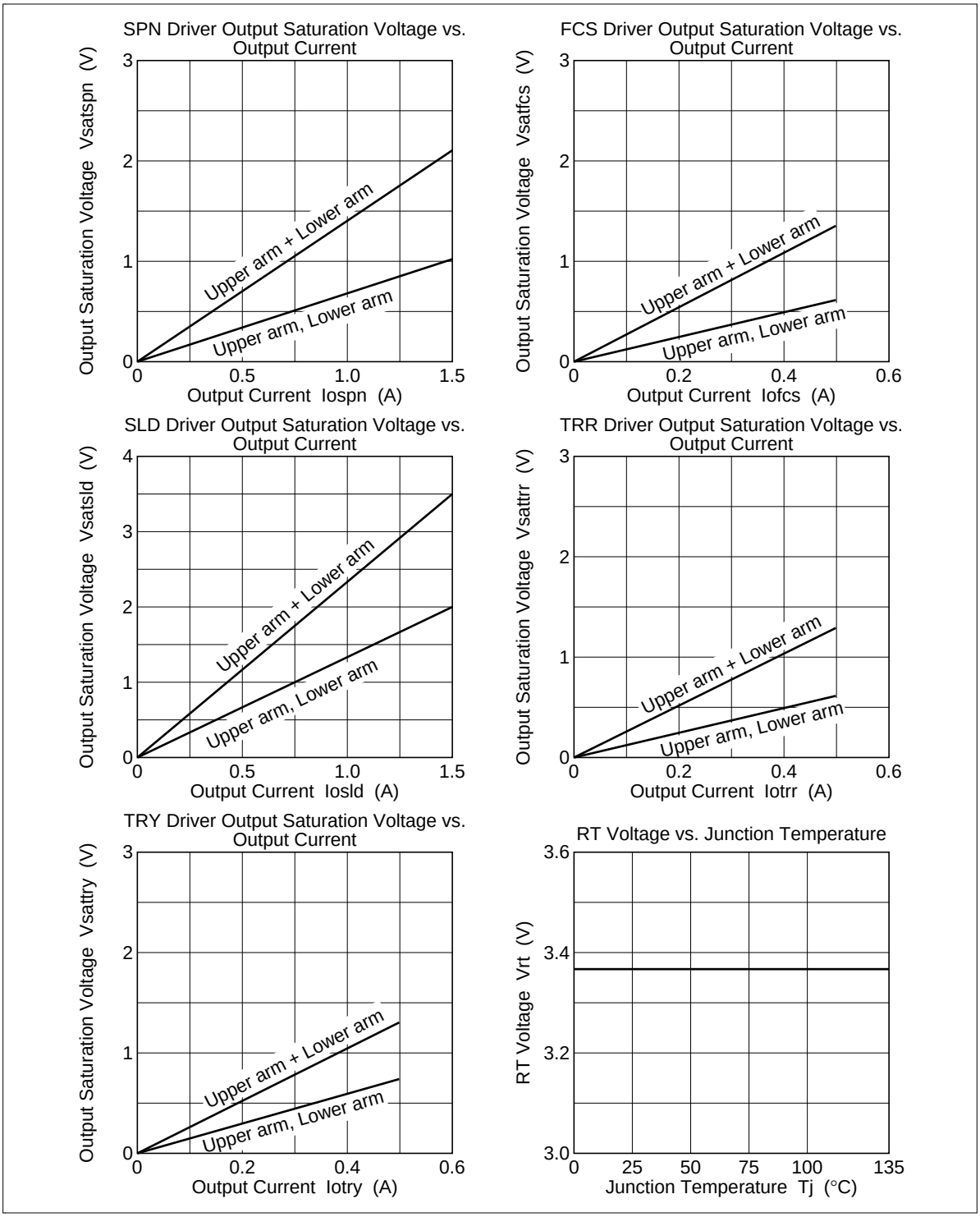


Figure 4

8. Design guide only.

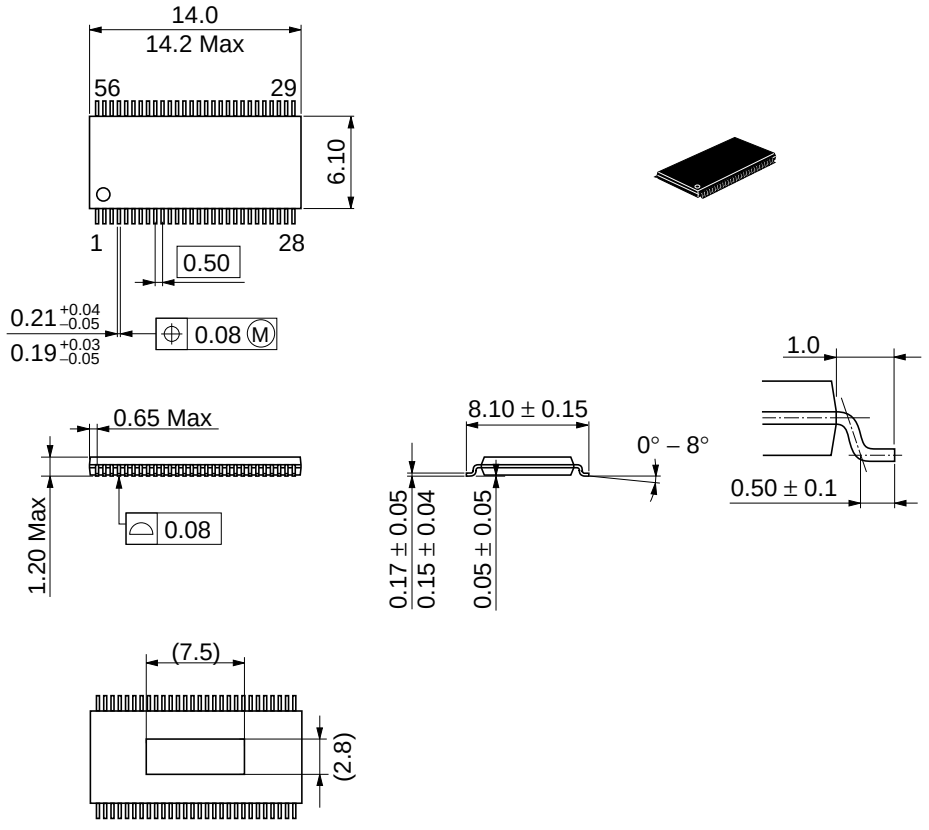
9. Vlimtry = VTRYP – VTRYLIM, or VTRYN – VTRYLIM

Reference Data



Package Dimensions

Preliminary Unit: mm



Hitachi Code	TTP-56DT
JEDEC	—
EIAJ	—
Weight (reference value)	0.32 g

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax:303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071