mosaic

Mosaic Semiconductor Inc.

32K X 8 EEPROM

MEM832V/J-90/12/15

Issue 2.1 : May 1993

PRELIMINARY

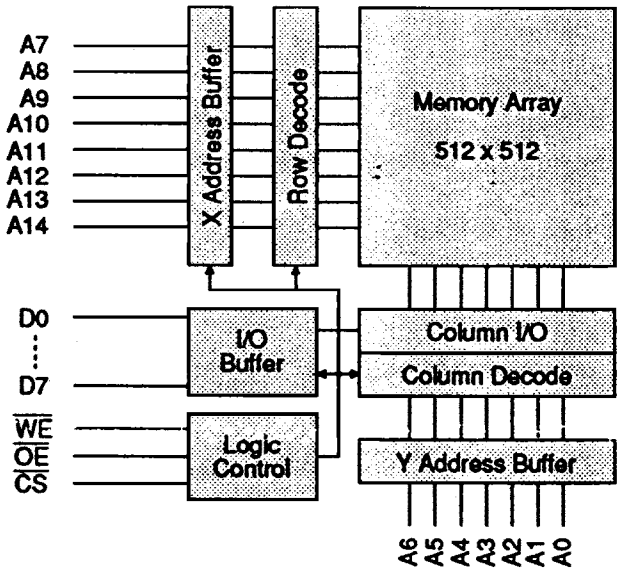
32,768 x 8 High Speed CMOS EEPROM

Features

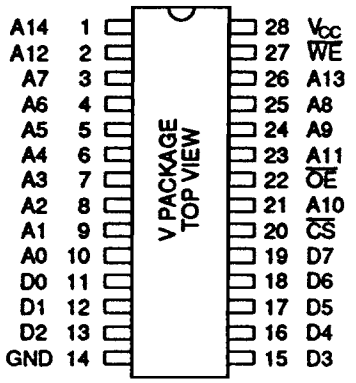
Very Fast Access Times of 90/120/150 ns.
VIL™ and JLCC packages available.
JEDEC Approved Byte-wide pinout
Operating Power 440 mW (max)
Standby Power 16.5 mW (max TTL)
1.65 mW (max CMOS)
Hardware and Software Data Protection.
64 Byte Page Operation.
DATA Polling/Toggle Bit for End of Write Detection.
10^4 Erase/Write cycles & 10 year Data Retention.
Completely Static Operation.
May be Screened in as MIL-STD-883 (suffix MB)

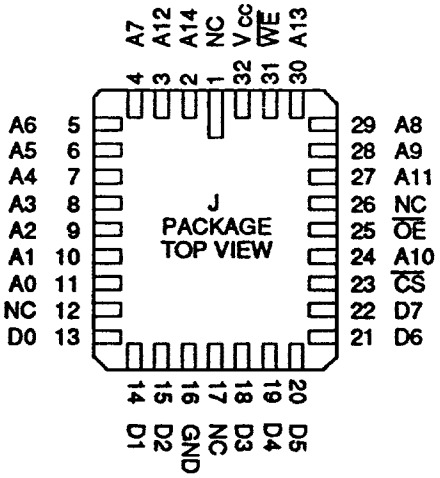
VIL is a Trademark of Mosaic Semiconductor Inc.

Block Diagram



Pin Definitions





Pin Functions

A0-A14	Address	D0-7	Data I/O
CS	Chip Select	WE	Write Enable
OE	Output Enable	NC	No Connect
V_{cc}	Power	GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	JEDEC

Package dimensions and outlines are displayed on page 9.

VIL is a trademark of Mosaic Semiconductor, U.S. Patent number D316251.

Absolute Maximum Ratings

Voltage on any pin relative to GND	V_T	-0.6V to +6.25	V
Voltage on $\overline{OE}$ and A9 relative to GND	V_{OEA}	-0.6V to +13.5	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature Under Bias	T_{BAS}	-55 to +125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (MEM832I)
	T_{AM}	-55	-	125	°C (MEM832M,MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{CC}+1V$	-	10	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	-	10	µA
Average Current	I_{CC1}	f = 5 MHz, $I_{I/O}$=0mA	-	80	mA
Standby Current TTL	I_{SB}	$2.0V \le \overline{CS} \le V_{CC}+1V$	-	3	mA
Standby Current CMOS	I_{SB1}	$V_{CC}-0.3V \le \overline{CS} \le V_{CC}+1V$	-	300	µA
Output Voltage	V_{OL}	I_{OL}=6mA	-	0.45	V
	V_{OH}	I_{OH}=-4mA	2.4	-	V
Write Inhibit Voltage	V_{WI}		3.0	-	V

Capacitance (V_{CC}=5V±10%, T_A=25°C, f=1MHz)

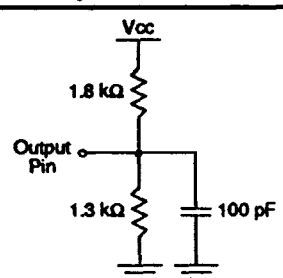
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	C_{IN}	V_{IN} = 0V	4	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	8	12	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

* Input pulse levels: 0.8V to 2.4V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Test Load



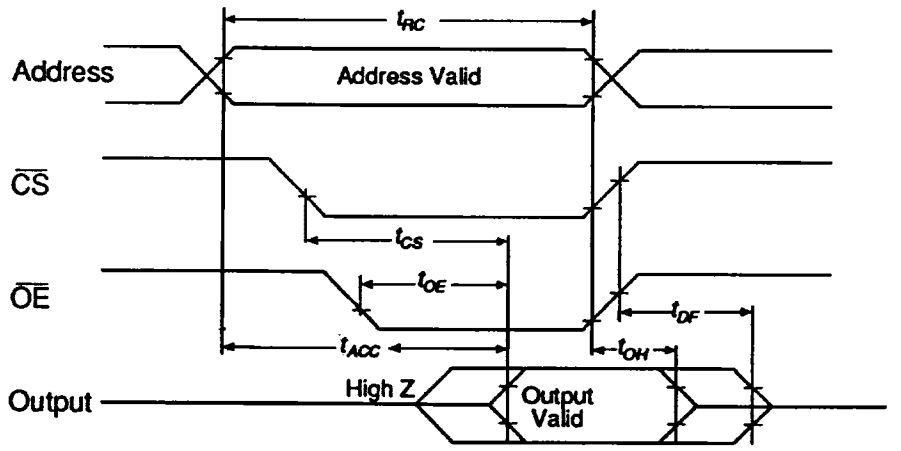
Electrical Characteristics and Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-90 min	-90 max	-12 min	-12 max	-15 min	-15 max	Unit	Notes
Read Cycle Time	t_{RC}	90	-	120	-	150	-	ns	
Address to Output Delay	t_{ACC}	-	90	-	120	-	150	ns	
$\overline{CS}$ to Output Delay	t_{CS}	-	90	-	120	-	150	ns	(1)
$\overline{OE}$ to Output Delay	t_{OE}	0	45	0	50	0	50	ns	(2)
$\overline{CS}$ or $\overline{OE}$ to Output Float	t_{DF}	0	45	0	50	0	50	ns	(3,4)
Output Hold from $\overline{OE}$, $\overline{CS}$ or Address, (whichever occured first)	t_{OH}	0	-	0	-	0	-	ns	

Notes: (1) $\overline{CS}$ may be delayed up to $t_{ACC} - t_{CS}$ after the address transition without impact on t_{ACC}.
(2) $\overline{OE}$ may be delayed up to $t_{CS} - t_{OE}$ after the falling edge of $\overline{CS}$ without impact on t_{CS} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
(3) t_{DF} is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5pF).
(4) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform

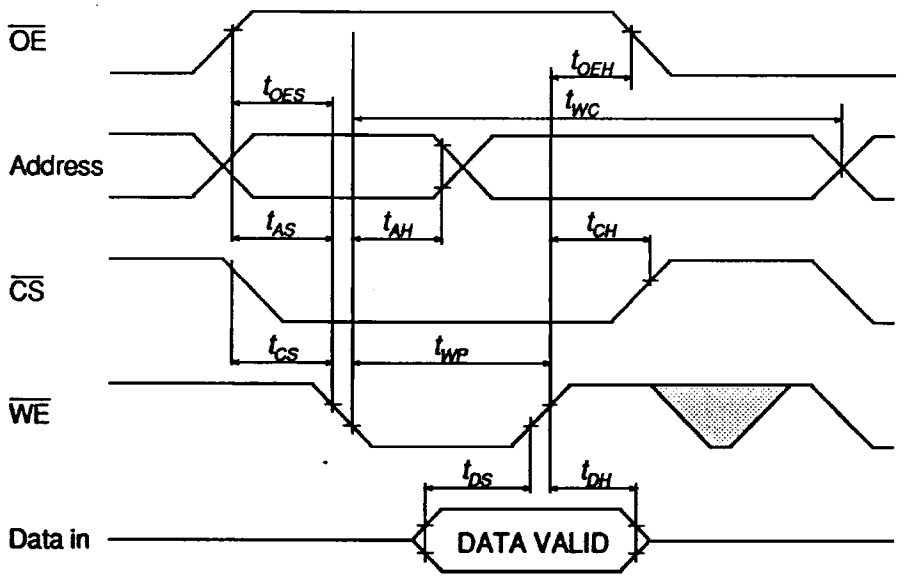


Write Cycle

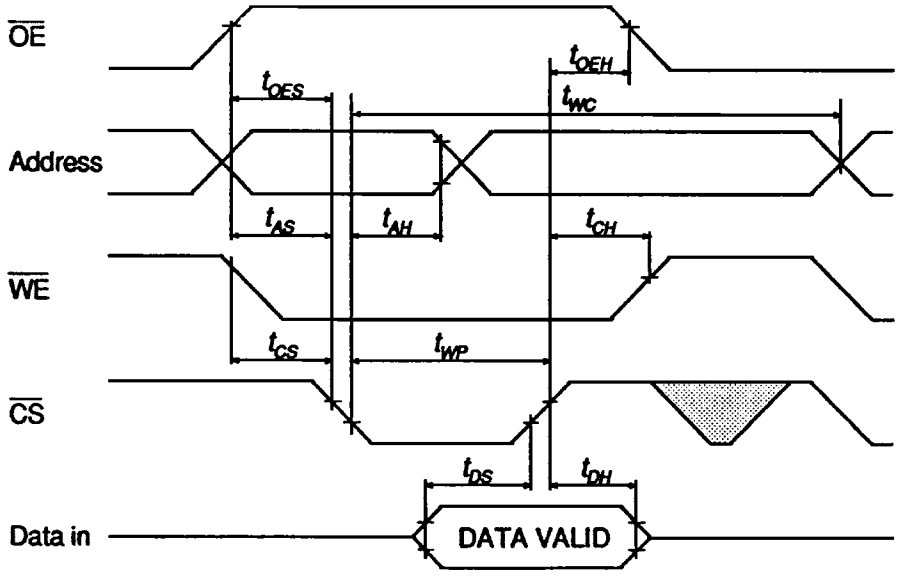
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	12	ms
Address, $\overline{OE}$ Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	-	-	ns

Note: (1) NR = No Restriction

AC Write Waveform - $\overline{WE}$ Controlled



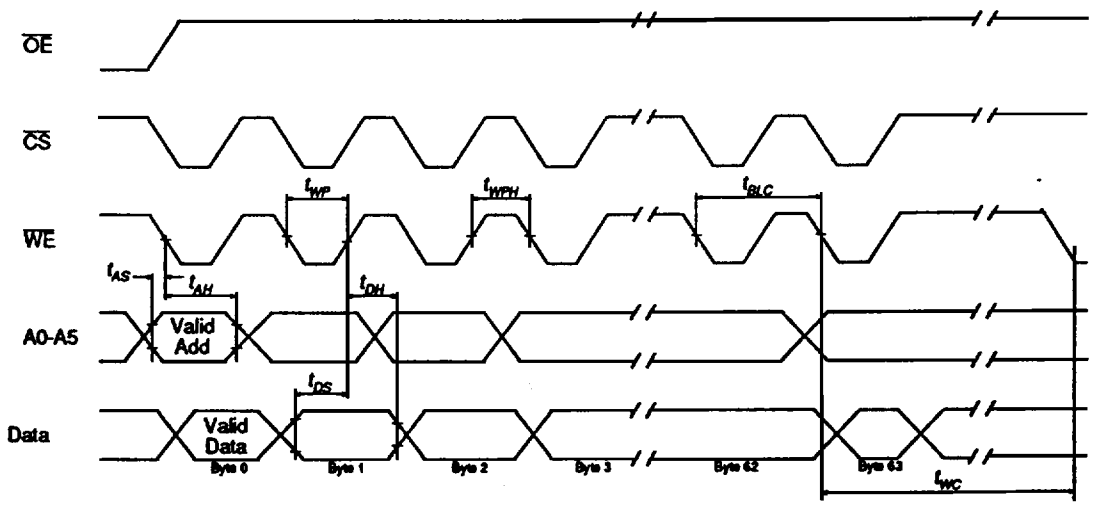
AC Write Waveform - $\overline{CS}$ Controlled



Page Mode Write Cycle

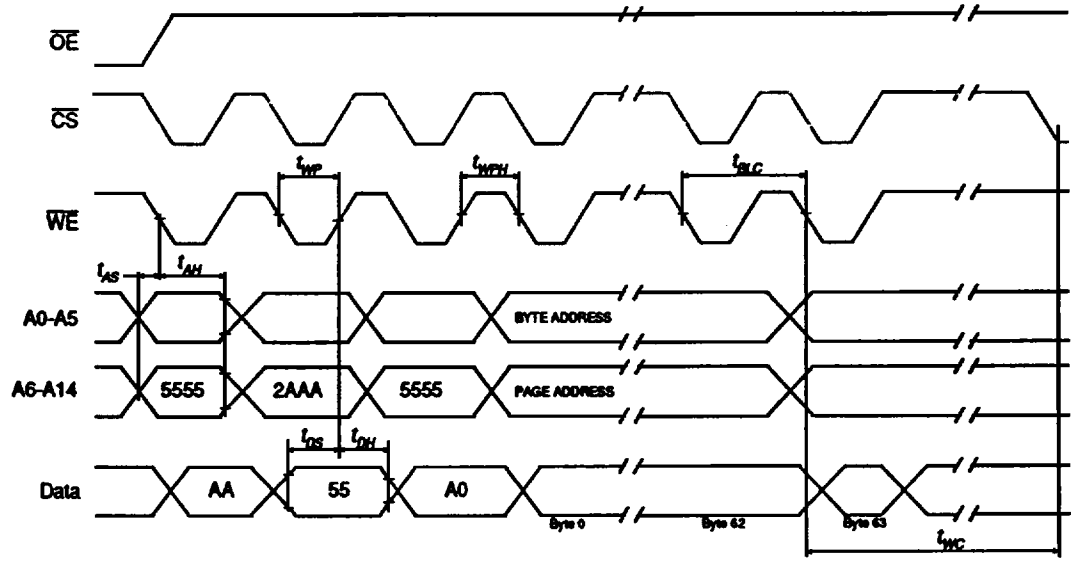
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	12	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte Load Cycle Time	t_{BLC}	.2	-	150	µs
Write Pulse Width High	t_{WPH}	50	-	-	ns

Page Mode Write Waveform



Note: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

Software Protected Write Waveform



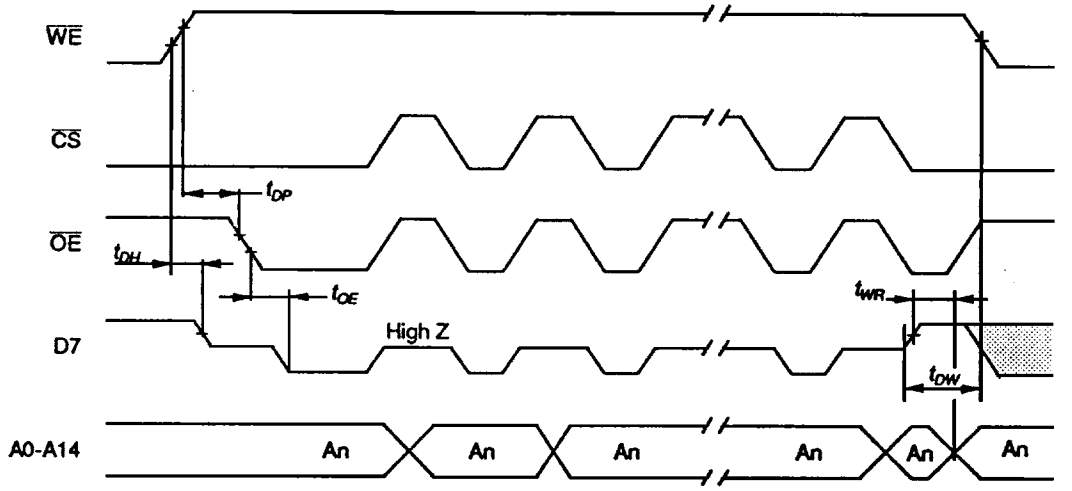
Note: A6 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$) after the Software code has been entered. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

DATA Polling Characteristics (1)

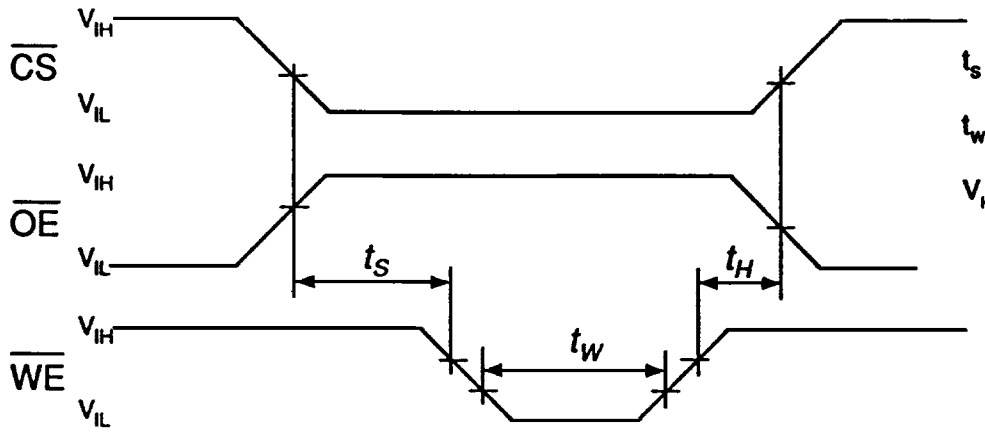
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	0	-	-	ns
WE High to Data Polling	t_{DP}	500	-	-	µs
OE to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{WR}	0	-	-	ns
Delay to Next Write	t_{DW}	10	-	-	µs

Note : (1) These parameters are sampled and not 100% tested.

DATA Polling Waveform



Hardware Chip Erase Waveform



$t_S = t_H = 5\mu s$ (min)

$t_W = 10$ ms (min)

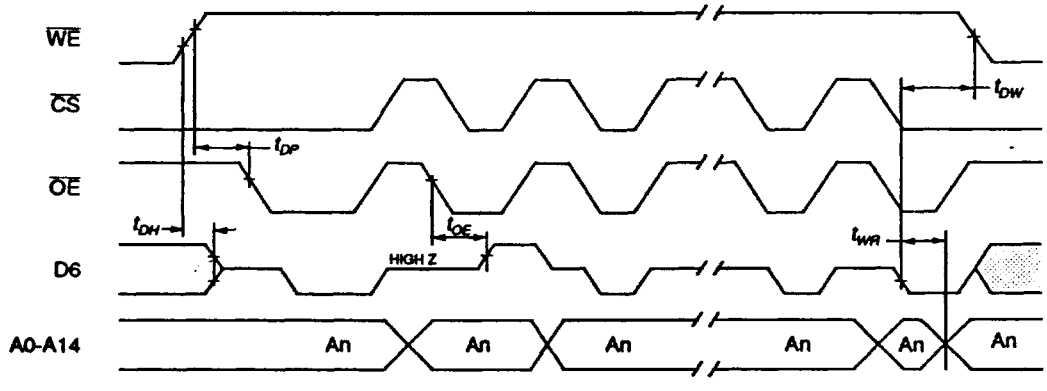
$V_H = 12V \pm 0.5V$

Toggle Bit Characteristics (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
Data Polling	t_{DP}	500	-	-	µs
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	100	ns
$\overline{OE}$ High Pulse	t_{OEH}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns
Delay to Next Write	t_{DW}	10	-	-	µs

Note : (1) These parameters are sampled and not 100% tested.

Toggle Bit Waveform



Notes : (1) Toggling either $\overline{OE}$ or $\overline{CS}$ or both $\overline{OE}$ and $\overline{CS}$ will operate toggle bit.
(2) Beginning and ending state of D6 may vary.
(3) Any address location may be used but the address should not vary.

Device Operation

Read

The MEM832 is accessed in the same way as a static RAM. A read is accomplished when both $\overline{OE}$ and $\overline{CS}$ are low. The read is then cancelled by either $\overline{CS}$ or $\overline{OE}$ returning high. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CS}$ is high.

Write

A low pulse on $\overline{WE}$ with $\overline{CS}$ low or a low pulse on $\overline{CS}$ with $\overline{WE}$ low indicates a Write Cycle. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$, and the data is latched on the first rising edge of $\overline{CS}$ or $\overline{WE}$. Once a Byte Write has begun it will automatically time itself to completion.

Page Mode Write

This mode allows 1 to 64 bytes of data to be loaded into the EEPROM, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of $\overline{WE}$ (or $\overline{CS}$) within 100µs of the same transition of the previous byte. If this 100µs time is exceeded, the load period ends and internal programming starts. A6 to A14 specify the page address (which must be valid during the above transitions) and A0 to A5 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

Hardware Chip Erase

All of the memory locations on the MEM832 can be erased in 10 ms by placing 12.0V±0.5V onto $\overline{OE}$ and controlling $\overline{WE}$ and $\overline{CS}$ to follow the Chip Erase timing characteristics. This function will operate even if the device is in Software Data Protection Mode as explained later.

DATA Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to Read the device will result in the complement of the written data appearing on D7. Once the Write Cycle is complete true data appears on the outputs and the next Write Cycle may begin.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Operating Modes

The table below shows the logic inputs required to control the operating modes of the MEM832.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*OUTPUTS*
Read	0	0	1	Data Out
Write (1)	0	1	0	Data in
Standby	1	X	X	Floating
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	Floating
Chip Erase	0	V_H	0	Floating

$1 = V_{IH}$ $0 = V_{IL}$ X = Don't care V_H = 12.0V±0.5V Note: (1) Refer to AC Programming Waveforms

Software Data Protection

The MEM832 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the MEM832 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithms

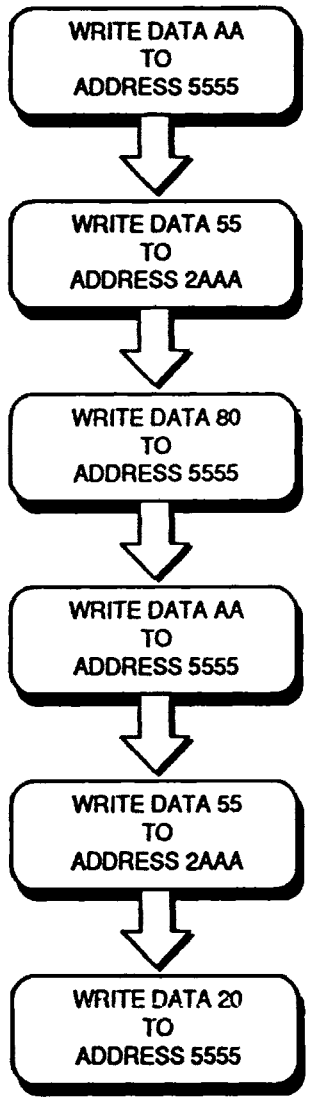
Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write from from 1 to 64 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection Algorithm

Regardless of wheather the device has been protected or not, once the software data protected aglorithm is used and the data is written, the MEM832 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and any subsequent power-up.

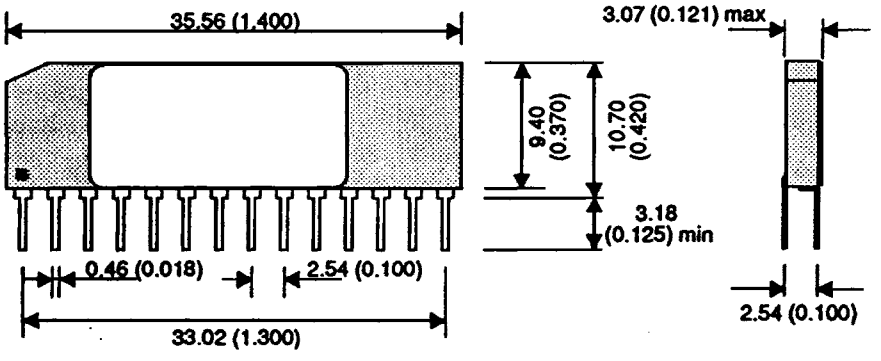
Software Data Protect Disable

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer. The following six step algorithm will reset the internal protection circuit. After t_{WC}, the MEM832 will be in standard operating mode.

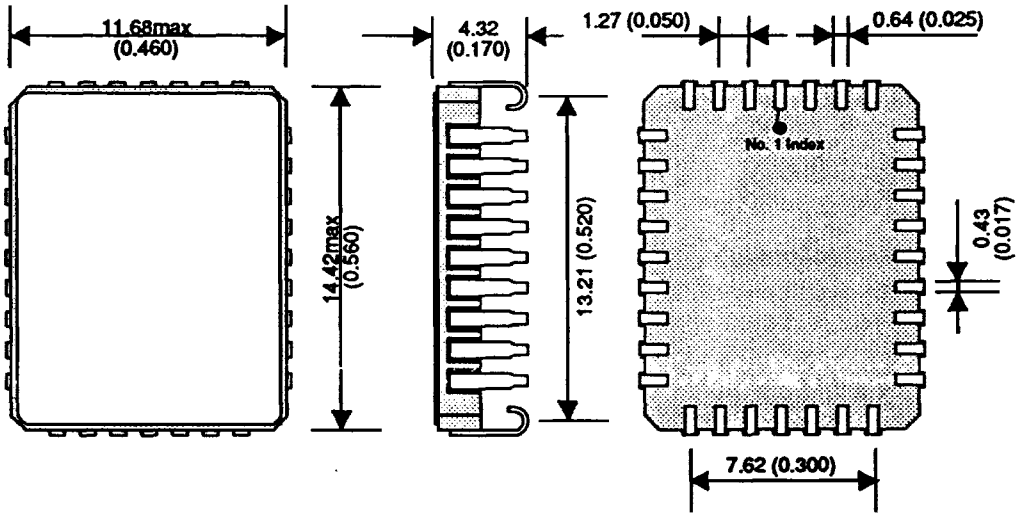


Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.010)

28 Pin 0.1" Vertical-In-Line (VIL™) - 'V' Package



32 pin Leaded Chip Carrier (JLCC) - 'J' Package



Ordering Information

MEM832VMB-90

Speed	90	= 90 ns
	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed in accordance with MIL STD 883, Method 5004, non-compliant
Packages	V	= Ceramic 0.1" VIL™
	J	= Ceramic JLCC

Note: For more information regarding screening flows contact Mosaic Semiconductor for a 'Screening Flow Applications Note.'

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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