FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-30334-1E

MEMORY
CMOS

MASK ROM CARD
PCMCIA Rel.2/JEIDA Ver.4 conformable

MB98A51121/51221/51321/51421/51521-17

MASK ROM CARD 2 M/4 M/8 M/16 M/32 M-BYTE

■ DESCRIPTION

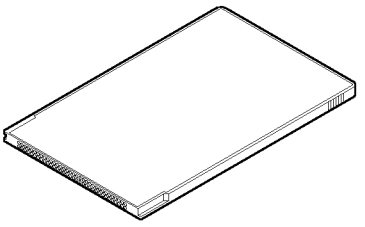
This card is a PCMCIA and JEIDA-compliant 68-pin two-piece Mask ROM card with the 16-bit mask ROM being installed on the common memory.

However, to use this card as PCMCIA Rel.2, JEIDA Ver.4, the card attribute information has to be stored in the Mask ROM.

■ FEATURES

- External dimensions: 85.6 mm × 54.0 mm × 3.3 mm
- +5 V single power supply
- Usable in 8 bits × 16 bits configuration
- Complete static operation
- I/O level TTL compatible
- Output tri-state
- Complete capacitive load without pull-up resistor or pull-down resistor except $\overline{CE}_1$ and $\overline{CE}_2$.
- 68-pin two-piece connector form

■ PACKAGE



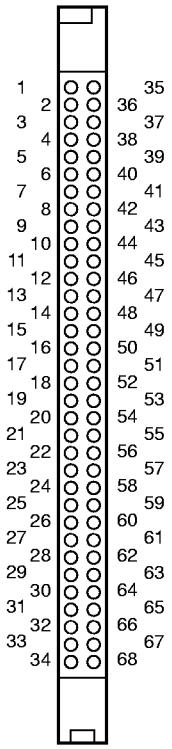
(CRD-68P-M04)

■ PRODUCT CLASS

Part Number	Memory Device	Memory Configuration (word × bit)	Access Time (ns) (max.)
MB98A51121	16-Mbit Mask ROM ×1 pcs	2 M × 8/1 M × 16	170
MB98A51221	16-Mbit Mask ROM × 2 pcs	4 M × 8/2 M × 16	
MB98A51321	16-Mbit Mask ROM × 4 pcs	8 M × 8/4 M × 16	
MB98A51421	16-Mbit Mask ROM × 8 pcs	16 M × 8/8 M × 16	
MB98A51521	16-Mbit Mask ROM × 16 pcs	32 M × 8/16 M × 16	

■ PIN ASSIGNMENTS

(CONNECTOR SIDE)



(CRD-68P-M02)

• Pin Name

Symbol	I/O	Pin Name
A_0 to A_{25}	I	Address input
D_0 to D_{15}	I/O	Data I/O
$\overline{CE_1}$, $\overline{CE_2}$	I	Card enable
$\overline{CD_1}$, $\overline{CD_2}$ *	O	Card detection
$\overline{VS_1}$, $\overline{VS_2}$	O	Voltage sense
$\overline{REG}$	I	Attribute memory space select
$\overline{OE}$	I	Output enable
$\overline{WE}$	I	Write enable
BVD1, BVD2 *	O	Battery voltage detection
WP *	O	Write protect
V_{CC}	—	Supply voltage (+5 V)
GND	—	Ground
N.C.	—	No connection

* : Those pins are internally connected; use care when handling.

Pin No.	Symbol	Pin No.	Symbol
1	GND	35	GND
2	D_3	36	$\overline{CD_1}$
3	D_4	37	D_{11}
4	D_5	38	D_{12}
5	D_6	39	D_{13}
6	D_7	40	D_{14}
7	$\overline{CE_1}$	41	D_{15}
8	A_{10}	42	$\overline{CE_2}$
9	$\overline{OE}$	43	$\overline{VS_1}$ *
10	A_{11}	44	N.C.
11	A_9	45	N.C.
12	A_8	46	A_{17}
13	A_{13}	47	A_{18}
14	A_{14}	48	A_{19} *
15	$\overline{WE}$/N.C. *	49	A_{20} *
16	N.C.	50	A_{21}/N.C. *
17	V_{CC}	51	V_{CC}
18	N.C.	52	N.C.
19	A_{16}	53	A_{22}/N.C. *
20	A_{15}	54	A_{23}/N.C. *
21	A_{12}	55	A_{24}/N.C. *
22	A_7	56	A_{25}/N.C. *
23	A_6	57	$\overline{VS_2}$ *
24	A_5	58	N.C.
25	A_4	59	N.C.
26	A_3	60	N.C.
27	A_2	61	$\overline{REG}$/N.C. *
28	A_1	62	BVD2
29	A_0	63	BVD1
30	D_0	64	D_8
31	D_1	65	D_9
32	D_2	66	D_{10}
33	WP	67	$\overline{CD_2}$
34	GND	68	GND

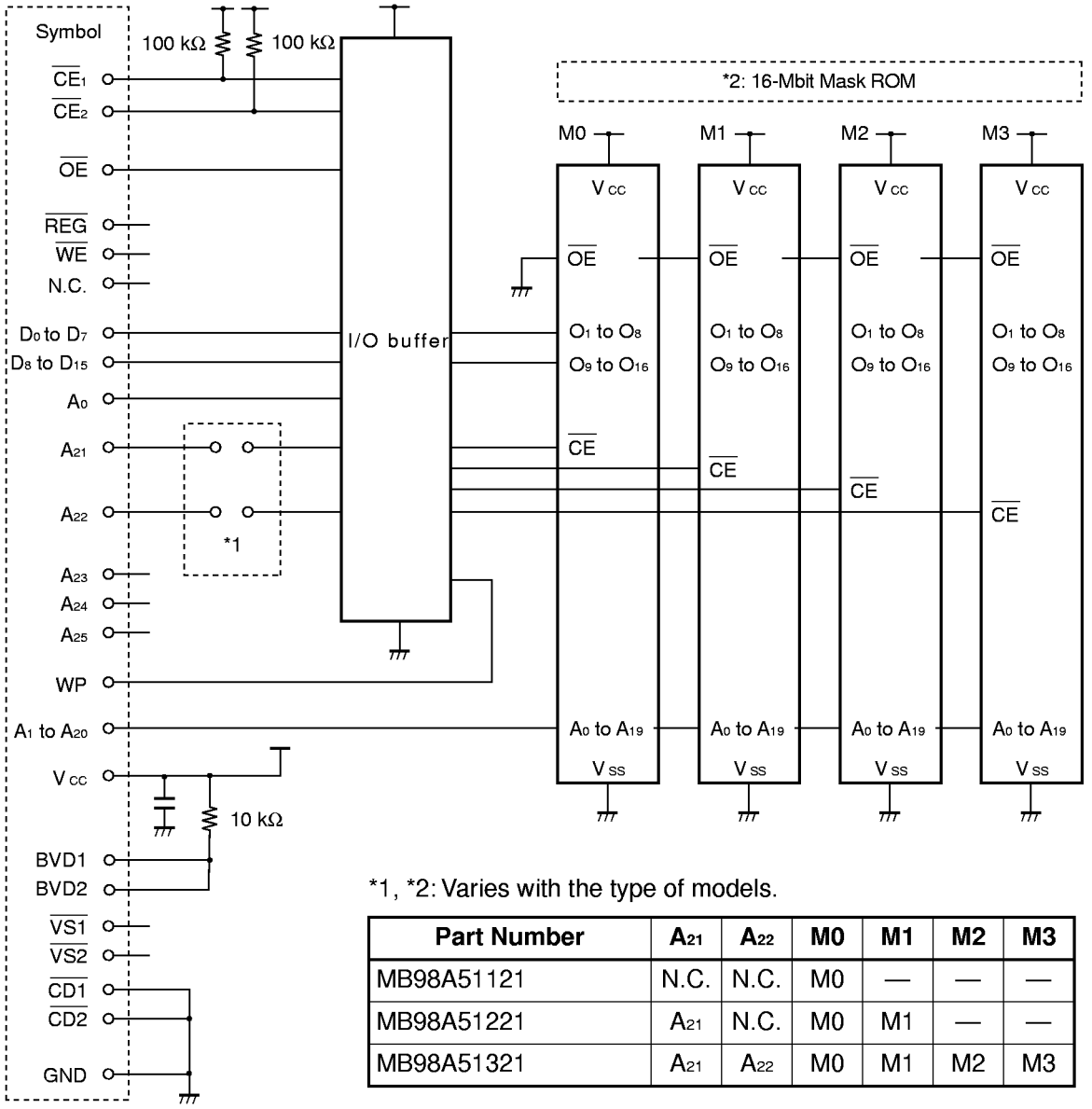
* : Whether a pin is an address pin or N.C. pin depends on the type of the models. See ■ DIFFERENCE OF PIN FUNCTIONS.

■ DIFFERENCE OF PIN FUNCTIONS

Part Name	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	$\overline{REG}$	$\overline{WE}$	$\overline{VS_1}$	$\overline{VS_2}$
MB98A51121	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
MB98A51221									
MB98A51321									
MB98A51421									
MB98A51521	A_{21}	A_{22}	A_{23}	A_{24}					

■ BLOCK DIAGRAM

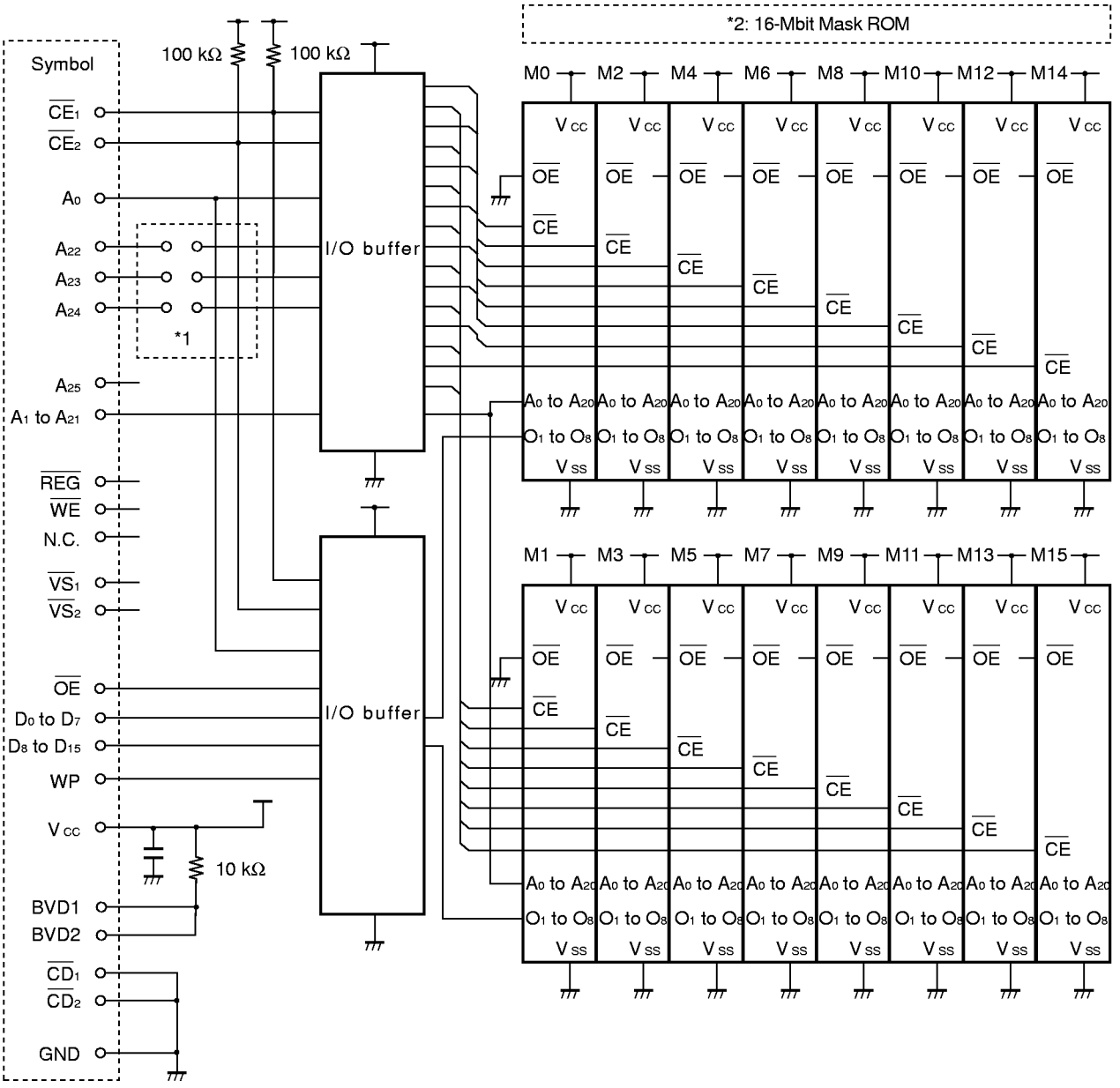
1. 16-Mbit Mask ROM × 1/× 2/× 4 Being Mounted



*1, *2: Varies with the type of models.

Part Number	A_{21}	A_{22}	M0	M1	M2	M3
MB98A51121	N.C.	N.C.	M0	—	—	—
MB98A51221	A_{21}	N.C.	M0	M1	—	—
MB98A51321	A_{21}	A_{22}	M0	M1	M2	M3

2. 16-Mbit Mask ROM × 8/× 16



*1, *2: Varies with the type of models.

Part Number	A_{22}	A_{23}	A_{24}	M0/1	M2/3	M4/5	M6/7	M8/9	M10/11	M12/13	M14/15
MB98A51421	A_{22}	A_{23}	N.C.	M0/1	M2/3	M4/5	M6/7	—	—	—	—
MB98A51521	A_{22}	A_{23}	A_{24}	M0/1	M2/3	M4/5	M6/7	M8/9	M10/11	M12/13	M14/15

■ FUNCTIONAL TRUTH TABLE

$\overline{CE_2}$	$\overline{CE_1}$	A_0 (BYTE)	$\overline{OE}$	Operating Mode	Output Pin (D_8 to D_{15})	Output Pin (D_0 to D_7)
H	H	×	×	Standby	High-impedance	High-impedance
×	×	×	H	Output disable	High-impedance	High-impedance
H	L	L	L	Read (× 8 bit)	High-impedance	Output data (even bytes)
H	L	H	L	Read (× 8 bit)	High-impedance	Output data (odd bytes)
L	H	×	L	Read (× 8 bit)	Output data (odd bytes)	High-impedance
L	L	×	L	Read (× 16 bit)	Output data (odd bytes)	Output data (even bytes)

H: High level, L: Low level, ×: Don't care

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Max.	Min.	
Supply Voltage *	V_{CC}	–0.3	+6.0	V
Input Voltage *	V_{IN}	–0.3	V_{CC} + 0.3	V
Output Voltage *	V_{OUT}	–0.3	V_{CC} + 0.3	V
Ambient Temperature	T_A	–10	+60	°C
Storage Temperature	T_{stg}	–30	+70	°C

* : The voltage values are with reference to GND = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage *	V_{CC}	4.75	5.0	5.25	V
	GND	—	0	—	V
High Level Input Voltage *	V_{IH}	2.4	—	V_{CC} + 0.3	V
Low Level Input Voltage *	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	+55	°C

* : The voltage values are with reference to the GND = 0 V.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(On the recommended conditions)

Parameter	Notes	Symbol	Test Conditions	Value			Unit
				Min.	Typ.	Max.	
Standby Supply Current		I_{SB1}	$\overline{CE_1}$, $\overline{CE_2} \geqq V_{CC}$ –0.2 V I_{OUT} = 0 mA	—	10	1600	µA
		I_{SB2}	$\overline{CE_1}$, $\overline{CE_2}$ = V_{IH} I_{OUT} = 0 mA	—	—	10	mA
Averaging Operation Supply Current		I_{CC}	Cycle = min. Duty cycle = 100% I_{OUT} = 0 mA, $\overline{OE}$ = V_{IH} V_{IN} = V_{IH} or V_{IL}	—	—	220	mA
Input Leak Current	*1	I_{LI}	V_{IN} = 0 V to V_{CC}	–40	±0.1	40	µA
Output Leak Current	*2	I_{LO}	V_{OUT} = 0 V to V_{CC}, $\overline{CE_1}$, $\overline{CE_2}$ = V_{IH} or $\overline{OE}$ = V_{IH}	–10	—	10	µA
High Level Output Voltage	*2	V_{OH}	I_{OH} = –1 mA	2.4	—	—	V
Low Level Output Voltage	*2	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V

Notes: *1. Excluding $\overline{CE_1}$ and $\overline{CE_2}$ pins.
*2. Excluding WP, BVD1, BVD2, $\overline{CD_1}$ and $\overline{CD_2}$ pins.

2. AC Characteristics

(1) Common Memory read cycle

(On the recommended conditions)

Parameter	Notes	Symbol	Test Conditions	Value		Unit
				Min.	Max.	
Read Cycle Time		t_{RC}	—	170	—	ns
Address Cycle Time		t_{ACC}	$\overline{CE_X}$ = V_{IH}, V_{IL} $\overline{OE}$ = V_{IL}	—	170	ns
Card Enable Access Time		t_{CE}	$\overline{OE}$ = V_{IL}	—	170	ns
Output Enable Access Time	*1	t_{OE}	$\overline{CE_X}$ = V_{IH}, V_{IL}	—	75	ns
Output Disable Time	*2	t_{DF}	—	—	60	ns
Output Hold Time		t_{OH}	$\overline{CE_X}$ = V_{IH}, V_{IL} $\overline{OE}$ = V_{IL}	0	—	ns

Notes: *1. The maximum delay of $\overline{OE}$ is $t_{ACC} - t_{OE}$ within the ranges in which the t_{ACC} is not affected.
*2. t_{DF} is determined by either $\overline{CE_X}$ or $\overline{OE}$, whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

3. Input/output Terminal Capacitance

(V_{IN}, V_{OUT} = GND, f = 1 MHz, T_A = +25°C)

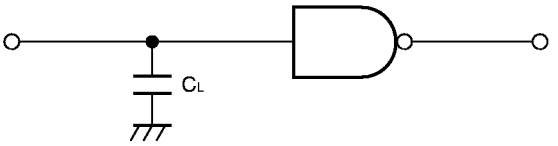
Parameter	Notes	Symbol	Value		Unit
			Min.	Max.	
Input Terminal Capacitance	*1	C_{IN}	—	75	pF
Output Terminal Capacitance	*2	$C_{I/O}$	—	50	pF

Notes: *1. Excluding $\overline{CE_1}$ and $\overline{CE_2}$ pins.
*2. Excluding WP, BVD1, BVD2, $\overline{CD_1}$, and $\overline{CD_2}$ pins.

4. AC Characteristics Test Conditions

Input voltage		: V_{IH} = 2.6 V, V_{IL} = 0.6 V
Input pulse rise time, fall time		: t_r, t_f = 5 ns (0.8 V to 2.4 V)
Timing measurement reference voltage	: Input	: V_{IH} = 2.4 V
		: V_{IL} = 0.8 V
	: Output	: V_{OH} = 2.2 V
		: V_{OL} = 0.8 V
Output load		: 1TTL + C_L (100 pF)

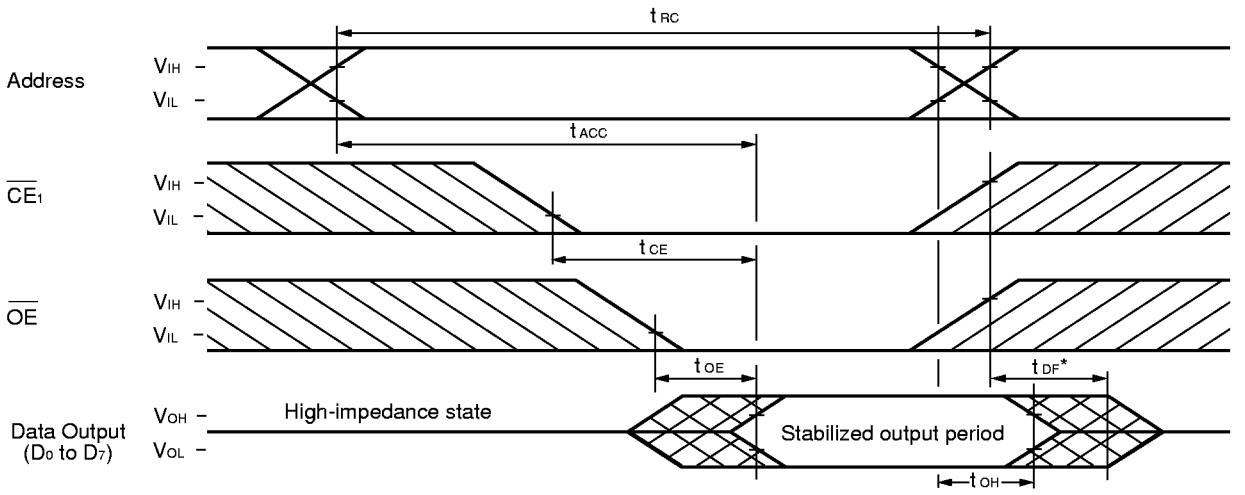
• **Output load circuit**



■ TIMING DIAGRAM

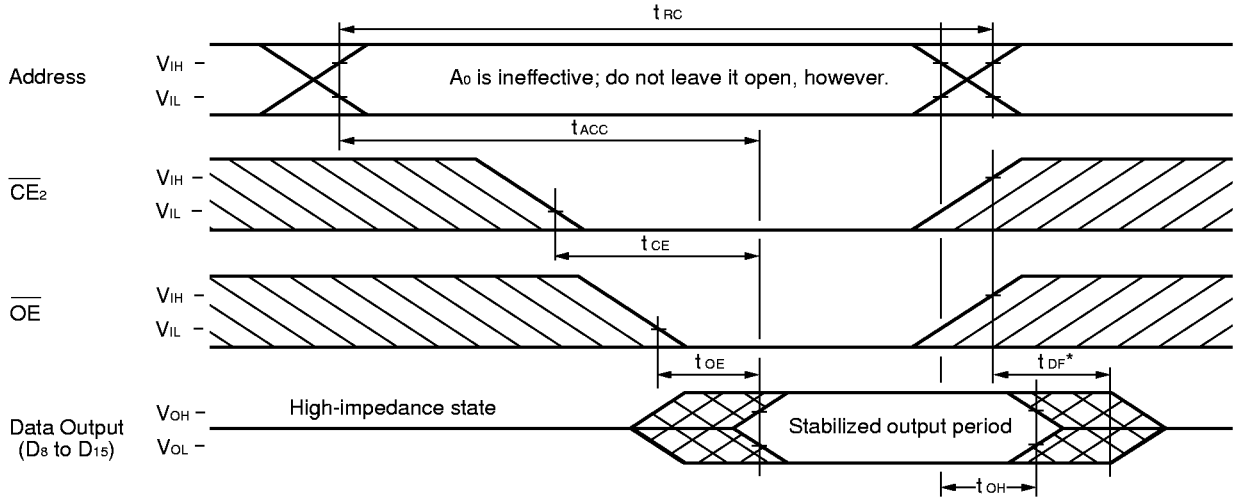
1. Common Memory Read Cycle

× 8 bit ($\overline{CE_2}$ = V_{IH})



*: t_{DF} is determined by either $\overline{OE}$ or $\overline{CE_1}$, whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

× 8 bit ($\overline{CE_1}$ = V_{IH})



*: t_{DF} is determined by either $\overline{OE}$ or $\overline{CE_2}$, whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

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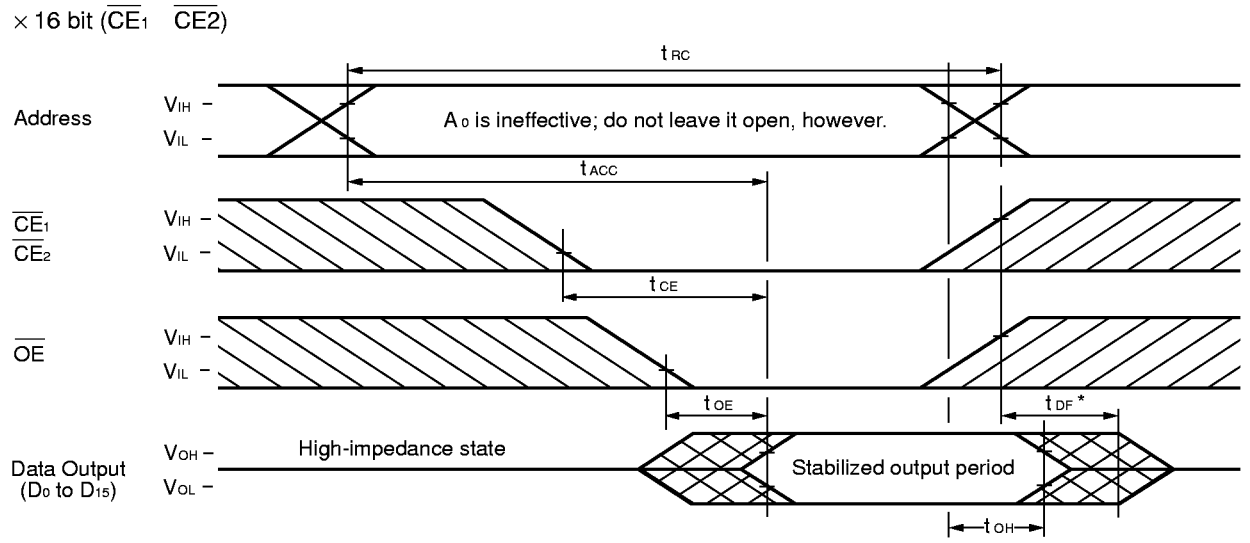


*: t_{DF} is determined by either $\overline{OE}$ or $\overline{CE_1}$ = $\overline{CE_2}$, whichever is faster with rise time.
The decision level is determined by the time the output is in a high-impedance state.

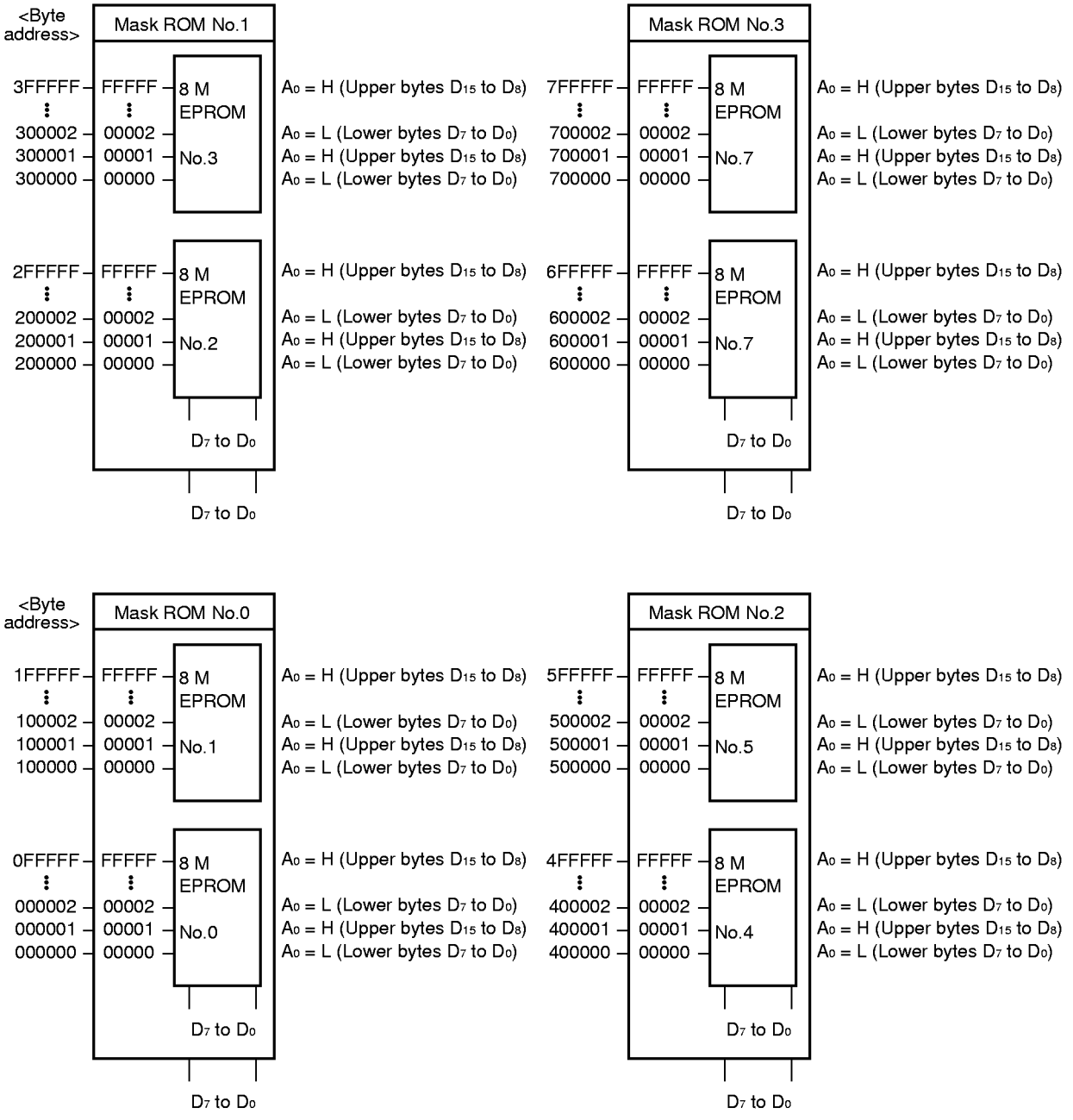
■ DATA RELEASE METHOD

Data release is accepted by the 8-Mbit EPROM (1 Mword × 8 bits).

To prevent erroneous writing of data, provide three samples per piece of data. Also indicate the card memory address for writing.

- Mapping between release data EPROM address and memory card address
  (16 Mbit Mask ROM × 1/ × 2/ × 4 being mounted)

The range of the address for the MB98A51121 is 000000 to 1FFFFF (2 Mbytes).
The range of the address for the MB98A51221 is 000000 to 3FFFFF (4 Mbytes).
The range of the address for the MB98A51321 is 000000 to 7FFFFF (8 Mbytes).



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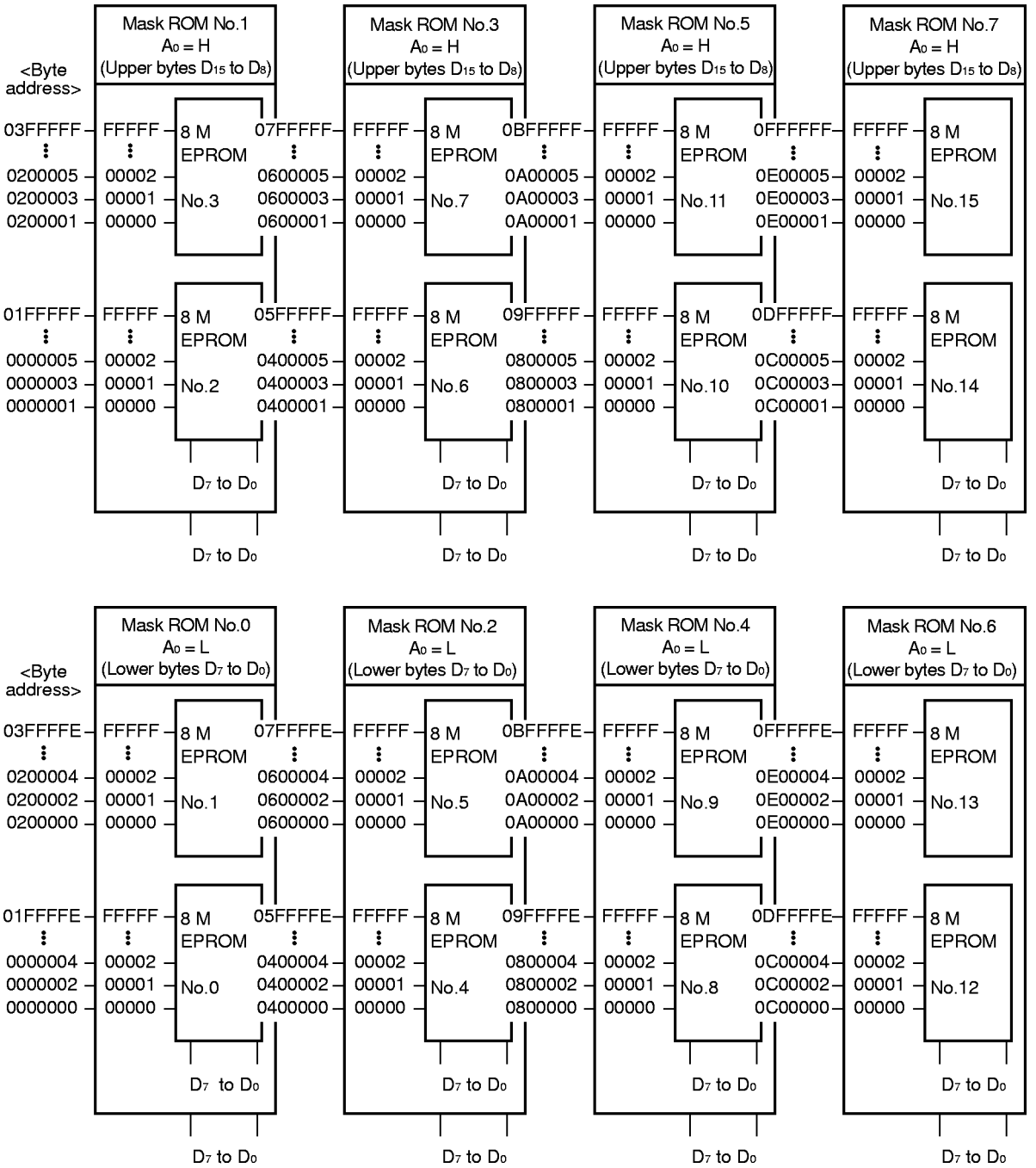
- Mapping between release data EPROM address and memory card address
  (16 Mbit Mask ROM × 8/× 16 being mounted)

The range of the address for the MB98A51421 is 000000 to FFFFFF (16 Mbytes).
The range of the address for the MB98A51521 is 0000000 to1FFFFFF (32 Mbytes)



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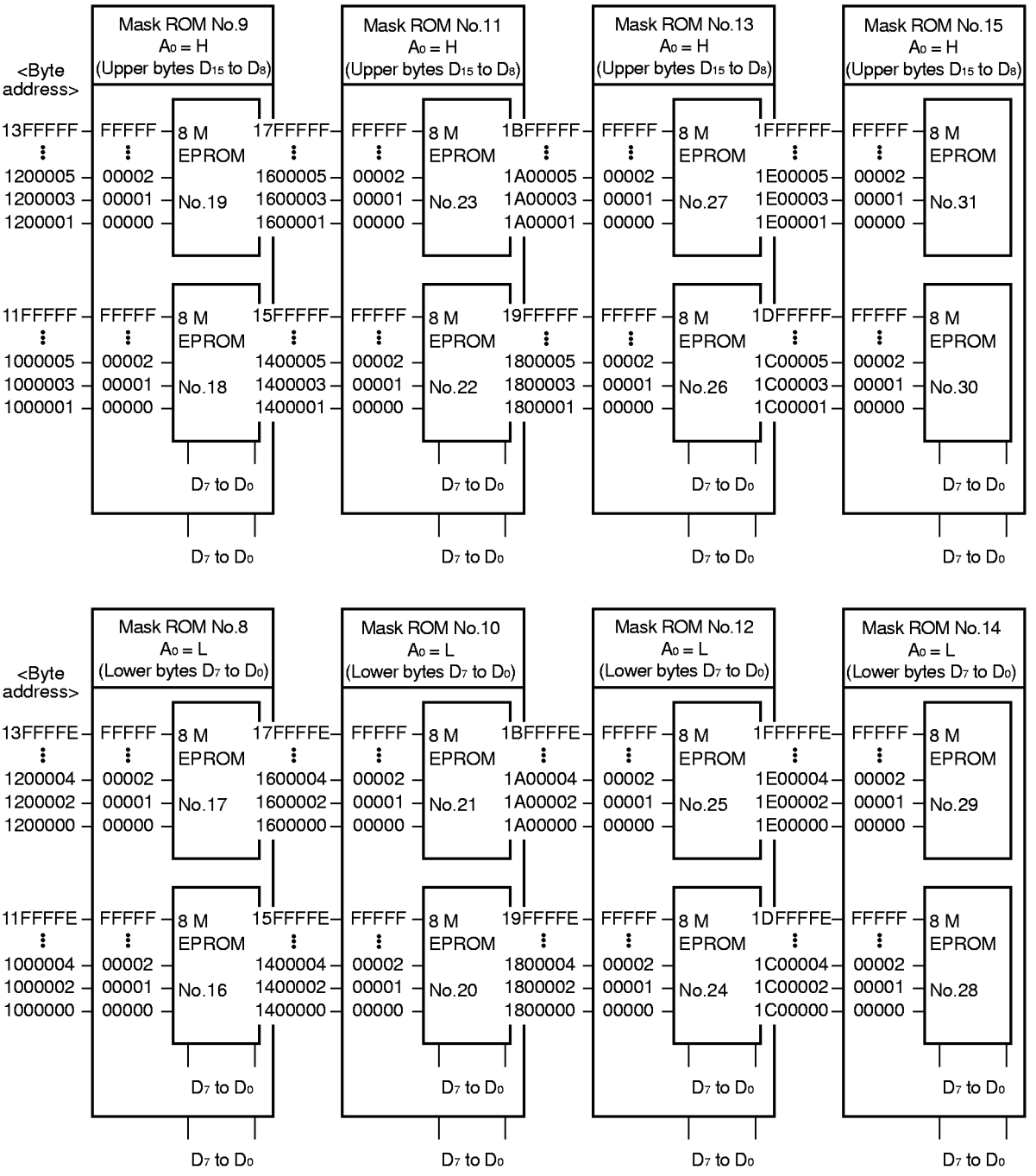
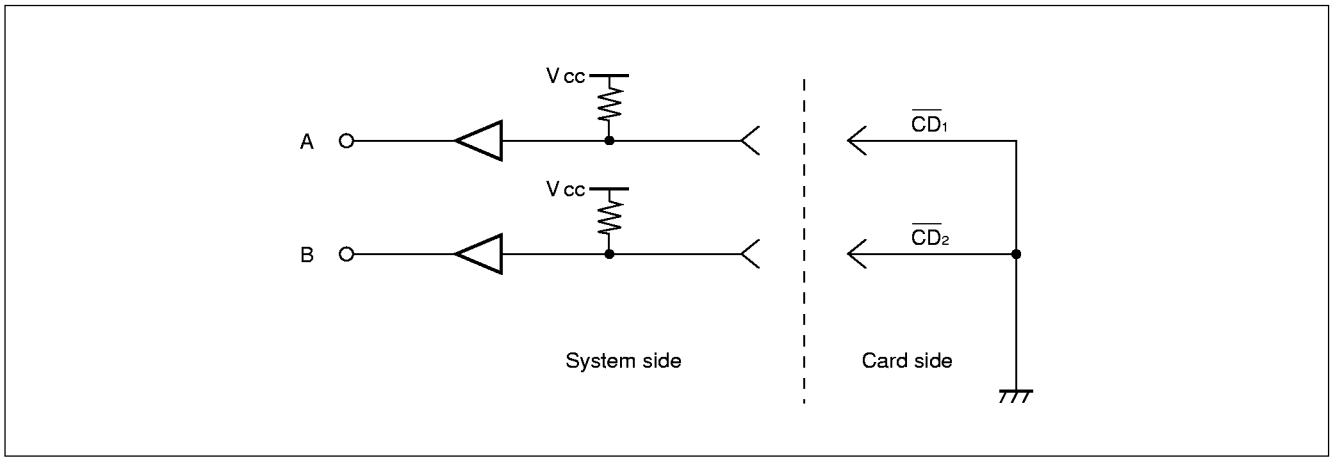

Mask ROM No.9
A0 = H
(Upper bytes D15 to D8)
Mask ROM No.11
A0 = H
(Upper bytes D15 to D8)
Mask ROM No.13
A0 = H
(Upper bytes D15 to D8)
Mask ROM No.15
A0 = H
(Upper bytes D15 to D8)
<Byte address>
13FFFFF
11FFFFF
1200005
1200003
1200001
1000005
1000003
1000001
FFFFF
00002
00001
00000
8 M EPROM
No.19
No.18
No.23
No.22
No.27
No.26
No.31
No.30
17FFFFF
15FFFFF
1600005
1600003
1600001
1400005
1400003
1400001
1BFFFFF
19FFFFF
1A00005
1A00003
1A00001
1800005
1800003
1800001
1FFFFFF
1DFFFFF
1E00005
1E00003
1E00001
1C00005
1C00003
1C00001
D7 to D0
Mask ROM No.8
A0 = L
(Lower bytes D7 to D0)
Mask ROM No.10
A0 = L
(Lower bytes D7 to D0)
Mask ROM No.12
A0 = L
(Lower bytes D7 to D0)
Mask ROM No.14
A0 = L
(Lower bytes D7 to D0)
13FFFFE
11FFFFE
1200004
1200002
1200000
1000004
1000002
1000000
No.17
No.16
No.21
No.20
No.25
No.24
No.29
No.28
17FFFFE
15FFFFE
1600004
1600002
1600000
1400004
1400002
1400000
1BFFFFE
19FFFFE
1A00004
1A00002
1A00000
1800004
1800002
1800000
1FFFFFE
1DFFFFE
1E00004
1E00002
1E00000
1C00004
1C00002
1C00000

■ AUXILIARY CAPABILITIES

1. Card Detection Pins ($\overline{CD}_1$, $\overline{CD}_2$)

These pins verify a card is correctly inserted into the system.

The two pins are internally connected to the ground; with the system side connection being pulled up to the V_{CC}, detection of the voltage of these pins allows the system to check the state of connectivity of a card (See the diagram below).



2. Write Protection Pin (WP)

The Mask ROM Card, whose common memory is write-protected, outputs a high-level write-protection signal.

■ DEVICE HANDLING PRECAUTIONS

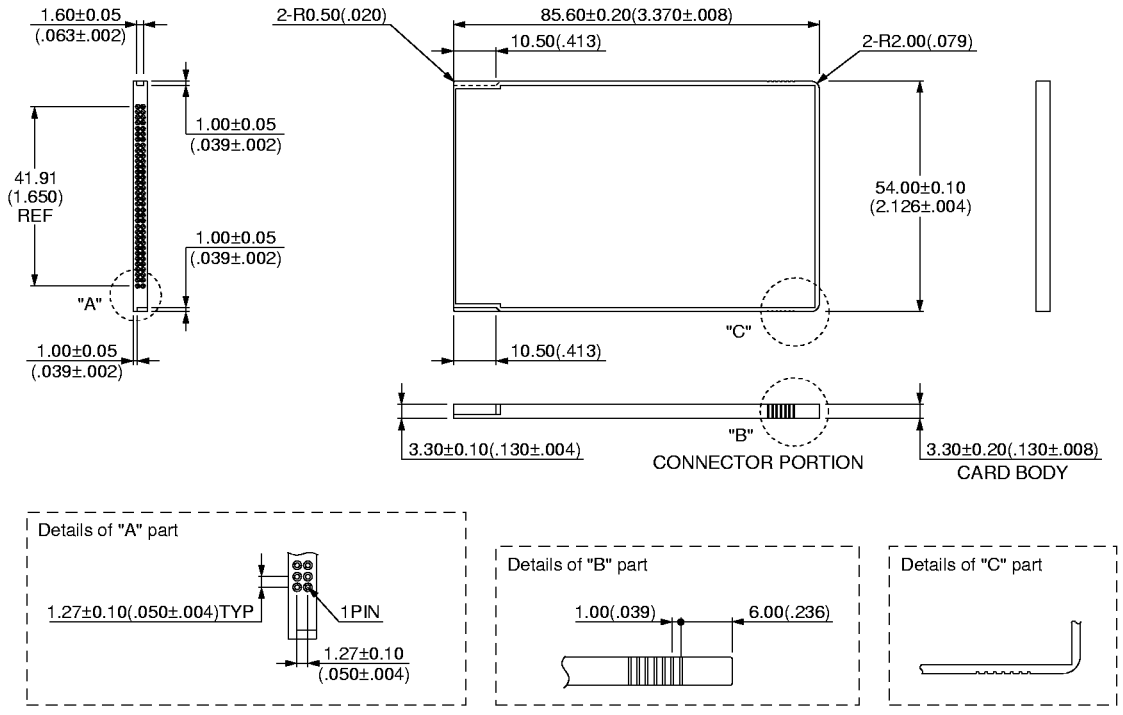
The device in composed of fine electronic parts, so take care in handling or keeping it as below.

- The card is made fine, so do not keep it in the high temperature nor high humiditly, place line in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

■ PACKAGE DIMENSIONS

68-pin Memory Card
(CRD-68P-M02)

Note: Dimensions conform with PCMCIA/JEIDA



Dimensions in mm (inches)