MX23L12810

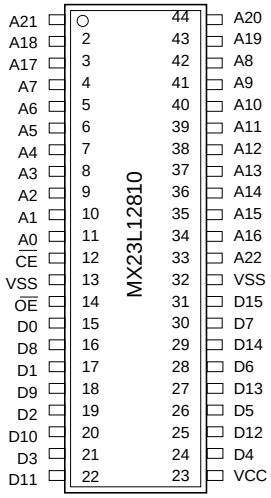
128M-BIT (8M x 16) MASK ROM (SOP ONLY)

FEATURES

- Bit organization
  - 8M x 16 (word mode)
- Fast access time
  - Random access: 90ns (max.)
- Current
  - Operating:50mA
  - Standby:15uA
- Supply voltage
  - 3.0~3.6V
- Package
  - 44 pin SOP (500mil)
- Temperature
  - 0 ~ 70℃

PIN CONFIGURATION

44 SOP(For Word Mode Only)



PIN DESCRIPTION

Symbol	Pin Function
A0~A22	Address Inputs
D0~D15	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

ORDER INFORMATION

Part No.	Access Time	Package
MX23L12810MC-90	90ns	44 pin SOP
MX23L12810MC-10	100ns	44 pin SOP
MX23L12810MC-12	120ns	44 pin SOP
MX23L12810MC-13	130ns	44 pin SOP
MX23L12810MC-15	150ns	44 pin SOP

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Supply Voltage Relative to VSS	VCC	-0.3V to 4.3V
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC + 2V (Note)
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	50mA	f=5MHz, all outputs open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	15uA	$\overline{CE}$>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

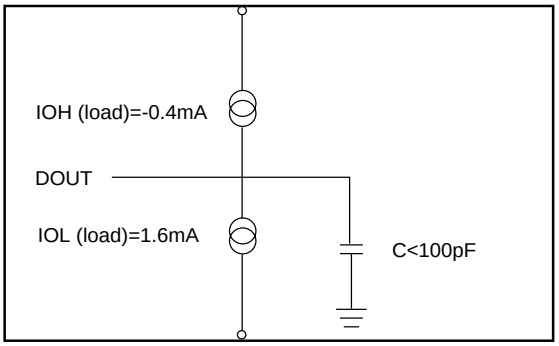
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.0V~3.6V)

Item	Symbol	23L12810-90		23L12810-10		23L12810-12		23L12810-13		23L12810-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	90ns	-	100ns	-	120ns	-	130ns	-	150ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns	-	130ns	-	150ns
Chip Enable Access Time	tACE	-	90ns	-	100ns	-	120ns	-	130ns	-	150ns
Output Enable Time	tOE	-	25ns	-	30ns	-	50ns	-	50ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

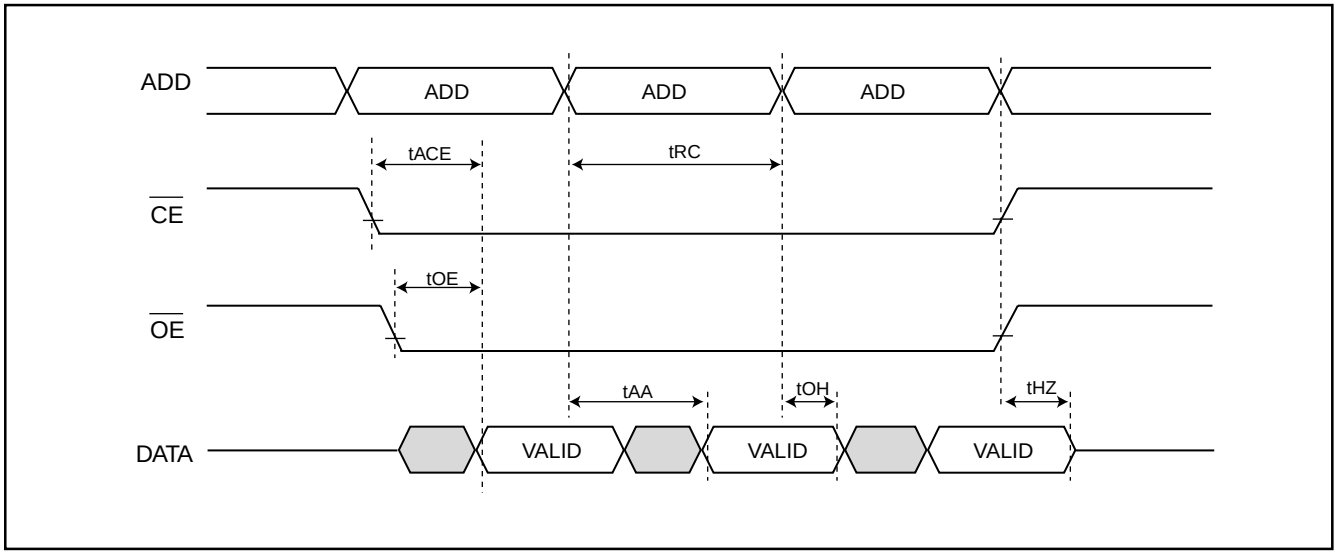
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note: No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

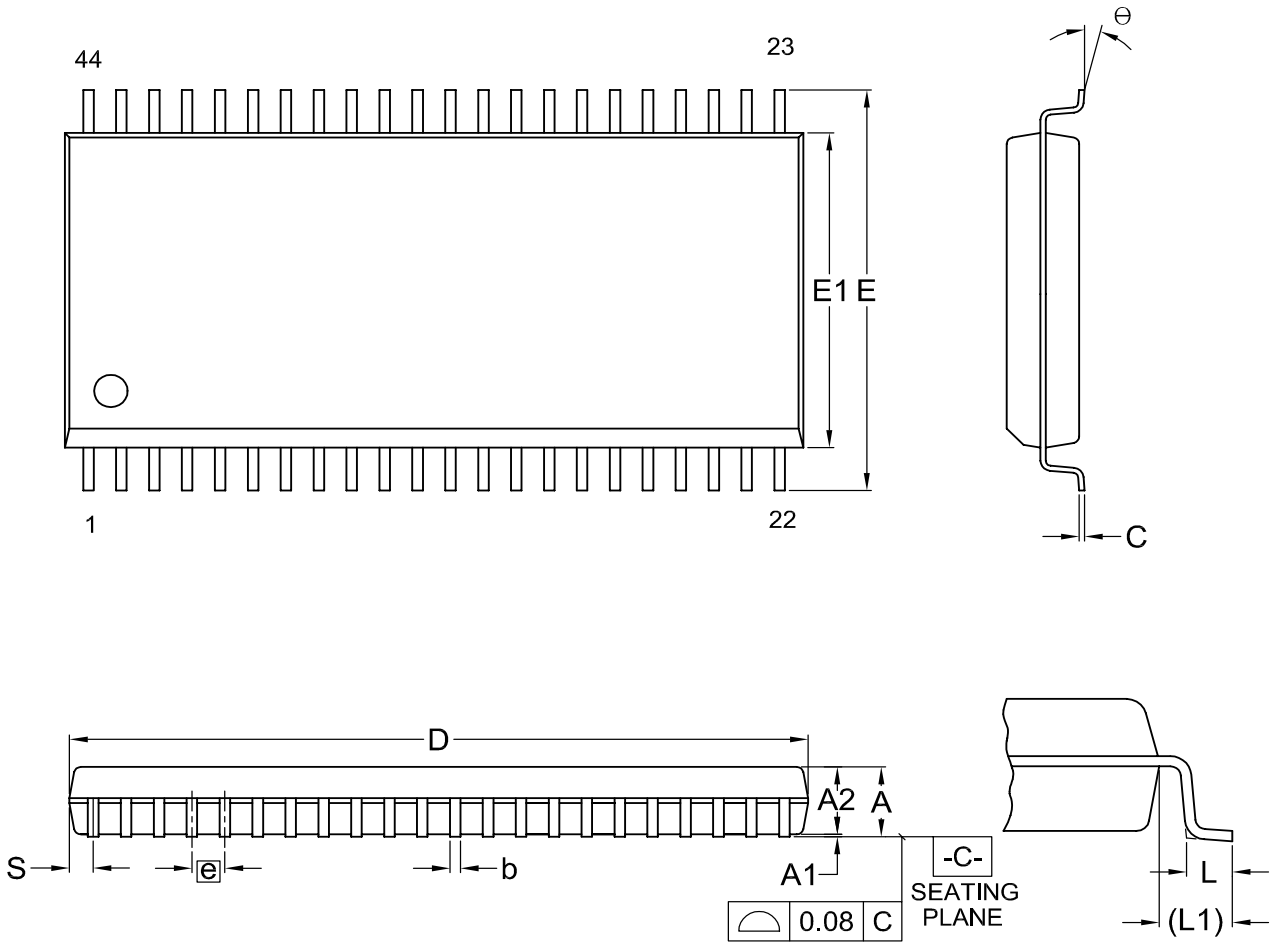
TIMING DIAGRAM

RANDOM READ



PACKAGE INFORMATION

Title: Package Outline for SOP 44L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	5	MO-175			09-24-'02

REVISION HISTORY

Revision #	Description	Page	Date
1.1	Modify Current Operating:60mA-->40mA	P1	DEC/12/2000
	Modify ICC1:60mA-->40mA, f=5MHz, all outputs open	P2	
	Del ICC2	P2	
1.2	Modify Current Operating:40mA-->50mA	P1	DEC/14/2000
	Modify ICC1:40mA-->50mA	P2	
1.3	Add Access Time:90/100/120ns	P1,2	AUG/28/2001
	Add Temperature:0~70℃	P1	
	Modify Supply voltage:3.4V±0.2-->3.0V~3.6V	P1,2	
1.4	Modify Package Information	P4	FEB/01/2002
1.5	1. Add supply voltage relative to VSS	P2	JUL/19/2002
	2. Change voltage on any pin relative to VSS:-0.5V to VCC+2.0	P2	
1.6	1. To modify Package Information	P4	NOV/20/2002
1.7	1. Added notes in Absolute Maximum ratings	P2	DEC/03/2002
1.8	1. Modify VIN: -0.5V to VCC + 2V --> -1.3V to VCC + 2V (Note)	P2	DEC/10/2002

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