DESCRIPTION

The 82S82 binary coded (BCD) arithmetic unit is a high speed Schottky MSI circuit with lookahead carry/$\overline{\text{borrow}}$ that has been designed for easy systems usage. Depending on the state of the $\overline{\text{add}}$/subtract control line, the unit produces the BCD sum or difference of two decimal numbers presented to the BCD inputs in the 8-4-2-1 weighted BCD format. A comparison output (A=B) is provided as well. When in the subtract mode, this output indicates if two BCD numbers are equal and its open collector feature allows easy comparison of several decades.

The 82S82 BCD arithmetic unit has been designed such that input and output logic levels including the carry/$\overline{\text{borrow}}$ are in their true logic form. Compared to multichip hardware solutions previously at the designer's disposal, the 82S82 arithmetic unit generates the BCD carry/$\overline{\text{borrow}}$ terms internally in the look-ahead mode and does BCD arithmetic directly. For more than one BCD decade the carry/$\overline{\text{borrow}}$ term may ripple between 82S82's. For ultra fast BCD arithmetic operations the Signetics 74182 fast-carry extender may be used together with the 82S82's. The 74182 suitably combines the 82S82's active LOW carry generate ($\overline{\text{CgOUT}}$) and carry propagate ($\overline{\text{CpOUT}}$) terms for complete look-ahead carry between decades.

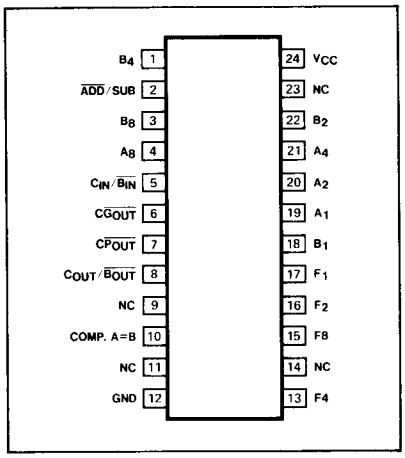
When the $\overline{\text{ADD}}$/SUBTRACT control input is LOW, BCD addition is performed (A + B + CIN = F). Input codes above 9 to either the A_N or B_N inputs are not defined to give valid output sums except for the special case of binary to BCD conversion. In the normal BCD addition mode the F outputs show true BCD results and an active HIGH carryout signal results for sums greater than 9.

For subtraction the $\overline{\text{ADD}}$/SUBTRACT control input be HIGH. Internally subtraction is performed by 9's complement addition yielding the difference (A − B − 1 = F) of two BCD numbers when the CIN/$\overline{\text{BIN}}$ input is LOW. If the CIN/$\overline{\text{BIN}}$ is HIGH during subtraction, the absence of a borrow in signal gives A − F = F. For A≥B the BCD difference is available at the F outputs in its true form. If A<B, the 10's complement of the correct answer appears at the F outputs with CIN/$\overline{\text{BIN}}$ HIGH or if CIN/$\overline{\text{BIN}}$ is LOW the 9's complement results. As long as A<B an active LOW borrow is also generated.

The 82S82 BCD arithmetric unit is also useful for binary to BCD conversion. By summing B = 0 with binary inputs 0≤A≤15, where A is the number being converted, a true BCD output results. A carry is generated to the next decade for A>9.

The function table for the 82S82 summarizes the device operation. In those applications where only BCD addition is required, the Signetics 82S82 BCD adder should be considered.

PIN CONFIGURATION



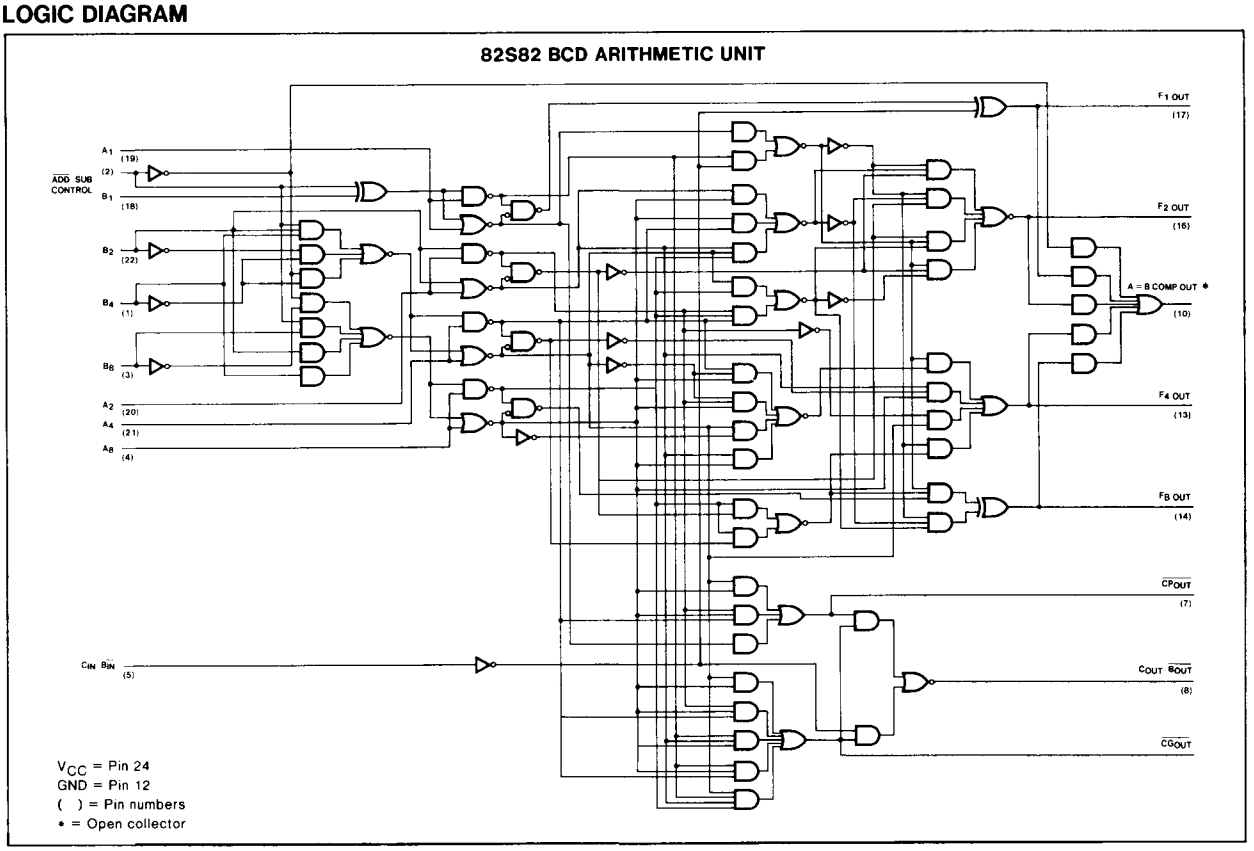
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +75°C	MILITARY RANGES V_{CC}=5V±5%; T_A=−55°C to +125°C
Plastic DIP	N82S82N	
Ceramic DIP	N82S82F	
Flatpak		

FUNCTION TABLE

FUNCTION	$\overline{ADD}$/SUB	A(A_8,A_4,A_2,A_1)	B(B_8,B_4,B_2,B_1)	$C_{in}/\overline{B_{in}}$	F(F_8,F_4,F_2,F_1)	$C_{out}/\overline{B_{out}}$	COMPARE (A = B)
Add	L	BCD Augend	BCD Addend	H = Carry L = No Carry	IF C_{in} = H F = A + B + 1 IF C_{in} = L F = A + B	F≤9 $C_{OUT}/\overline{B_{OUT}}$ = L F>9 $C_{OUT}/\overline{B_{OUT}}$ = H	X
Subtract	H	BCD Minuend	BCD Subtrahend	L = Borrow H = No Borrow	IF B_{in} = L F = A − B − 1 IF B_{in} = H F = A − B	A>B $C_{OUT}/\overline{B_{OUT}}$ = H A≤B $C_{OUT}/\overline{B_{OUT}}$ = L A<B $C_{OUT}/\overline{B_{OUT}}$ = L A≥B $C_{OUT}/\overline{B_{OUT}}$ = H	X
Compare	H	BCD Word A	BCD Word B	H	A − B	A<B $C_{OUT}/\overline{B_{OUT}}$ = L A>B $C_{OUT}/\overline{B_{OUT}}$ = H	If A = B Compare = H If A≠B Compare = L
Binary to BCD Conversion	L	0≤A≤15	B = 0	X	BCD	A≤9 C_{OUT} = L A>9 C_{OUT} = H	X

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

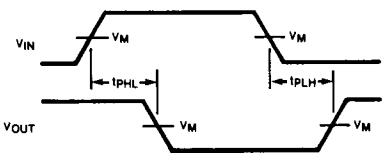
	PARAMETER	TEST CONDITIONS	82S82 Min	82S82 Max	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = 4.75V, I_{OH} = −1mA	2.6		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 16mA		0.5	V
I_{OH}	Output HIGH current	V_{CC} = 4.75V, V_{OUT} = 5.5V		250	μA
I_{IH}	Input HIGH current A_N,B_1,$\overline{B_8}$,$C_{IN}/\overline{B_{IN}}$ B_2,B_4,$\overline{Add}$/Sub	V_{CC} = 4.75V, V_{IN} = 4.75V		 10 20	 μA μA
I_{IL}	Input LOW current A_N,B_1,$\overline{B_8}$,$C_{IN}/\overline{B_{IN}}$ B_2,B_4,$\overline{Add}$/Sub	V_{CC} = 5.25V, V_{IN} = 0.5V		 −400 −800	 μA μA
V_{CD}	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = −18mA		−1.2	V
I_{OS}	Output short circuit current	V_{CC} = 5.25V, V_{OUT} = OV	−20	−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V		122	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

	PARAMETER	TEST CONDITIONS	82S82 C_L = 15pF R_L = 280Ω Min	82S82 C_L = 15pF R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Any A_N,B_N,$C_{IN}/\overline{B_{IN}}$ to F_N	Figures 1 & 2		35 35	ns ns
t_{PLH} t_{PHL}	Propagation delay Any A_N to $C_{OUT}/\overline{B_{OUT}}$	Figures 1 & 2		40 35	ns ns
t_{PLH} t_{PHL}	Propagation delay Any B_N to $C_{OUT}/\overline{B_{OUT}}$	Figures 1 & 2		45 35	ns ns
t_{PLH} t_{PHL}	Propagation delay $C_{IN}/\overline{B_{IN}}$ to $C_{OUT}/\overline{B_{OUT}}$	Figure 2		25 15	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Add}$/Sub to F_N	Figures 1 & 2		35 35	ns ns
t_{PLH} t_{PHL}	Propagation delay A_N,B_N to $\overline{CP_{OUT}}$	Figures 1 & 2		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay A_N,B_N to $\overline{CG_{OUT}}$	Figures 1 & 2		25 32	ns ns
t_{PLH} t_{PHL}	Propagation delay A_N,B_N to $(A=B)_{OUT}$	Figures 1 & 2		50 50	ns ns

AC WAVEFORMS

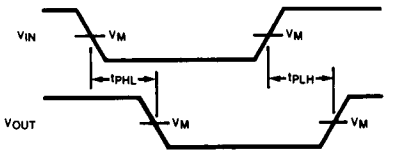
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.5V.

Figure 1

WAVEFORM FOR NON-INVERTING OUTPUTS

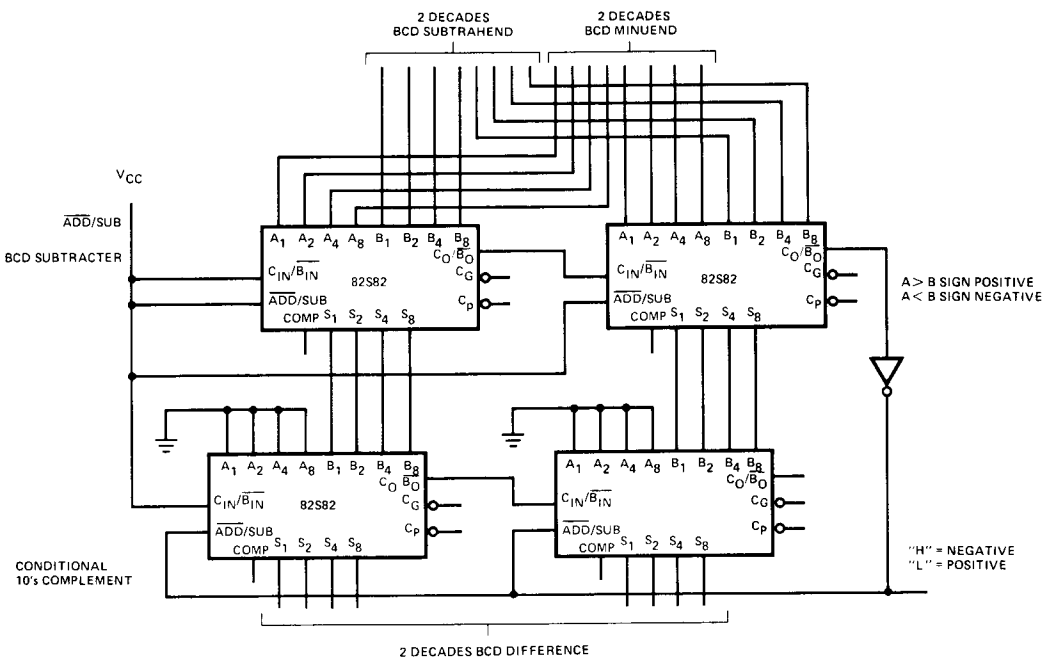


V_M = 1.5V.

Figure 2

TYPICAL APPLICATIONS

SIGN AND MAGNITUDE GENERATION FOR (A–B)



TRUTH TABLE FOR BINARY TO BCD CONVERSION

($10 \leq A_N \leq 15$, $B_N = 0$)										
$\overline{Add}/Sub$	$C_{IN}/\overline{B_{IN}}$	A_8	A_4	A_2	A_1	S_8	S_4	S_2	S_1	$C_{OUT}/\overline{B_{OUT}}$
L	L	H	L	H	L	H	L	L	L	H
L	L	H	L	H	H	H	L	L	H	H
L	L	H	H	L	L	H	L	H	L	H
L	L	H	H	L	H	H	L	H	H	H
L	L	H	H	H	L	H	H	L	L	H
L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	L	H	L	L	H	H
L	H	H	L	H	H	H	L	H	L	H
L	H	H	H	L	L	H	L	H	H	H
L	H	H	H	L	H	H	H	L	L	H
L	H	H	H	H	L	H	H	L	H	H
L	H	H	H	H	H	H	H	H	L	H

BINARY TO BCD CONVERSION