8-bit Data Bus One-Time PROM Card

Connector Type

Two-piece 60-pin

MF4128-F3DAPXX
MF4256-F3DAPXX
MF4512-F3DAPXX
MF41M0-F1EAPXX
MF42M0-F1EAPXX

DESCRIPTION

Mitsubishi's One-Time PROM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm × 54mm × 3.4mm). The cards use an 8-bit data bus.
Available in 128K, 256K, 512K, 1 M and 2 M byte capacities, Mitsubishi's One-Time PROM cards are available with either a 60 pin, two-piece connector.

- Buffered interface
- 60-pin connector
- 8-bit data width

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.
- Electrostatic discharge protection to 25kV

APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

PRODUCT LIST

Item / Type name	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF4128-F3DAPXX	128KB	8	200	Two-piece	60	60P-001
MF4256-F3DAPXX	256KB					
MF4512-F3DAPXX	512KB					
MF41M0-F1EAPXX	1MB		250			
MF42M0-F1EAPXX	2MB					

MITSUBISHI ELECTRIC

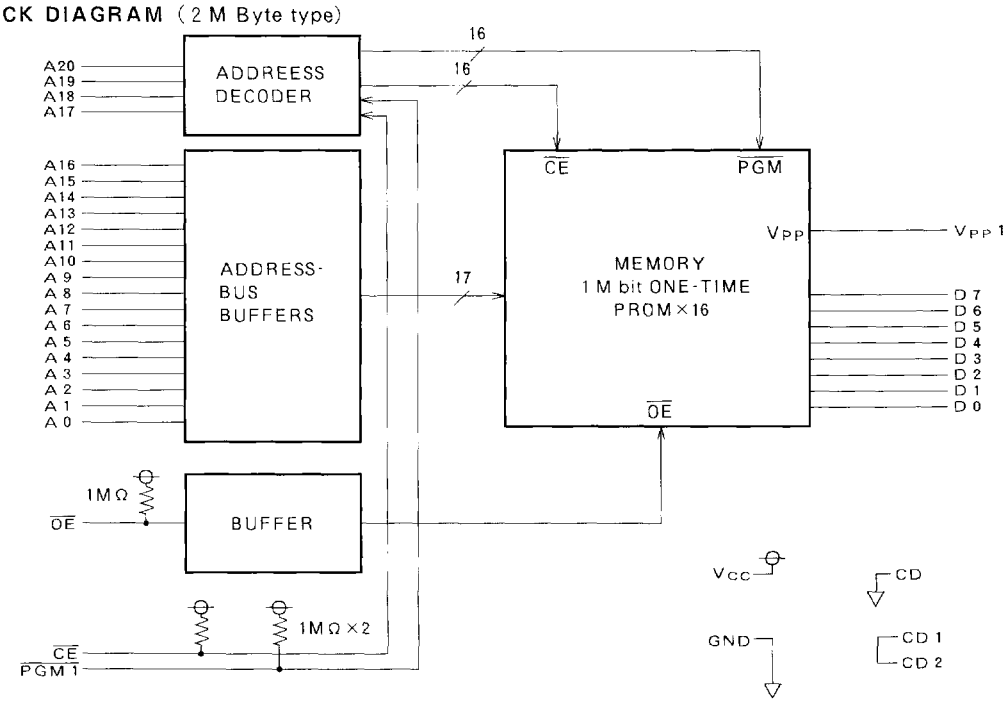
PIN ASSIGNMENT

Two-Piece Type (60-pin)

Pin No.	Symbol	Function
1	NC	No connection
3	V_{PP} 1	Power supply
5	A12	Address input
7	A 7	
9	A 6	
11	A 5	
13	A 4	
15	A 3	
17	A 2	
19	A 1	
21	A 0	
23	D 0	Data I/O
25	D 1	
27	D 2	
29	GND	Ground
31	D 3	Data I/O
33	D 4	
35	D 5	
37	D 6	
39	D 7	
41	$\overline{CE}$	Card enable
43	A10	Address input
45	$\overline{OE}$	Output enable
47	A11	Address input
49	A 9	
51	A 8	
53	A13	
55	A14	
57	$\overline{PGM1}$	Program control
59	V_{CC}	Power supply

Pin No.	Symbol	Function
2	NC	No connection
4	NC	
6	CD 1	Card detect 1
8	A15	Address input
10	A16	
12	A17	NC for ≤128KB types
14	A18	NC for ≤256KB types
16	A19	NC for ≤512KB types
18	A20	NC for ≤ 1 MB types
20	NC	No connection
22	NC	
24	NC	
26	NC	
28	NC	
30	GND	Ground
32	GND	
34	NC	No connection
36	NC	
38	NC	
40	NC	
42	NC	
44	NC	
46	NC	
48	NC	
50	NC	
52	B 0	GND
54	B 1	No connection
56	B 2	GND
58	CD 2	Card detect 2
60	V_{CC}	Power supply

BLOCK DIAGRAM (2 M Byte type)



FUNCTION TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM1}$	V_{PP} (typ.)	V_{CC} (typ.)	I/O	I_{CC}
Standby	H	X	X	5 V	5 V	High-impedance	Standby
Read	L	L	X	5 V	5 V	Data out	Active
Output disable	L	H	X	5 V	5 V	High-impedance	Active
Byte program	L	H	L	12.5V	6 V	Data in	Active
Program verify	L	L	H	12.5V	6 V	Data out	Active
Page data latch	H	L	H	12.5V	6 V	Data in	Active
Page program	H	H	L	12.5V	6 V	High-impedance	Active
Program inhibit	X	L	L	12.5V	6 V	High-impedance	Active
	X	H	H	12.5V	6 V	High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5~7.0	V
V_{PP}	Supply voltage		−0.5~14.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5 (7.0Max.)	V
V_O	Output voltage		0~V_{CC}	V
T_{opr}	Operating temperature		0~70	℃
T_{stg}1	Storage temperature 1		−40~80	℃

READ OPERATION

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~50℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} supply voltage		V_{CC}		V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~50℃, V_{CC} = V_{PP} = 4.75~5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH} = −400 μA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2.1mA				0.45	V
I_{IH}	High input current	V_I = V_{CC} V				10	μA
I_{IL}	Low input current	V_I = 0 V	PGM $\overline{OE}$ $\overline{CE}$			−20	μA
			Other inputs			−10	
I_{OZH}	High output current in off state	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_o = V_{CC} V				10	μA
I_{OZL}	Low output current in off state	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_o = 0 V				−10	μA
$I_{CC}1 \cdot 1$	Standby V_{CC} supply current	$\overline{CE}$ = V_{IH}, Outputs = open, Other inputs = V_{IH} or V_{IL}	128K			40	mA
			256K			50	
			512K			55	
			1 M			65	
			2 M			85	
$I_{CC}1 \cdot 2$	Standby V_{CC} supply current	$\overline{CE}$ ≧ V_{CC} − 0.2V, Output = open, Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V	128K			5	mA
			256K				
			512K				
			1 M				
			2 M				
$I_{CC}2 \cdot 1$	Active VCC supply current (Minimum cycle)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Outputs = open, Other inputs = V_{IH} or V_{IL}	128K			145	mA
			256K			150	
			512K			165	
			1 M			160	
			2 M			190	
$I_{CC}2 \cdot 2$	Active VCC supply current (Minimum cycle)	$\overline{CE}$ = $\overline{OE}$ ≦ 0.2V, Outputs = open, Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V	128K			110	mA
			256K			110	
			512K			115	
			1 M			110	
			2 M			120	
$I_{PP}1$	V_{PP} supply current		128K			0.1	mA
			256K			0.2	
			512K			0.4	
			1 M			2.0	
			2 M			4.0	

Note 1 : Direction for current flowing into IC is indicated as positive (no mark).

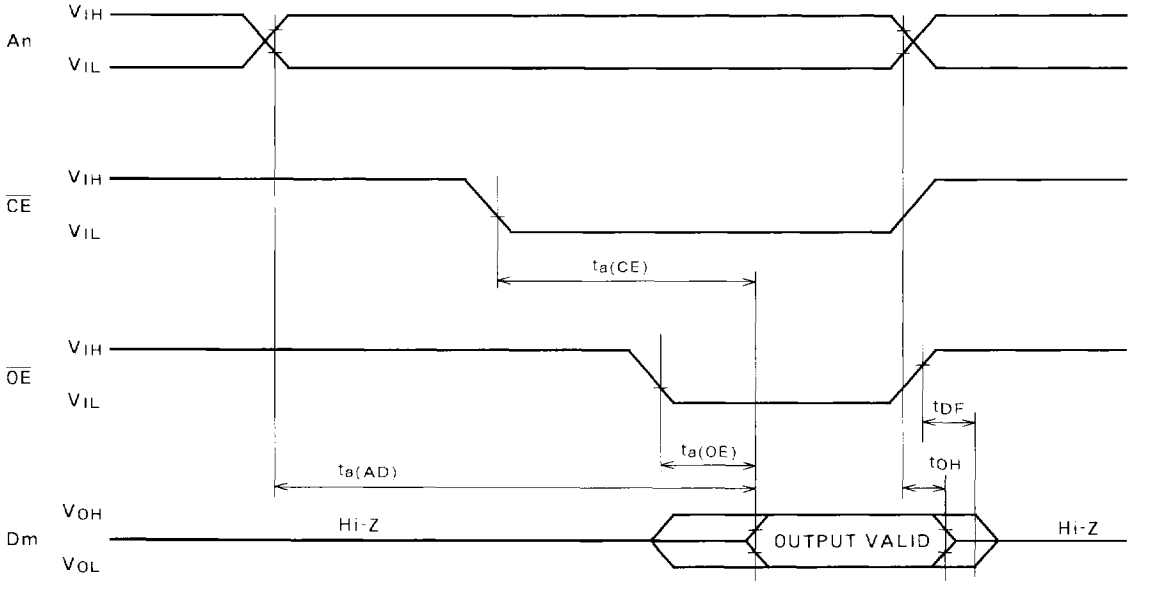
SWITCHING CHARACTERISTICS

Read Cycle (T_a = 0 ~ 50℃, $V_{CC} = V_{PP}$ = 4.75 ~ 5.25V, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
$t_{a(AD)}$	Address access time	$\overline{CE} = \overline{OE} = V_{IL}$	1M, 2M			250	ns
			others			200	
$t_{a(CE)}$	Card select access time	$\overline{OE} = V_{IL}$	1M, 2M			250	ns
			others			200	
$t_{a(OE)}$	Output enable access time	$\overline{CE} = V_{IL}$	1M, 2M			125	ns
			others			100	
t_{DF}	Output disable time (from $\overline{OE}$)	$\overline{CE} = V_{IL}$	1M, 2M	0		110	ns
			others	0		100	
t_{OH}	Data hold time after address change	$\overline{CE} = \overline{OE} = V_{IL}$		0			ns

Note 2 : V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

TIMING DIAGRAM (READ OPERATION)



Note 3 : Test conditions

Input pulse levels		: V_{IL} = 0.45V, V_{IH} = 0.8 × V_{CC} V
Input pulse rise, fall time		: $t_r = t_f$ = 10ns
Reference voltage	input	: V_{IL} = 0.8V, V_{IH} = 0.7 × V_{CC} V
	output	: V_{OL} = 0.8V, V_{OH} = 2.0V
		(t_{DF} is measured when output voltage is ±500mV from steady state.)
Load		: 100pF + 1TTL gate
		: 5pF + 1TTL gate (at t_{DF} measuring)

PROGRAM OPERATION

RECOMMENDED OPERATING CONDITIONS (T_a=20~30℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} supply voltage	12.2	12.5	12.8	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a=20~30℃, V_{CC}=5.75~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH}=−400μA		2.4			V
V_{OL}	Low output voltage	I_{OL}=2.1mA				0.45	V
I_{IH}	High input current	V_I=V_{CC} V				10	μA
I_{IL}	Low input current	V_I=0V	$\overline{PGM}$ $\overline{OE}$ $\overline{CE}$			−20	μA
			Other inputs			−10	
$I_{CC}3$ ・1	Active V_{CC} supply current	Inputs=V_{IH} or V_{IL}, Outputs=open	128K			145	mA
			256K			210	
			512K			320	
			1M			520	
			2M			965	
$I_{CC}3$ ・2	Active V_{CC} supply current	Inputs≦0.2V or ≧V_{CC}−0.2V, Outputs=open	128K			65	mA
			256K			120	
			512K			220	
			1M			420	
			2M			820	
$I_{PP}2$ ・1	V_{PP} supply current	$\overline{CE}$=V_{IL} <BYTE PROGRAM>	128K			65	mA
			256K			70	
			512K			75	
			1M			80	
			2M			100	
$I_{PP}2$ ・2		$\overline{CE}$=V_{IH} <PAGE PROGRAM>	128K			115	mA
			256K			120	
			512K			125	
			1M			130	
			2M			150	

Note 4 : Direction for current flowing into IC is indicated as positive (no mark).

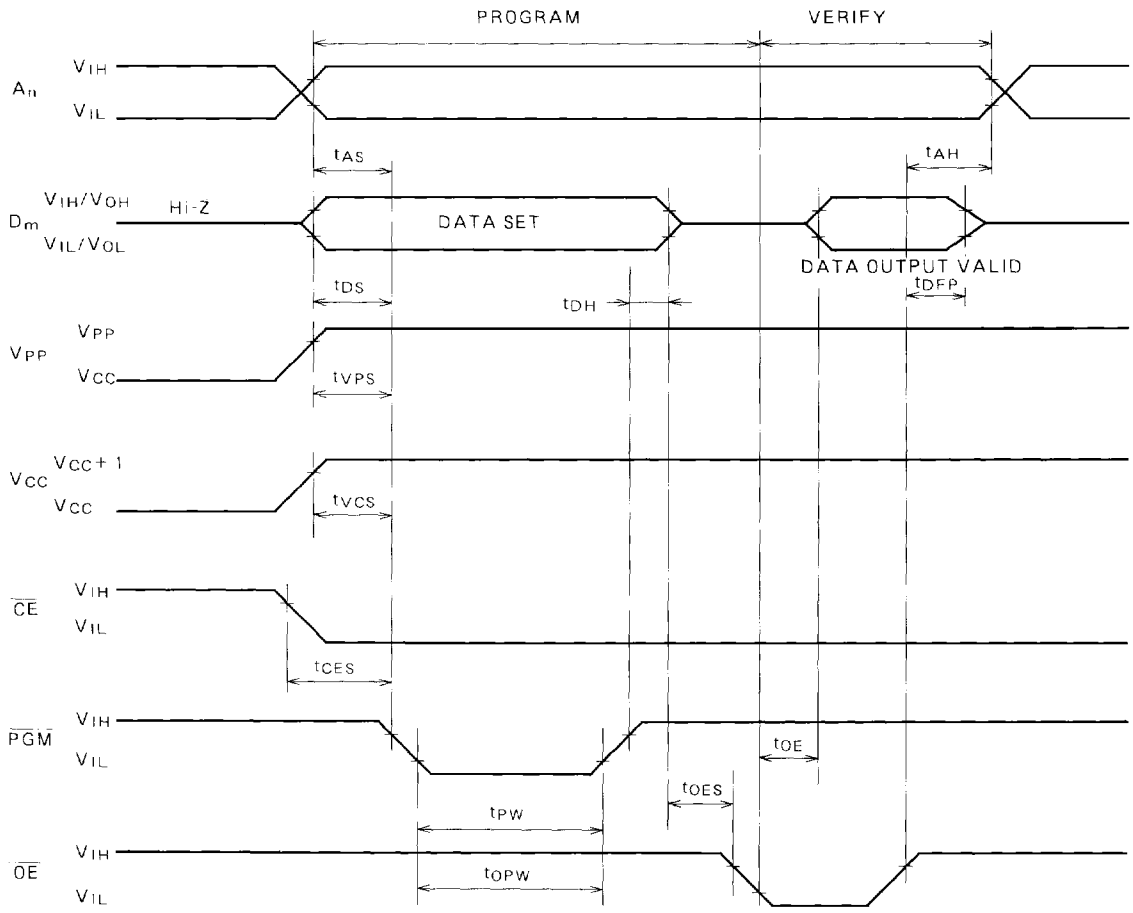
BYTE PROGRAM

SWITCHING CHARACTERISTICS (T_a=20~30℃, V_{CC}=5.75~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address setup time	2			μs
t_{OES}	$\overline{OE}$ setup time	2			μs
t_{DS}	Data setup time	2			μs
t_{AH}	Address hold time	0			μs
t_{DH}	Data hold time	2			μs
t_{DFP}	Output disable time (from $\overline{OE}$)	0		180	ns
t_{VCS}	V_{CC} setup time	2			μs
t_{VPS}	Vpp setup time	2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width	0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width	0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time	2			μs
t_{OE}	Data valid from $\overline{OE}$			200	ns

Note 5 : V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.
6 : Typical value is at V_{CC}= 6 V, V_{PP}=12.5V, T_a=25℃.

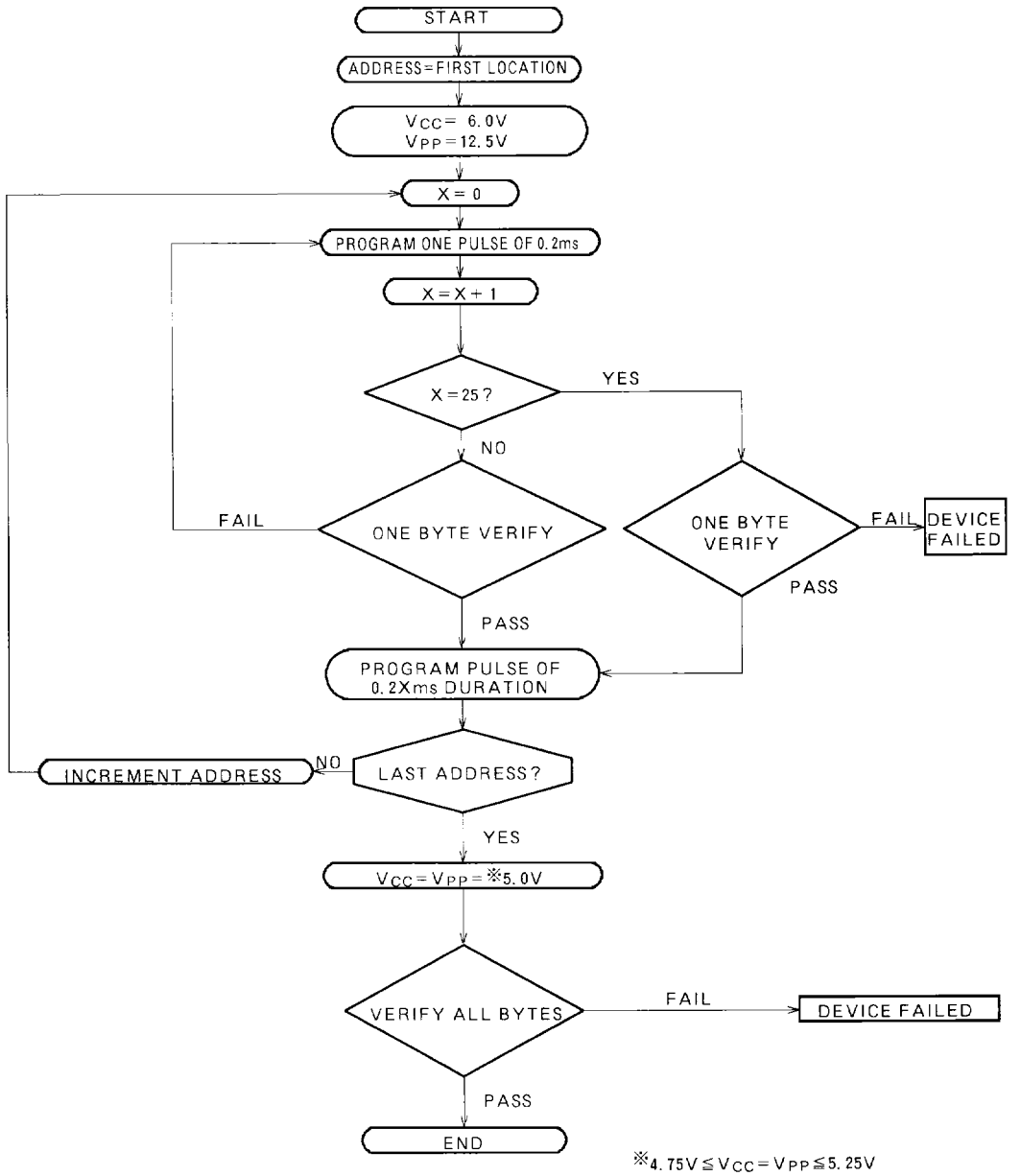
BYTE PROGRAM
TIMING DIAGRAM (PROGRAM OPERATION)



Note 7 : Test conditions

Input pulse levels	: V_{IL}=0.45V, V_{IH}=0.8×V_{CC} V
Input pulse rise, fall time	: t_r=t_f=10ns
Reference voltage input	: V_{IL}=0.8V, V_{IH}=0.7×V_{CC} V
output	: V_{OL}=0.8V, V_{OH}=2.0V
	(t_{DFP} is measured when output voltage is ±500mV from steady state.)

BYTE PROGRAMMING ALGORITHM FLOW CHART



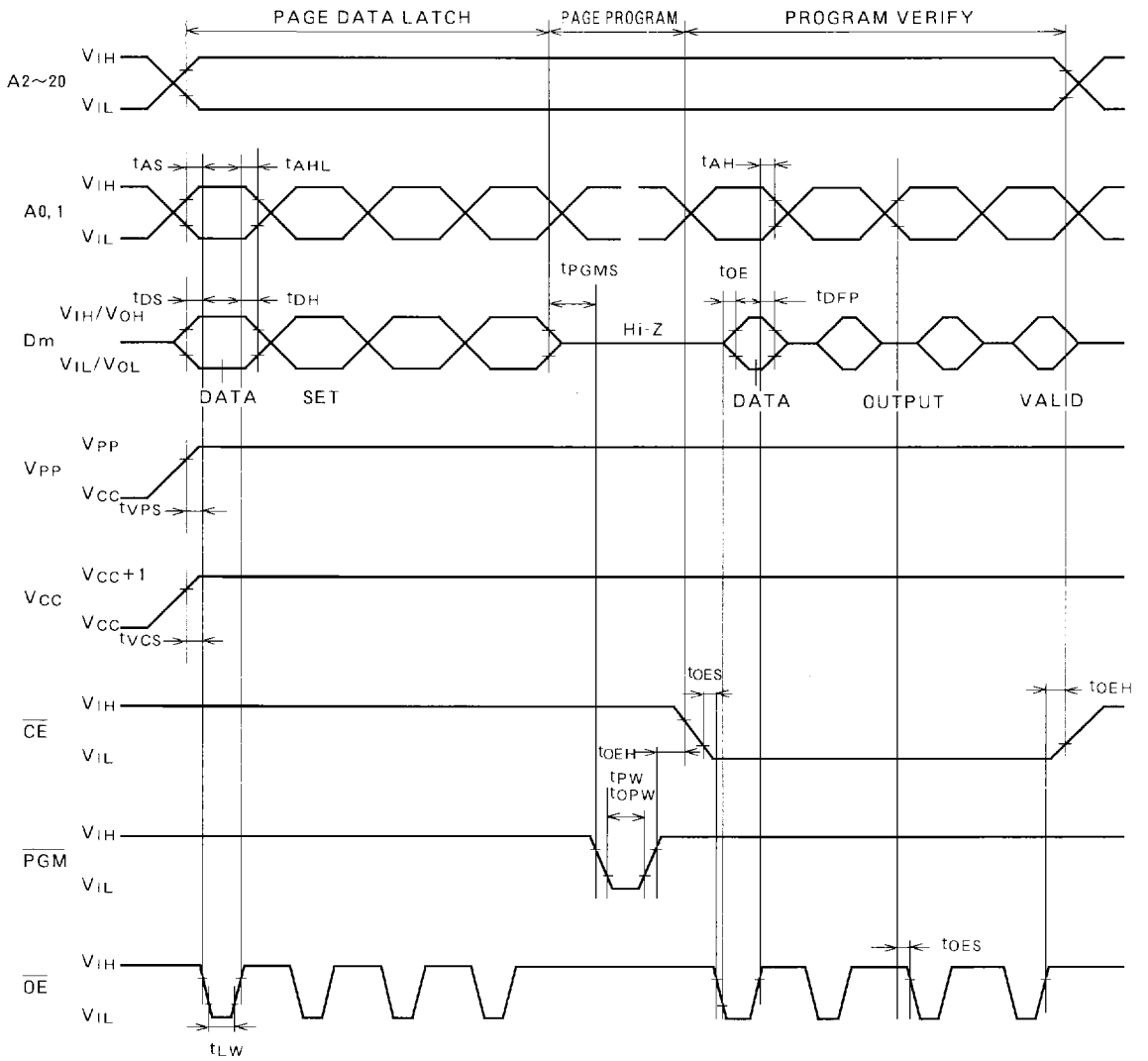
PAGE PROGRAM

SWITCHING CHARACTERRISTICS (T_a=20~30°C, V_{CC}=5.25~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address setup time	2			μs
t_{OES}	$\overline{OE}$ setup time	2			μs
t_{DS}	Data setup time	2			μs
t_{AH}	Address hold time	0			μs
t_{AHL}		2			μs
t_{DH}	Data hold time	2			μs
t_{DFP}	Output disable time (from $\overline{OE}$)	0		180	ns
t_{VCS}	V_{CC} setup time	2			μs
t_{VPS}	V_{PP} setup time	2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width	0.19	0.20	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width	0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time	2			μs
t_{OE}	Data valid from $\overline{OE}$	0		200	ns
t_{LW}	Data latch time	1			μs
t_{PGMS}	$\overline{PGM}$ setup time	2			μs
t_{CEH}	$\overline{CE}$ hold time	2			μs
t_{OEH}	$\overline{OE}$ hold time	2			μs

Note 8 : V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

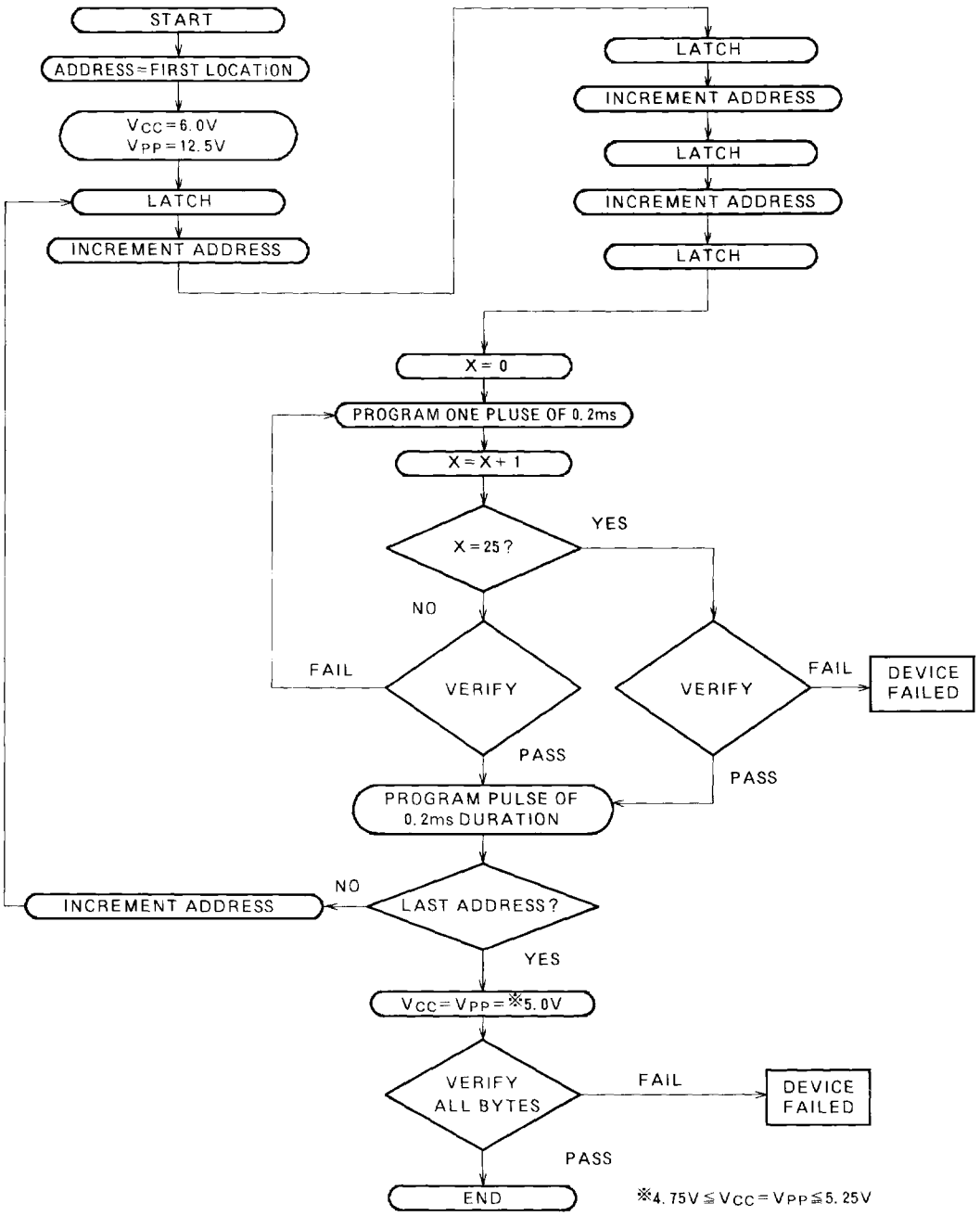
PAGE PROGRAM TIMING DIAGRAM (PROGRAM OPERATION) (2 M Byte type)



Note 9 : Test conditions

Input pulse levels	: $V_{IL}=0.45V$, $V_{IH}=0.8\times V_{CC}$ V	
Input pulse rise, fall time	: $t_r=t_f=10ns$	
Reference voltage input	: $V_{IL}=0.8V$, $V_{IH}=0.7\times V_{CC}$ V	(t_{DFP} is measured when output voltage
output	: $V_{IL}=0.8V$, $V_{IH}=2.0V$	is ±500mV from steady state.)

PAGE PROGRAMMING ALGORITHM FLOW CHART



CAPACITANCE

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1 MHz, T_a = 25℃	128K			30	pF
			256K			40	
			512K				
			1 M			55	
			2 M			70	
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1 MHz, T_a = 25℃	128K			35	pF
			256K			50	
			512K			80	
			1 M			140	
			2 M			260	

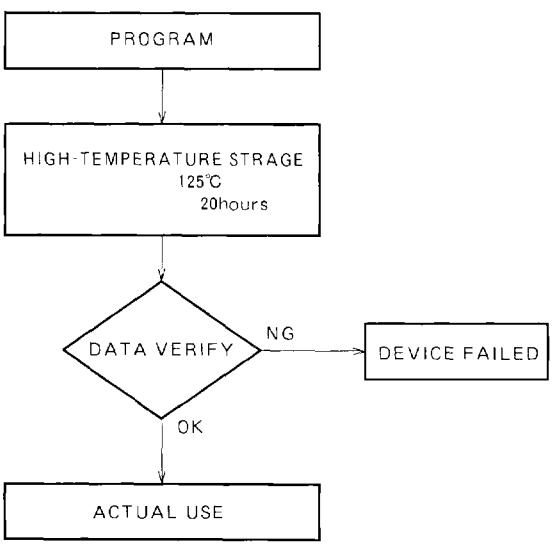
Note 10 : These items are not 100% tested.

DEVICE IDENTIFIER MODE

This card does not support a device identifier mode.
Do not apply voltages exceeding 7 V to A 9 pin.

RECOMMENDED SCREENING CONDITIONS

The following screening test recommended before using a card for evaluation which you have programmed. If you use cards for other purpose, it is recommended that the manufacturer programs them.



Note 11 : The color of the panels might be affected at this high-temperature storage.
After the data-verify test, putting on your designed labels on the surface of the card is recommended.