

Features

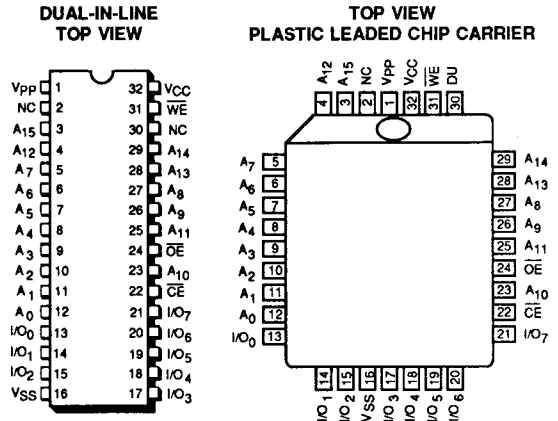
- 64K Byte Flash Erasable Non-Volatile Memory
- Low Power CMOS Process
- Electrical Byte Write and Chip/Sector Erase
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- Flash EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
 - Minimum 100 Cycle Endurance
 - Optional 1000 Cycle Endurance Screening
 - Minimum 10 Year Data Retention
- 5 V ± 10% V_{CC}, 0°C to +70°C Temperature Range
- Silicon Signature®
- JEDEC Standard Byte Wide Pinout
 - 32 Pin DIP
 - 32 Pin J-Bend Plastic Leaded Chip Carrier

Description

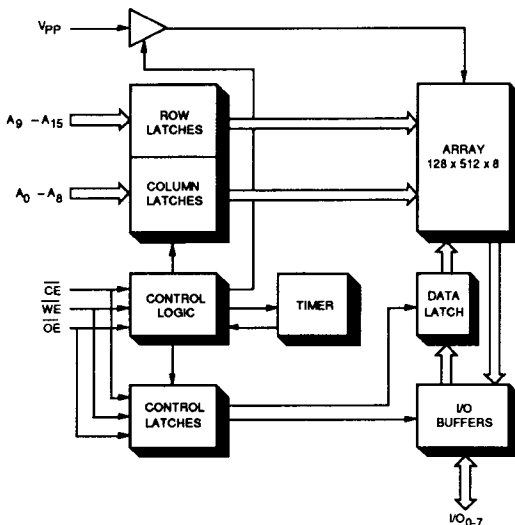
The 48F512 is a 512K bit CMOS FLASH EEPROM organized as 64K x 8 bits. SEEQ's 48F512 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

SEEQ's patented split gate FLASH EEPROM cell design reduces both the time and cost required to alter code in program and data storage applications.

Pin Configuration



Block Diagram



Pin Names

A ₀ -A ₈	COLUMN ADDRESS INPUT
A ₉ -A ₁₅	ROW ADDRESS INPUT
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O ₀₋₇	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V _{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

Silicon Signature is a registered trademarks of SEEQ Technology.

The 48F512's fast electrical erase and 0.5 ms/byte programming is 20 times faster than reprogramming of UVEPROMs. Electrical erase and reprogramming make the 48F512 ideal for applications with high density requirements, but where ultraviolet erasure is either impractical or impossible.

SEEQ's FLASH memories provide users with the flexibility to alter code in all or small sections of the memory array. The memory array is divided into 128 sectors, with each sector containing 512 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the 48F512 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address on $A_0 - A_{13}$ with chip enable (\overline{CE}) and output enable (\overline{OE}) at V_{IL} and write enable (\overline{WE}) at V_{IH} . The V_{pp} pin can be at any TTL level or V_p during read operations. See page 5 for additional information on A.C. parameters and read timing waveforms.

Erase and Write

Erasing and writing of the 48F512 can only be accomplished when $V_{pp} = V_p$. Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. All control pins are noise protected; a pulse of less than 20 ns will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{pp} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_0 through A_{13} . The data inputs must be all ones to begin the erase. Following

a write of 'FF', the part will wait for time t_{ABORT} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{ABORT} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{pp} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase will change all bits in the memory to a logical 1. The 48F512 uses a two-step, software controlled looping algorithm to perform the chip erase operation. Each loop requires that a chip erase select be performed prior to the start of each chip erase cycle.

Byte Write

A byte write is used to change any 1 in a byte to a 0. Individual bytes, multiple bytes or the entire memory can be written at one time. If a bit in a byte needs to be changed from a 0 to a 1, the byte must first be erase via sector or chip erase and then reprogrammed with the desired data. Any byte write operation requires that the V_{pp} pin be at high voltage (V_p).

Data is organized in the 48F512 in a group of bytes called a sector. The memory array is divided into 128 sectors of 512 bytes each. Individual bytes are written as part of a sector write operation. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.

The 48F512 uses a software controlled looping algorithm (figure 1) to perform writes and verify successful byte programming. During a byte write operation, all non "FF" bytes are incrementally written using a 75 μ s minimum t_{wc} . Each byte write is automatically latched and timed on-chip, so that the microprocessor can perform other tasks once the write cycle has been initiated. Write cycle time duration can be controlled by the microprocessor, or the on-chip timer will automatically terminate t_{wc} after 150 μ s. One write loop has been completed when all non "FF" data for all desired bytes have been written. After 7 programming loops, a read-verification cycle is performed. For any bytes which do not verify, a fill-in programming loop is performed.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sectors must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

¹ Only non "FF" bytes can be written.

Power Up/Down Protection

This device contains a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input (\overline{CE} , \overline{OE} , \overline{WE}) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage

Silicon Signature Bytes

	A_0	Data (Hex)
SEEQ Code	V_{IL}	94
Product Code 48F512	V_{IH}	1A

may result. To minimize switching transients on this pin we recommend using a minimum 0.1 μ f decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 48F512 which contains the device's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_0 to 12 ± 0.5 V and bringing all other address inputs, plus chip enable, and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0 .

Mode Selection Table

Mode	\overline{CE}	\overline{OE}	\overline{WE}	V_{PP}	A_{9-15}	A_{0-8}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip Erase Select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip Erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Block Erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Range*

Temperature

Storage -65°C to +125°C

Under Bias -10°C to +85°C

All inputs except V_{PP} and outputs with respect to V_{SS} +7 V to -0.5 V

V_{PP} pin with respect to V_{SS} 14 V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

E.S.D. Characteristics^[1]

Symbol	Parameter	Value	Test Condition
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note: Characterization data — not tested.

Recommended Operating Conditions

48F512	
Temperature Range (Ambient)	0°C to 70°C
V _{CC} Supply Voltage	5V ± 10%

Capacitance^[2] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Value	Test Condition
C _{IN}	Input Capacitance	6 pF	V _{IN} = 0 V
C _{OUT}	Output capacitance	12 pF	V _{IO} = 0 V

Note 2: This parameter is only sampled and not 100% tested.

DC Operating Characteristics Over the V_{CC} and temperature range

Symbol	Parameter	Limits			Test Condition	
		Min.	Max.	Unit		
I _{LI}	Input Leakage		1	μA	V _{IN} = 0.1V to V _{CC}	
I _{LO}	Output Leakage		10	μA	V _{IN} = 0.1V to V _{CC}	
V _P	Program/Erase Voltage	11.4	13	V		
V _{PR}	V _{pp} Voltage During Read	0	V _P	V		
I _{PP}	V _P Current	Standby Mode		200	μA	$\overline{CE} = V_{IH}, V_{PP} = V_{PR}$
		Read Mode		200	μA	$\overline{CE} = V_{IL}, V_{PP} = V_{PR}$
		Byte Write		30	mA	V _{PP} = V _P
		Chip Erase Sector Erase		60 10	mA mA	V _{PP} = V _P V _{PP} = V _P
I _{CC1}	Standby V _{CC} Current		100	μA	$\overline{CE} = V_{CC} - 0.3V$	
I _{CC2}	Standby V _{CC} Current		5	mA	$\overline{CE} = V_{IH}$ min.	
I _{CC3}	Active V _{CC} Current		40	mA	$\overline{CE} = V_{IL}$	
V _{IL}	Input Low Voltage	-0.3	0.8	V		
V _{IH}	Input High Voltage	2.0	7.0	V		
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2.1 ma	
V _{OH1}	Output Level (TTL)	2.4		V	I _{OH} = -400 μA	
V _{OH2}	Output Level (CMOS)	V _{CC} -1.0		V	I _{OH} = -100 μA	

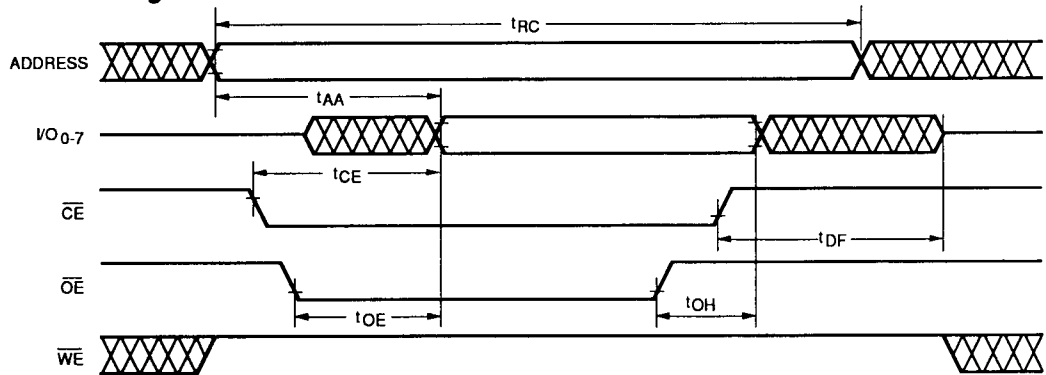
READ

AC Characteristics

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{AA}	Address to Data		200		250		300	ns
t_{CE}	\overline{CE} to Data		200		250		300	ns
t_{OE}	\overline{OE} to Data		75		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to Data Float		50		60		100	ns
t_{OH}	Output Hold Time	0		0		0		ns

Read Timing



A.C. Test Conditions

Output Load: 1 TTL gate and $C(load) = 100$ pF

Input Rise and Fall Times: < 20 ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level:

Inputs 1V and 2V

Outputs 0.8V and 2V

Byte Write

AC Characteristics

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F512		Unit
		Min.	Max.	
t_{VPS}	V_{PP} Setup Time	2		μ s
t_{VPH}	V_{PP} Hold Time	150		μ s
t_{CS}	\overline{CE} Setup Time	0		ns
t_{CH}	\overline{CE} Hold Time	0		ns
t_{OES}	\overline{OE} Setup Time	10		ns
t_{OEH}	\overline{OE} Hold Time	10		ns
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	\overline{WE} Pulse Width	100		ns
t_{WC}	Write Cycle Time	75		μ s
t_{WR}	Write Recovery Time		1.5	ms

NOTE: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g. access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Byte Write Timing

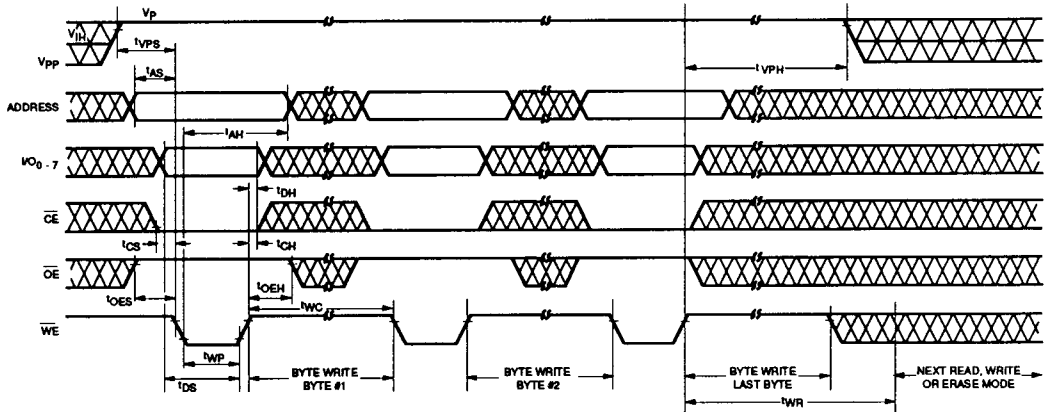
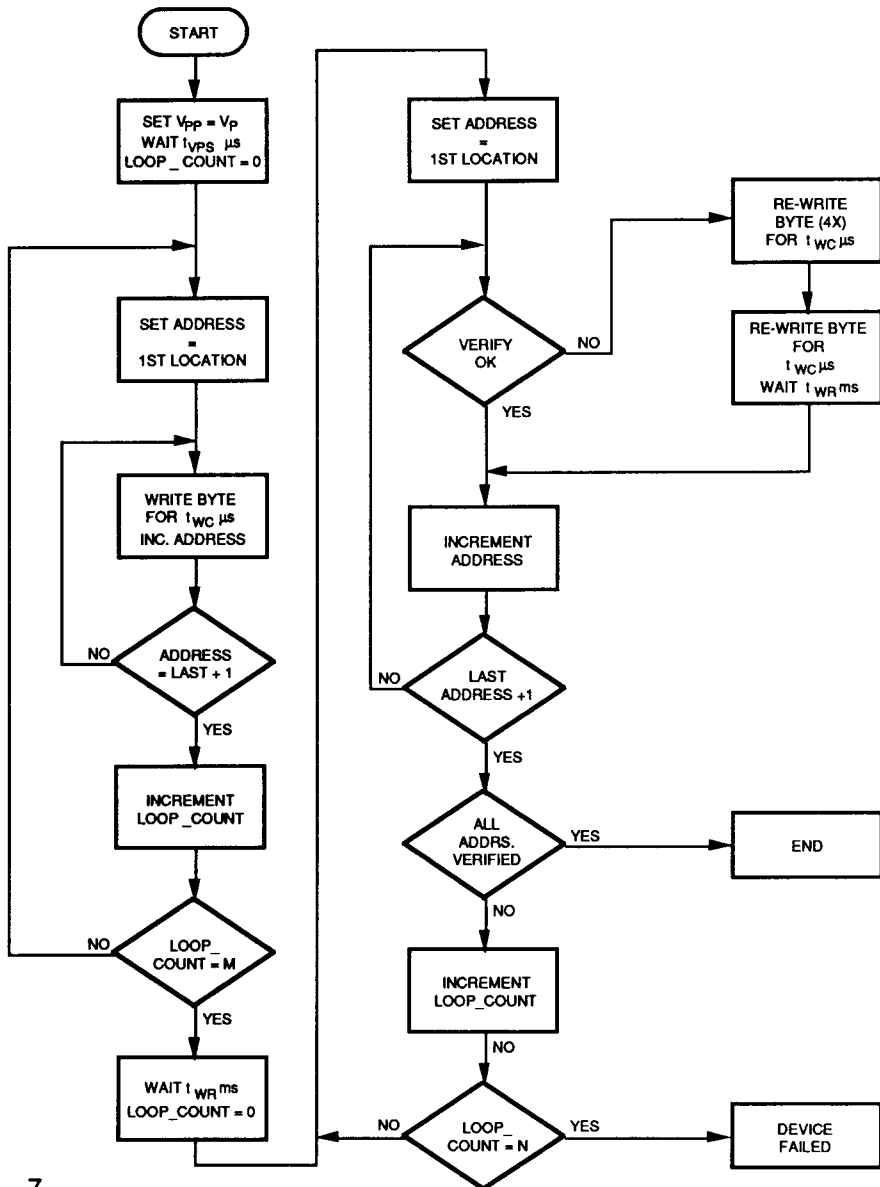


Figure 1
48F512 Write Algorithm



M = 7
N = 6

Sector Erase

AC Characteristics

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F512		Unit
		Min.	Max.	
t_{VPS}	V_{PP} Setup Time	2		μ s
t_{VPH}	V_{PP} Hold Time	500		ms
t_{CS}	\overline{CE} Setup Time	0		ns
t_{OES}	\overline{OE} Setup Time	0		ns
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	\overline{WE} Pulse Width	100		ns
t_{CH}	\overline{CE} Hold Time	0		ns
t_{OEH}	\overline{OE} Hold Time	0		ns
t_{ERASE}	Sector Erase Time	500		ms
t_{ABORT}	Sector Erase Delay		250	μ s
t_{ER}	Erase Recovery Time		250	ms

Sector Erase Timing

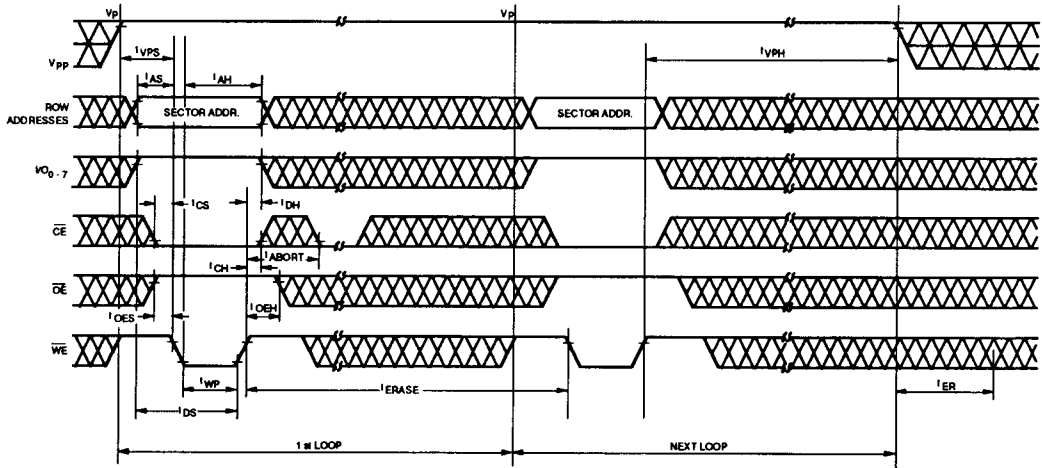
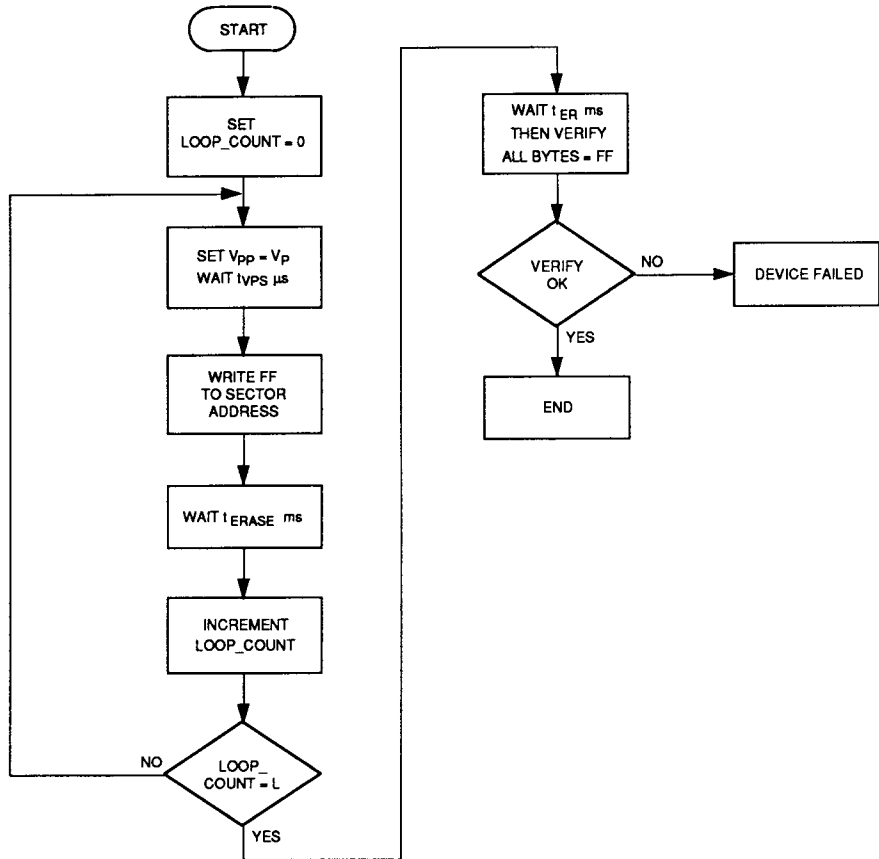


Figure 2
48F512 Sector Erase Algorithm



L = 24

Chip Erase

AC Characteristics

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F512		Unit
		Min.	Max.	
t_{VPS}	V_{PP} Setup Time	2		μs
t_{VPH}	V_{PP} Hold Time	500		ms
t_{CS}	\overline{CE} Setup Time	0		ns
t_{OES}	\overline{OE} Setup Time	0		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	\overline{WE} Pulse Width	100		ns
t_{CH}	\overline{CE} Hold Time	0		ns
t_{OEH}	\overline{OE} Hold Time	0		ns
t_{ERASE}	Chip Erase Time	500		ms
t_{ER}	Erase Recovery Time		250	ms

Chip Erase Timing

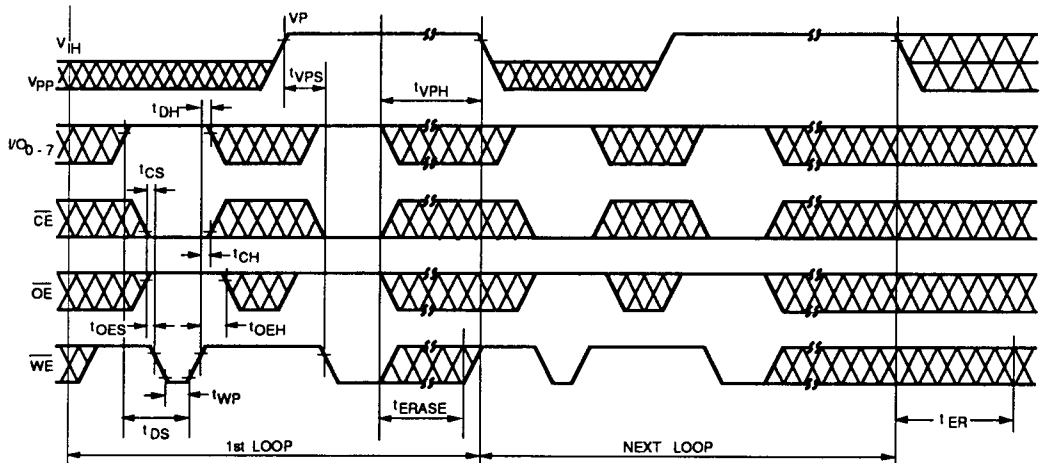
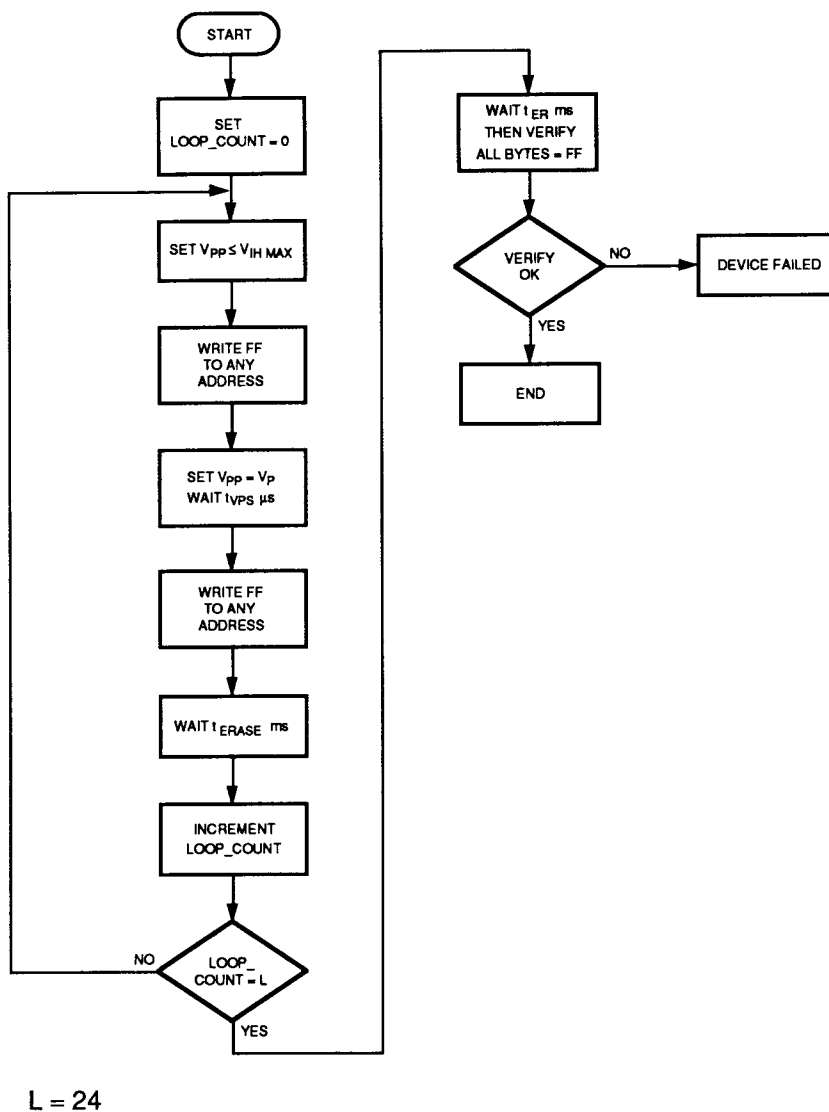


Figure 3
48F512 Chip Erase Algorithm



Ordering Information

<u>D</u> Package Type	<u>Q</u> Temperature Range	<u>48F512</u> Device	<u>K</u> Endurance	<u>- 200</u> Access Time
D = Ceramic Dip P = Plastic Dip N = Plastic Leaded Chip Carrier	Q = 0 to 70° C	64K x 8 FLASH EEPROM	BLANK = 100 K = 1000	200 = 200 ns 250 = 250 ns 300 = 300 ns