MP7695 DIE

10-Bit Low Power
Analog-to-Digital Converter
CMOS Die Specifications

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (TA = 25°C)

V_{DD} (to GND) .... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ .... V_{DD} +0.5 to GND –0.5 V
V_{IN} .... V_{DD} +0.5 to GND –0.5 V
All Inputs .... V_{DD} +0.5 to GND –0.5 V
All Outputs .... V_{DD} +0.5 to GND –0.5 V
T_J (maximum) .... +150°C

Ordering Information

Part No.	Parameters	
	INL (LSB)	DNL (LSB)
MP7695J-DIE	2.0	2.0

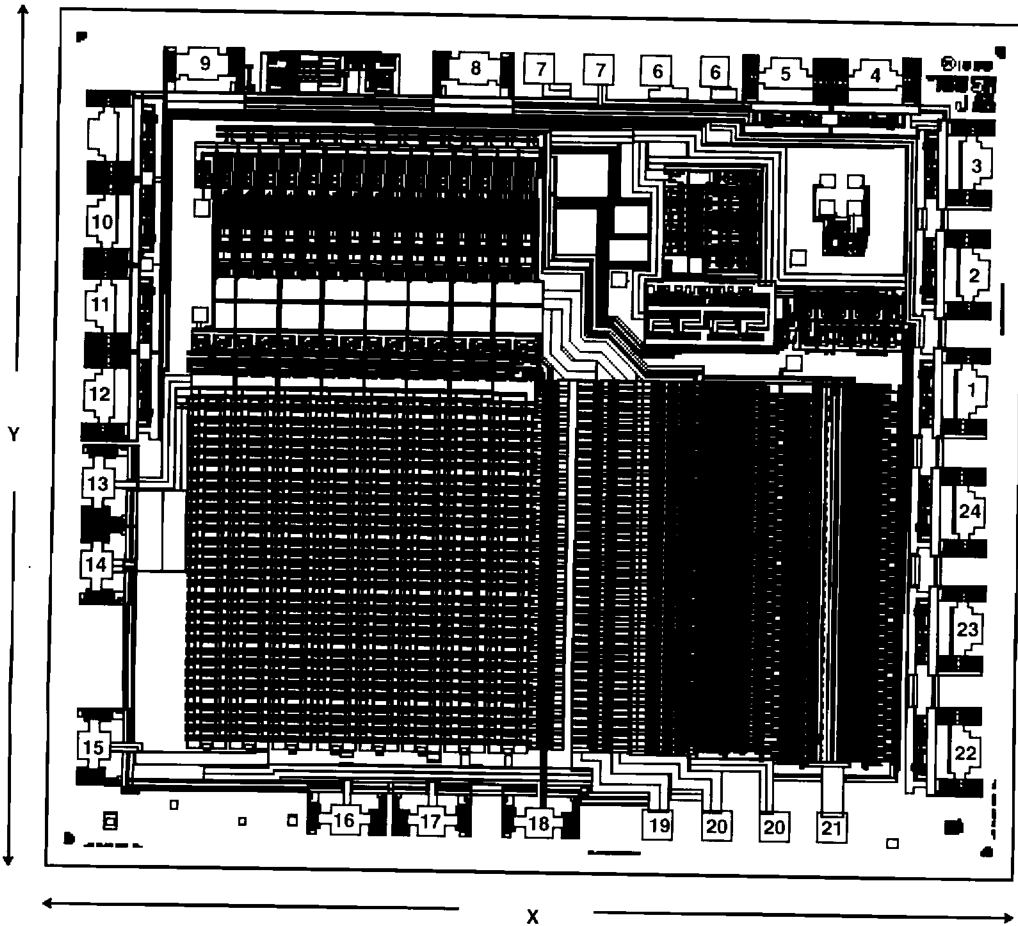
Electrical Parameters And Test Conditions (TA = 25°C, V_{DD} = 5 V, V_{REF} = 4.6 V, F_S = 1 MHz)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	CONDITIONS
N	Resolution	10		Bits	
INL	Relative Accuracy		2.0	LSB	Best Straight Line
DNL	Differential Non-Linearity		2.0	LSB	
I_{O2}	Output Leakage Current	–10.0	10.0	μA	
R_{IN}	Ref. Resistance	420	980	KΩ	
V_{IN}	Logic "1"	2.0		V	
V_{IL}	Logic "0"		0.8	V	
V_{OH}	Digital o/p, Logic "1"	V_{DD}-.5		V	I_L = 2.0 mA
V_{IL}	Digital o/p, Logic "0"		0.4	V	I_L = 4.0 mA
I_{DD}	Supply Current		20.0	mA	

NOTES:

1. Die are 100% electrically tested in wafer form to meet the limits shown above.
2. Die are visually inspected per MIL-STD-883, Method 2010, condition B to an AQL of 2.5%.
3. Absolute maximum ratings are for TA = 25°C unless otherwise specified.
4. AC electrical characteristics are neither guaranteed nor tested in die form.
5. Electrical performance and yield after assembly are not guaranteed due to variations in assembly processes.
6. Wafers and die are processed using ESD handling precautions, and are shipped vacuum-packed.

PHYSICAL CHARACTERISTICS



Die Data

Die Size	X = 130 mils, Y = 148 mils
Pad Size	4 X 4 mils nominal
Pad Metal	Al
Thickness	15 mils nominal
Backside Material	Si
Backside Potential	V_{DD}

Pad Designations

1. DB3
2. DB4
3. DB5
4. DB6
5. DB7
6. DGND
7. DV_{DD}
8. CLK
9. $\overline{OE}$
10. DB8
11. DB9
12. OFW
13. $V_{REF(+)}$
14. $V_{REF(-)}$
15. R1
16. R2
17. R3
18. V_{IN}
19. AGND
20. AV_{DD}*
21. AGND
22. DB0
23. DB1
24. DB2

*Connect pin 20 first