


SANYO Semiconductors

DATA SHEET

LV23200T — Bi-CMOS IC For Home Stereo System 1-chip Tuner IC Incorporating PLL

Overview

The LV23200T is a one-chip tuner IC incorporating PLL for home stereo system.

Functions

- AM tuner Changeover of the constant in RFAMP, MIX, OSC, IF AMP, DET, AGC, SD, OSC BUFF, IF BUFF, and AGC modes.
- FM tuner 1stIFAMP, IF limiter AMP, DET (COIL type) , S-METER, SD, AFC, IF BUFF.
- MPX PLL STEREO DECODER, forced MONO, AUDIO MUTE, function to prevent interference from a neighboring station, PILOT canceling function.
- PLL frequency synthesizer.

Features

- Tuner IC and PLL IC integrated into one chip.
- MPX-VCO incorporated and without need of adjustment.
- FM/AM output level independent setting possible.
- MOS transistor for active LPF incorporated.

Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	V _{CC}	7.0	V
	V _{DD} max	V _{DD}	6.0	V
Operating temperature	T _{opr}		-20 to +80	°C
Storage temperature	T _{stg}		-40 to +125	°C

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LV23200T

Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		5.0	V
	V _{DD}		3.0	V
Operating supply voltage range	V _{CC} op		4.5 to 6.0	V
	V _{DD} op1	X'tal oscillation = 4.5MHz	2.7 to 3.3	V

* Handle pin 34 with care because its electrostatic voltage at C = 200pF and R = 0Ω is 110 V.

Operating Characteristics at Ta = 25°C, V_{CC} = 5.0V, V_{DD} = 3.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	I _{CC} FM	No input in FM mode	25	35	45	mA
AM tuner block	I _{CC} AM	No input in AM mode	14	24	34	mA
PLL block	I _{DD} FM	X'tal = 4.5MHz, No input at tuner	2.0	3.0	4.0	mA
[FM-FE characteristics (MPX)] : FM-IF (5PIN) input, fc = 10.7MHz, fm = 1kHz, 75kHzdev (L+R = 90%, Pilot = 10%)						
Demodulation output	V _O	V _{IN} = 100dBμV	450	550	650	mVrms
3dB sensitivity 1	LS1	V _{IN} = 70dBμV reference, input at -3dB *at input of FIFA (pin 1)		28	33	dBμV
3dB sensitivity 2	LS2	V _{IN} = 100dBμV reference, input at -3dB *at input of FMFA (pin 5)		35	40	dBμV
Total harmonic distortion	THD1	V _{IN} = 100dBμV, MONO		0.4	1.5	%
Signal-to-noise ratio	S/N	V _{IN} = 100dBμV	70	76		dB
AM suppression ratio	AMR	V _{IN} = 100dBμV, AM = 30%	36	40		dB
SD sensitivity	SD-1	0%mod, SD sensitivity mode 1	43	50	57	dBμV
Total harmonic distortion	THD2	V _{IN} = 100dBμV, MAIN-MOD		0.5	1.5	%
Separation	SEP	V _{IN} = 100dBμV, L output/R output	30	45		dB
ST sensitivity	VL	V _{IN} = 100dBμV, (L+R)+Pilot		3.0	5.5	%
Mute attenuation	MUTE	V _{IN} = 100dBμV, L output		60		dB
Carrier leakage	CL	V _{IN} = 100dBμV, (L+R)+Pilot	30	40		dB
[AM characteristics] : fc = 999kHz, fm = 1kHz, 30%mod						
Demodulation output 1	V _O 1	V _{IN} = 23dBμV, 30%mod, fm = 1kHz	50	80	130	mVrms
Demodulation output 2	V _O 2	V _{IN} = 80dBμV, 30%mod, fm = 1kHz	170	240	310	mVrms
Signal-to-noise ratio 1	S/N1	V _{IN} = 23dBμV	15	20		dB
Signal-to-noise ratio 2	S/N2	V _{IN} = 80dBμV	48	54		dB
Total harmonic distortion	THD	V _{IN} = 80dBμV		0.4	1.3	%
SD sensitivity	SD-ON	0%mod (Internally fixed sensitivity)	14	24	34	dBμV
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	VHIS	CE, CL, DI		0.1V _{DD}		V
Output high level voltage	V _{OH}	PD ; I _O = -1mA	V _{DD} -1.0			V
Output low level voltage	V _{OL} 1	PD ; I _O = 1mA			1.0	V
	V _{OL} 2	BO ; I _O = 1mA			0.25	V
		BO ; I _O = 5mA			1.25	V
	V _{OL} 3	DO ; I _O = 1mA			0.25	V
	V _{OL} 4	AOUT ; I _O = 1mA, AIN = 2.0V			0.5	V
Output high level voltage	I _{IH} 1	CE, CL, DI ; VI = 6.0V			5.0	μA
	I _{IH} 2	XIN ; VI = V _{DD}	0.16		0.9	μA
	I _{IH} 3	AIN ; VI = 6.0V			200	nA
Input high level current	I _{IL} 1	CE, CL, DI ; VI = 0V			5.0	μA
	I _{IL} 2	XIN ; VI = 0V	0.16		0.9	μA
	I _{IL} 3	AIN ; VI = 0V			200	nA

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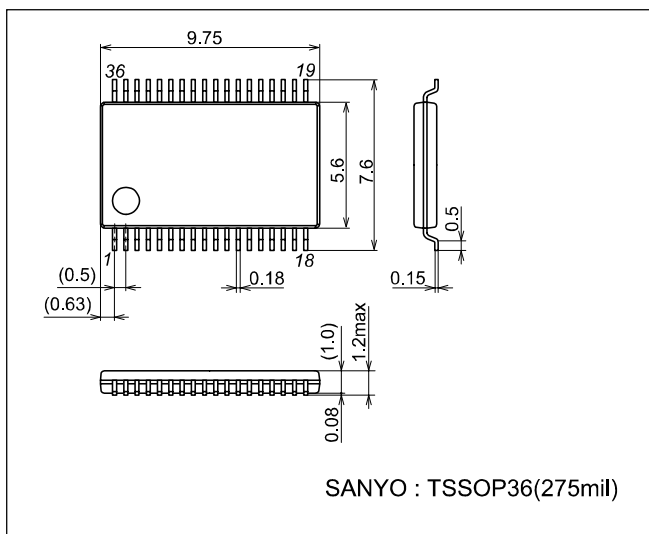
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output off-leak current	I_{OFF1}	BO, AOUT ; $V_O = 10V$			5.0	μA
	I_{OFF2}	DO ; $V_O = 6.0V$			5.0	μA
"H" level 3-state off-leak current	I_{OFFH}	PD ; $V_O = 6.0V$		0.01	200	nA
"L" level 3-state off-leak current	I_{OFFL}	PD ; $V_O = 0V$		0.01	200	nA

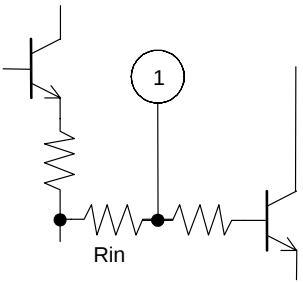
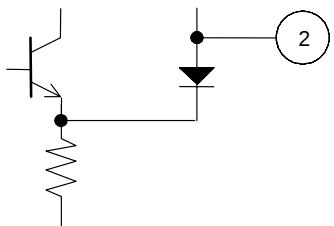
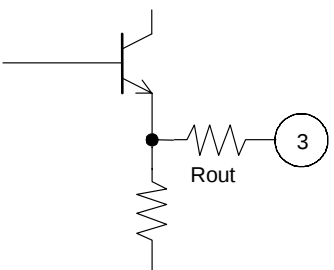
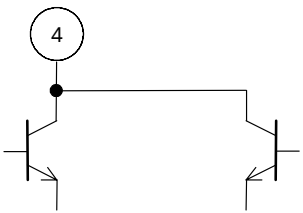
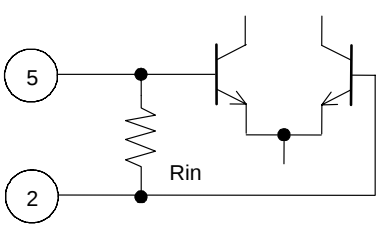
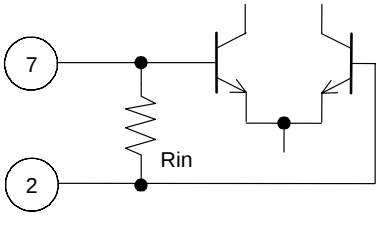
Package Dimensions

unit : mm

3253B



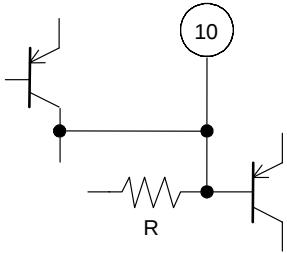
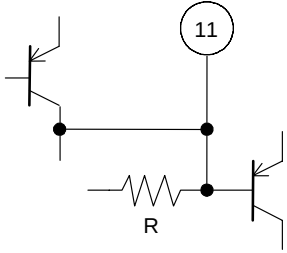
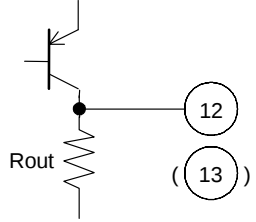
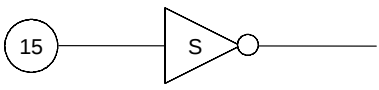
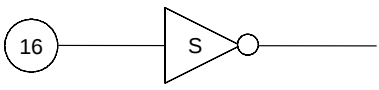
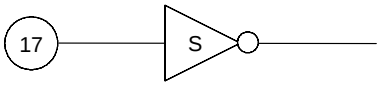
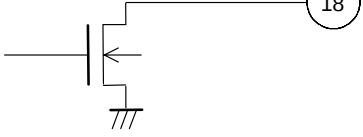
Description of Pin Functions

No.	Functions	Voltage (V)	Internal Equivalent Circuit	Remarks
1	FM 1stIF-AMP input	1.6V		Input impedance r_i (R_{in}). $R_{in} = 330\Omega$
2	REG	2.2V		Reference voltage of AM/FM IF/MPX block. $V_{reg} = 2.2V$
3	FM 1st IF-AMP output	3.0V		Output impedance r_o (R_{out}). $R_{out} = 300\Omega$
4	AM MIX output	V_{CC}		MIX coil used between pins 4 and 8 (V_{CC} voltage).
5	FM IF input	V_{reg}		Input impedance r_i (R_{in}). $R_{in} = 330\Omega$
6	GND	0V		AM/FM IF/MPX block GND
7	AM IF input	2.2V		Input impedance r_i (R_{in}). $R_{in} = 2k\Omega$
8	V_{CC}	5.0V		AM/FM IF/MPX block V_{CC}

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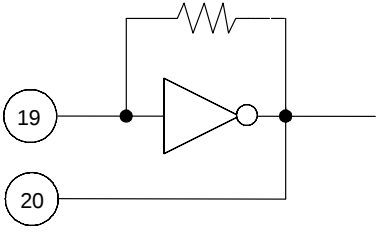
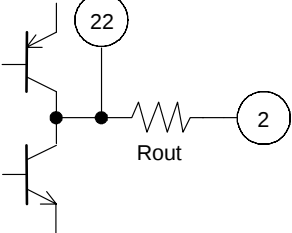
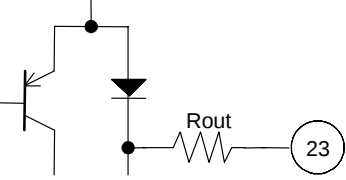
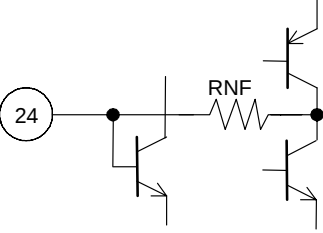
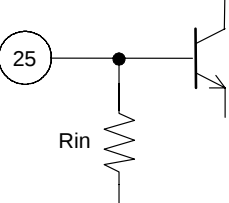
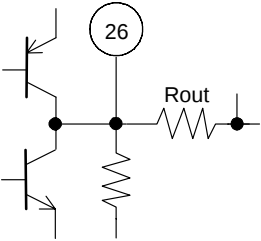
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No.	Functions	Voltage (V)	Internal Equivalent Circuit	Remarks
9	FM DET	V_{CC}		Recommended detection coil. 600BCAS-10790Z
10	Phase comparator filter	$V_{CC}-1.0V$		$R = 10k\Omega$
11	Pilot filter	$V_{CC}-1.0V$		$R = 10k\Omega$
12 13	L output R output	2.5V		Output impedance r_o (Rout). Rout = 7.7k Ω
15	CE	—		Chip enable pin At changeover from "L" to "H": Address latching. At changeover from "H" to "L": Data latching.
16	DI	—		Serial data input pin Sets data in synchronization with rise of data clock.
17	CL	—		Data clock input pin.
18	DO	—		Data output pin Outputs various data in synchronization with fall of data clock in the OUT mode.

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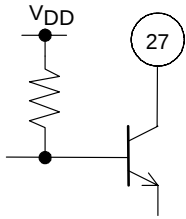
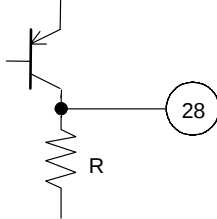
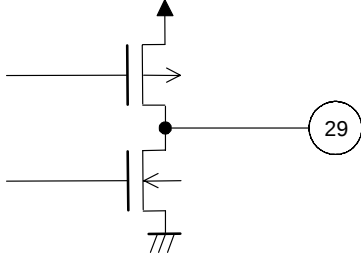
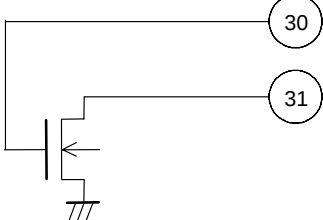
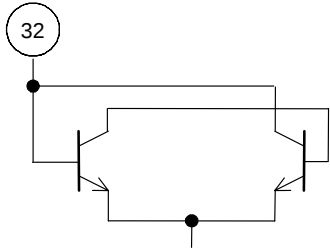
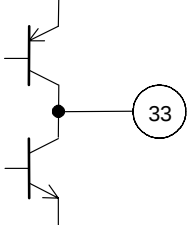
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No.	Functions	Voltage (V)	Internal Equivalent Circuit	Remarks
19 20	X IN X OUT	— —		Clock for internal reference Connect a 4.5 MHz crystal oscillator.
21	V _{DD}	3.0V		AM/FM IF/MPX block V _{DD}
22	Pilot canceling output	V _{reg}		Output impedance ro (Rout). Rout = 30kΩ
23	AM detection output	0.8V (FM) V _{reg} (AM)		Output impedance ro (Rout). Rout = 10kΩ
24	MPX input	V _{reg}		MPX inverse input pin. RNF = 20kΩ
25	PLL input	V _{reg}		Input impedance ri (Rin). Rin = 20kΩ
26	FM detection output	V _{reg} +0.7V		Output impedance ro (Rout). Rout = 3.3kΩ Adjusts separation using the capacitance value of a section between this pin and GND.

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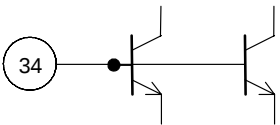
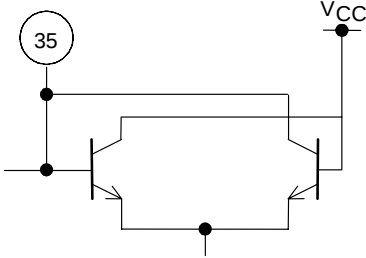
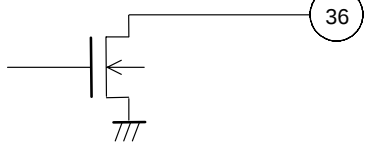
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No.	Functions	Voltage (V)	Internal Equivalent Circuit	Remarks
27	SD monitor	V_{DD}		Active "L" Open collector.
28	FMS meter and AM AGC outputs	0.2V (FM) 0.8V (AM)		Internal load resistance $R = 13.9k\Omega$ Determines the SD response speed during SEEK by a capacitor externally connected to pin 28.
29	PD	—		PLL charge pump output pin.
30 31	AIN AOUT	— —		Nch MOS transistor for PLL active low pass filter.
32	AM OSC	V_{CC}		OSC coil used between pins 32 and 8 (V_{CC} voltage).
33	AFC	V_{reg}		Enables adjustment of the FM SD band width by external resistor between pins 33 and 2 (V_{reg} voltage).

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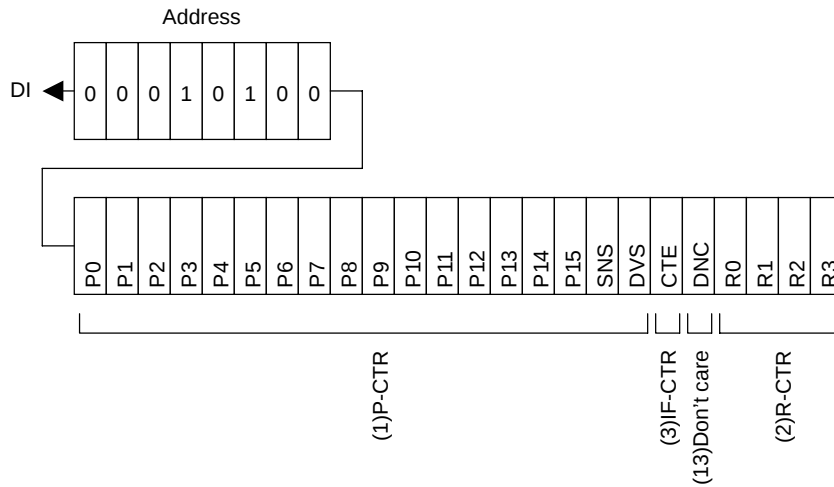
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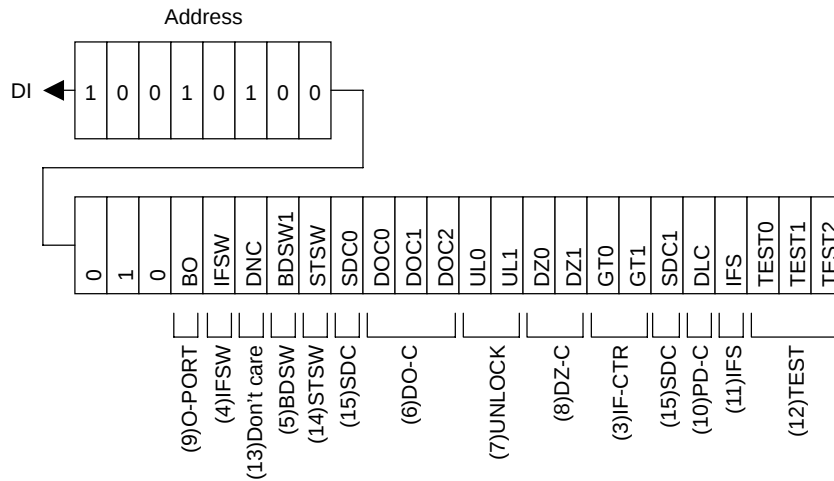
No.	Functions	Voltage (V)	Internal Equivalent Circuit	Remarks
34	AM RF input	Vreg		Use pin 34 with the same potential as for pin 32 (AFC voltage).
35	FM OSC input	V _{CC}		Use pin 35 through pull-up to pin 8 (V _{CC} voltage) by resistance load.
36	BO	—		Pin dedicated for output.

Composition of DI control data (serial data input)

(1) IN1 mode



(2) IN2 mode



Description of DI control Data

No.	Control block data	Description	Related data																																				
(1)	Programmable divider data P0 to P15 DVS, SNS	- Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : Don't care) <table><tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number (N)</th><th>Actual dividing</th></tr><tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr><tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr><tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr></table> * P0 to P3 invalid when LSB : P4 - To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : Don't care) <table><tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr><tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr><tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr><tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr></table>	DVS	SNS	LSB	set dividing number (N)	Actual dividing	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	0	1	AMIN	2 to 40MHz	0	0	AMIN	0.5 to 10MHz	
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No.	Control block data	Description	Related data																																																																																					
(2)	Reference divider data R0 to R3	- Reference frequency (fref) selection data <table><tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr></table> * PLL INHIBIT - The programmable divider and IF counter stop, with FMIN, AMIN, HCTR and LCTR inputs being in the pull-down condition (GND), and the charge pump has the high impedance.	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC	1	1	1	1	PLL INHIBIT	
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1	1	1	0	PLL INHIBIT+X'tal OSC																																																																																				
1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data CTE GT0, GT1	- IF counter counting start data CTE = 1 : Counting start = 0 : Counting start - Determines the counting time of universal counter <table><tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr><tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr><tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr><tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr><tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr></table>	GT1	GT0	Counting time	Wait time	0	0	4ms	3 to 4ms	0	1	8ms	3 to 4ms	1	0	16ms	3 to 4ms	1	1	32ms	3 to 4ms	IFS																																																																	
GT1	GT0	Counting time	Wait time																																																																																					
0	0	4ms	3 to 4ms																																																																																					
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1	0	16ms	3 to 4ms																																																																																					
1	1	32ms	3 to 4ms																																																																																					
(4)	MUTE control data IFSW	Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0 : at receiving 1 : MUTE																																																																																						
(5)	FM/AM BAND selection control data BDSW	Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0 : AM 1 : FM																																																																																						

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No.	Control block data	Description	Related data																																				
(6)	DO pin control data DOC0 DOC1 DOC2	• Data to control DO pin output <table><thead><tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>end-UC (See the item with asterisk below)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Low when SDON</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Low when stereo</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr></tbody></table> • The open condition is selected at power ON/reset. * IF counter counting end check DO pin ① Counting start ② Counting end ③ CE : HI ① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically. ② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made. ③ DO pin opens when serial data is entered/output (CE pin : Hi) Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL pin signal, regardless of DO pin control data (DOC).	DOC2	DOC1	DOC0	DO pin condition	0	0	0	Open	0	0	1	Low when unlock is detected.	0	1	0	end-UC (See the item with asterisk below)	0	1	1	Open	1	0	0	Open	1	0	1	Low when SDON	1	1	0	Low when stereo	1	1	1	Open	UL0, UL1 CTE
DOC2	DOC1	DOC0	DO pin condition																																				
0	0	0	Open																																				
0	0	1	Low when unlock is detected.																																				
0	1	0	end-UC (See the item with asterisk below)																																				
0	1	1	Open																																				
1	0	0	Open																																				
1	0	1	Low when SDON																																				
1	1	0	Low when stereo																																				
1	1	1	Open																																				
(7)	Unlock detection data UL0, UL1	• Phase error (φE) detection width selection data to judge if PLL is locked. Phase error exceeding the detection width is judged to mean that PLL is locked (* : don't care) <table><thead><tr><th>UL1</th><th>UL0</th><th>φE Detection width</th><th>Detection output</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of φE</td></tr><tr><td>1</td><td>*</td><td>±6.67μs</td><td>φE extended by 1 to 2 ms</td></tr></tbody></table> * DO pin is LOW. Serial data output : UL = 0.	UL1	UL0	φE Detection width	Detection output	0	0	Stop	Open	0	1	0	Direct output of φE	1	*	±6.67μs	φE extended by 1 to 2 ms	DOC0 DOC1 DOC2																				
UL1	UL0	φE Detection width	Detection output																																				
0	0	Stop	Open																																				
0	1	0	Direct output of φE																																				
1	*	±6.67μs	φE extended by 1 to 2 ms																																				
(8)	Phase comparator control data DZ0, DZ1	• Data to control the dead zone of phase comparator <table><thead><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></tbody></table> Dead zone width : DZA<DZB<DZC<DZD	DZ1	DZ0	Dead zone mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD																						
DZ1	DZ0	Dead zone mode																																					
0	0	DZA																																					
0	1	DZB																																					
1	0	DZC																																					
1	1	DZD																																					
(9)	Output port data BO	• Data to determine the output of output ports BO1 and BO2 "Data" = 0 : OPEN 1 : Low																																					
(10)	Charge pump control data DLC	• Data to enforce control of charge pump output <table><thead><tr><th>DLC</th><th>Charge pump output</th></tr></thead><tbody><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></tbody></table> * In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V_{CC}. (Dead lock clear circuit)	DLC	Charge pump output	0	Normal	1	Forced to LOW																															
DLC	Charge pump output																																						
0	Normal																																						
1	Forced to LOW																																						
(11)	IFS	• Normally, set Data = 1. Setting Data = 0 causes the input sensitivity worsening mode and the sensitivity decreases by about 10 to 30mVrms.																																					
(12)	LSI test data TEST0 to 2	• LSI test data TEST0 TEST1 TEST2 All to be set to "0" All set to zero at power ON/reset																																					
(13)	DNC	• Set data = 0.																																					

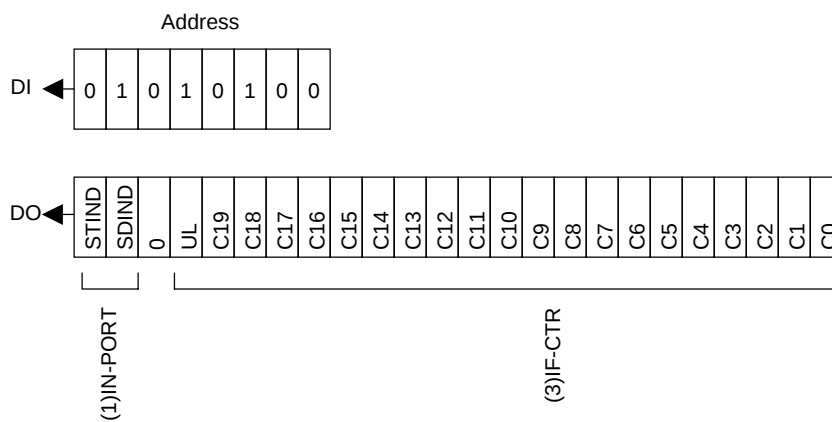
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No.	Control block data	Description	Related data
(14)	Forced monaural control data STSW	- Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0 : MONO 1 : STEREO	
(15)	SD sensitivity control data SDC	- Data to determine the output of output ports SDC, controlling the SD sensitivity "Data" = SDC0 : 0, SDC1 : 0 → SD sensitivity 1 = 50dBμV (Typ) SDC0 : 0, SDC1 : 1 → SD sensitivity 2 = 52dBμV (Typ) SDC0 : 1, SDC1 : 0 → SD sensitivity 3 = 57dBμV (Typ) SDC0 : 1, SDC1 : 1 → SD sensitivity 4 = 62dBμV (Typ) * Above data values indicate the difference of SD sensitivity levels and are reference values.	

DO control data (serial data output) composition

(1) OUT mode



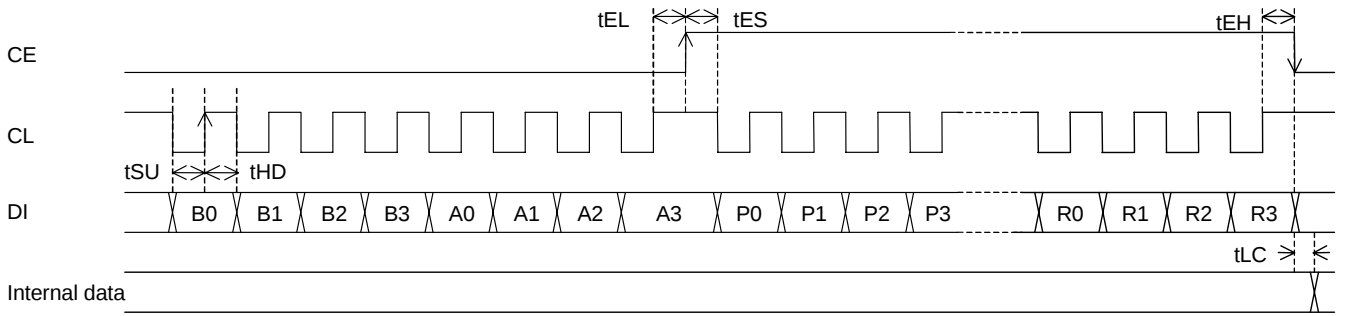
Description of DO output data

No.	Control block data	Description	Related data
(1)	Stereo and SD indicators control data STIND, SDIND	- Data latching stereo and SD indicator conditions. - Latching made in the data output (OUT) mode. - SDIND←Stereo indicator condition 0 : ST ON, 1 : ST OFF - STIND←SD indicator condition 0 : SD ON, 1 : SD OFF	
(2)	PLL unlock data UL	- Data latching the content of unlock detection circuit - UL←0 : At unlock 1 : At lock or in the detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	- Data latching the content of IF counter (20-bit binary counter) - C19←MSB of binary counter - C0 ←LSB of binary counter	CTE GT0 GT1

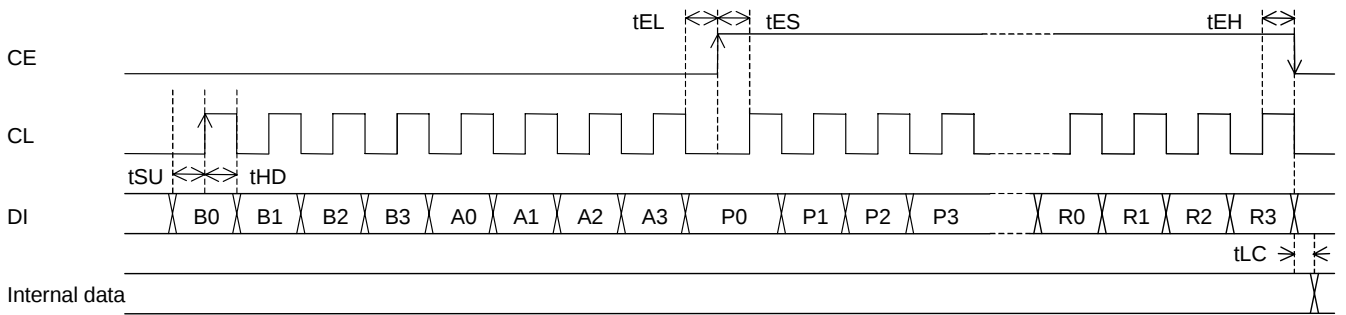
LV23200T

Serial data input (IN1/IN2) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75\mu s$ $t_{LC} < 0.75\mu s$

CL : Normally Hi

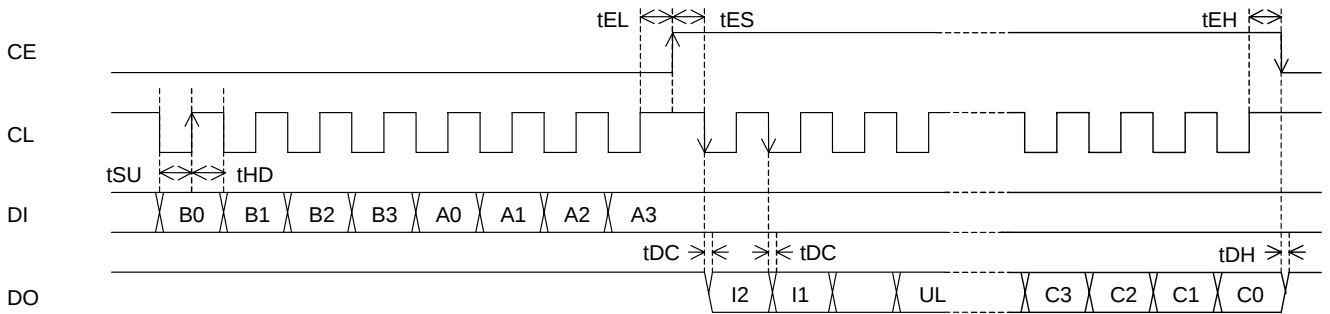


CL : Normally Low

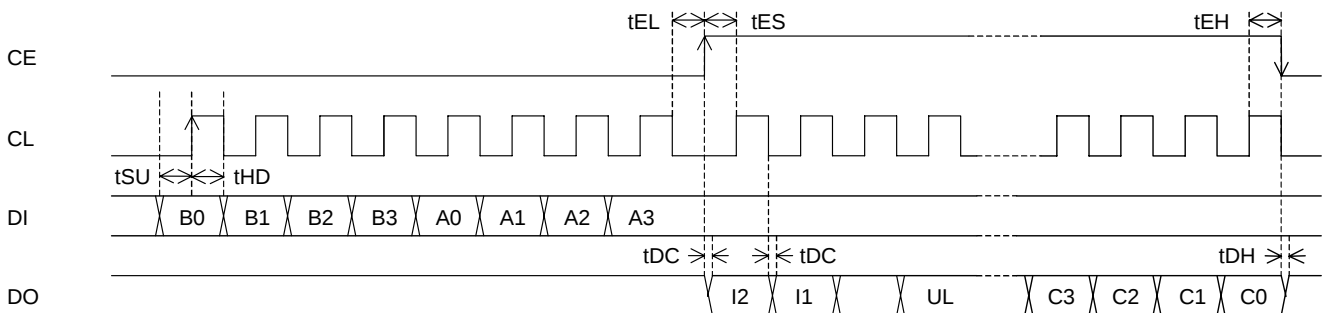


Serial data output (OUT) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75\mu s$ t_{DC} , $t_{DH} < 0.35\mu s$

CL : Normally Hi

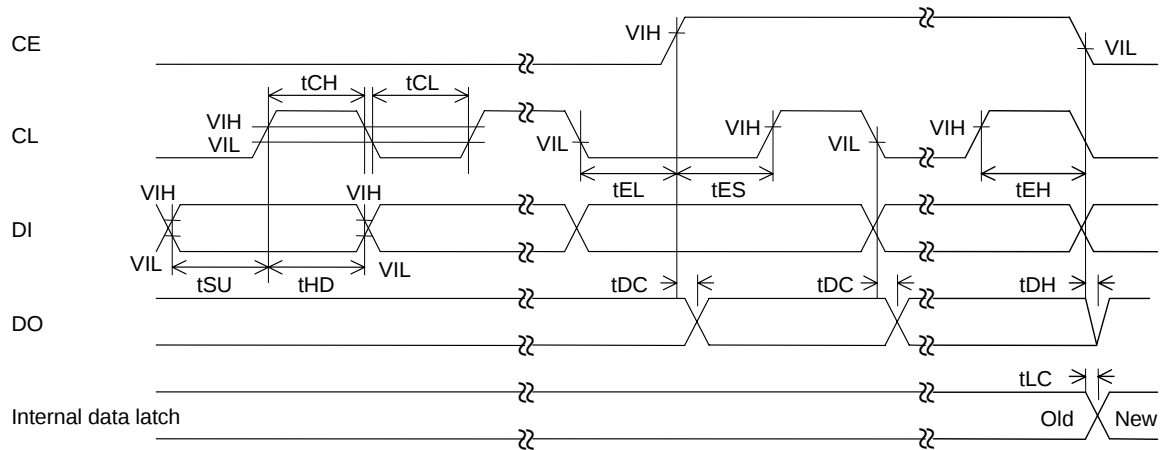


CL : Normally Low

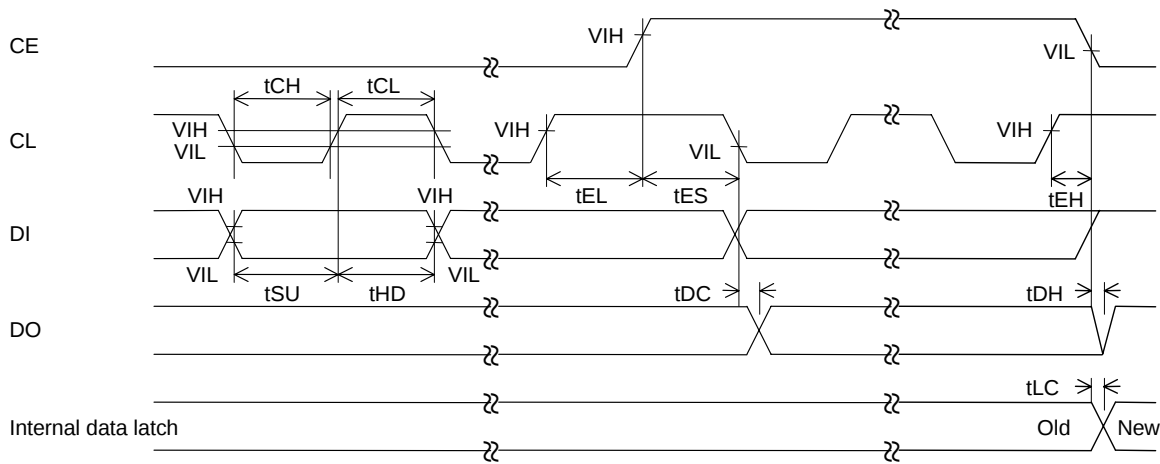


(Note) DO pin is an Nch open drain pin, so that the data varying time (t_{DC} and t_{DH}) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



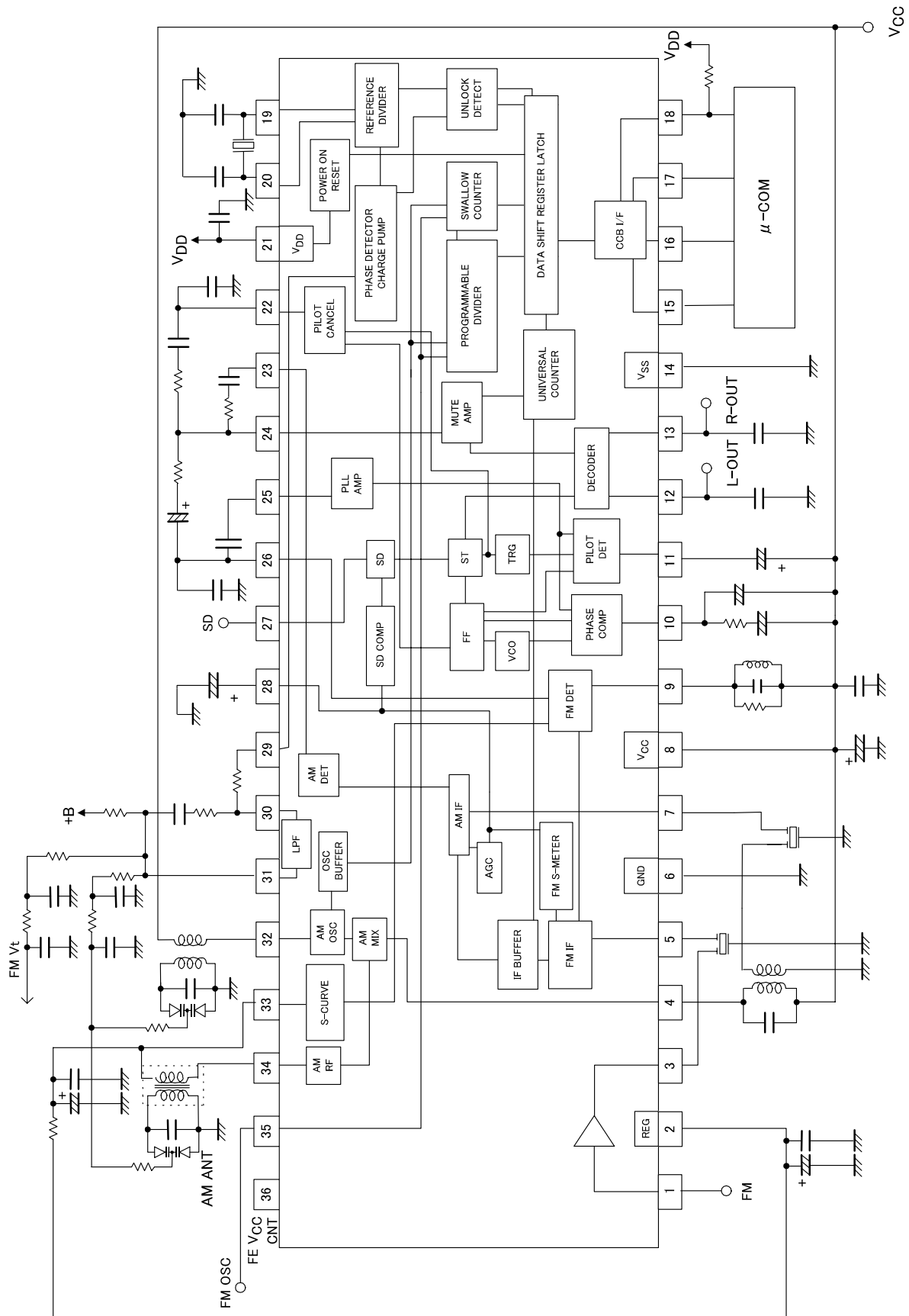
<< When CL stops at the "L" level >>



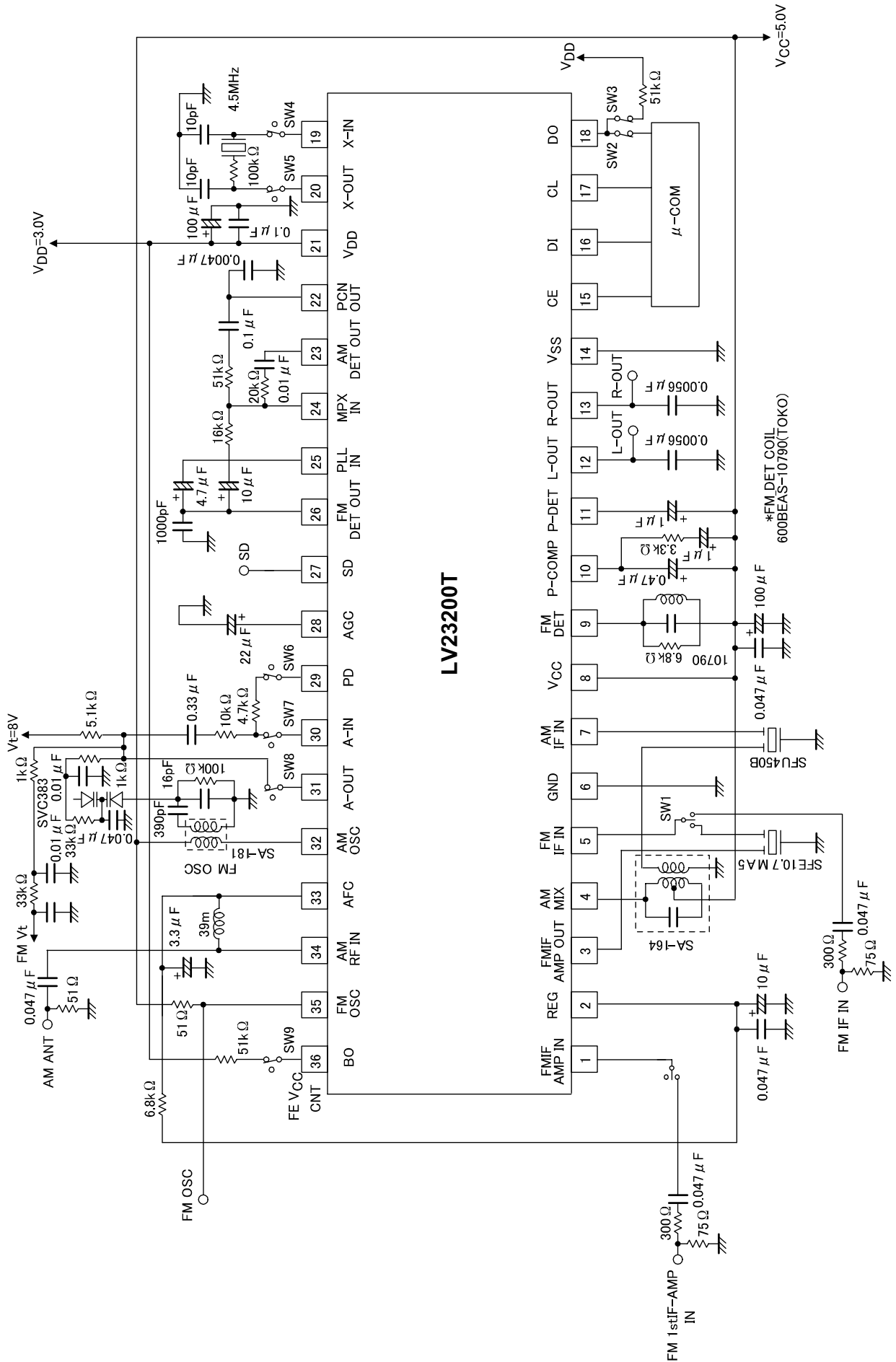
<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	tEH	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					

Block Diagram



Test Circuit



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