Signetics

FAST 74F322
Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	125 MHz	60mA

FAST Products

FEATURES

- **Multiplexed parallel I/O ports**
- **Separate serial input and output**
- **Sign extend function**
- **3-state outputs for bus applications**
- **Direct Overriding Clear**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F322N
20-Pin Plastic SOL	N74F322D

DESCRIPTION

The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

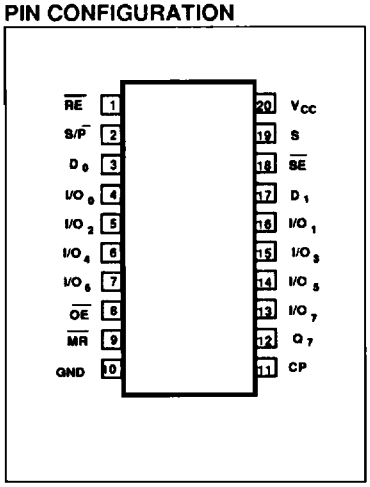
The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A Low signal on $\overline{RE}$ enables shifting or parallel loading, while a High signal enables the hold mode. A High signal on S/$\overline{P}$ enables shift right, while a Low signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a High signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A Low signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents thus performing the sign extend function. A High signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

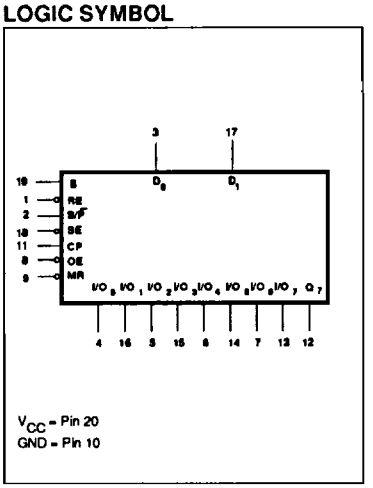
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Serial data inputs	1.0/1.0	20µA/0.6mA
S	Serial data select input	1.0/2.0	20µA/1.2mA
$\overline{SE}$	Sign Extend input	1.0/3.0	20µA/1.8mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
S/$\overline{P}$	Serial (High) or Parallel (Low) mode control input	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Register Enable input (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_7	Bi-state serial output	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

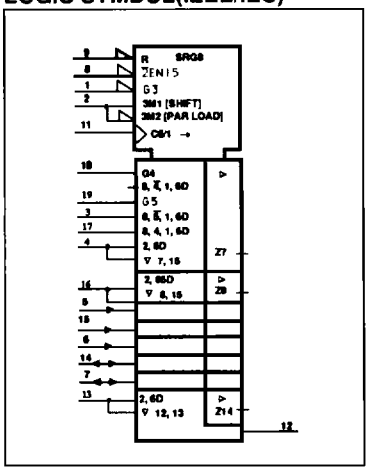
PIN CONFIGURATION



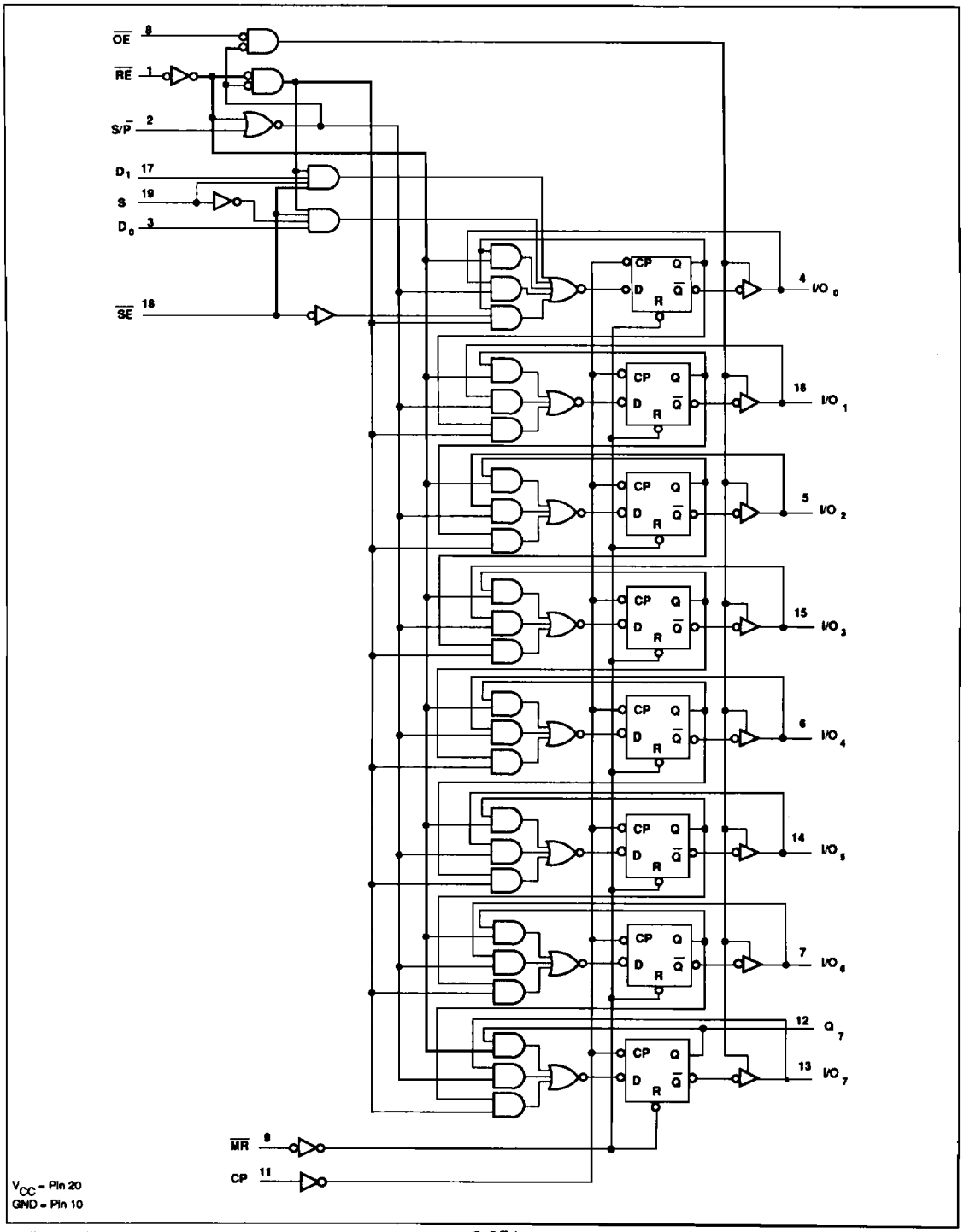
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS									OPERATING MODE
$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	Q_7	
L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L	Clear
L	X	H	X	X	L	X	L	L	L	L	L	L	L	L	L	
H	L	L	X	X	X	↑	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_7	Parallel load
H	L	H	H	L	L	↑	D_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Shift right
H	L	H	H	H	L	↑	D_1	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	
H	L	H	L	X	L	↑	O_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Sign extend
H	H	X	X	X	L	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
X	L	L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	NC	3-State
X	X	X	X	X	H	↕	Z	Z	Z	Z	Z	Z	Z	Z	NC	

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
I_0-I_7 = The level of the steady state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_7) are isolated from the I/O terminal.
D_0-D_7 = The level of the steady state inputs to the serial multiplexer input.
O_0-O_7 = The level of the respective Q_n flip-flop prior to the last clock Low-to-High transition.
* = When the input is High, all I/O terminals are at the high impedance state, sequential operation or clearing of the register is not affected.
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
		S						-1.2	mA
		others						-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	75	mA
		I_{CCL}					60	90	mA
		I_{CCZ}					65	95	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

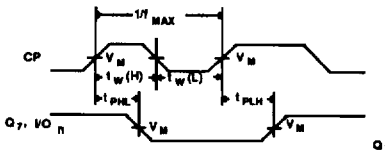
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 4.5	6.0 7.0	9.0 9.5	4.0 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	4.5 5.0	6.5 6.5	9.0 9.0	4.5 5.0	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.0 5.5	5.0 7.5	8.0 10.5	3.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.0 1.0	4.0 2.5	6.5 5.5	2.0 1.0	7.5 6.0	ns
t_{PZH} t_{PZL}	Output Enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 6.0	6.0 8.0	9.0 11.0	3.5 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 2.0	6.0 4.0	9.0 7.0	3.5 2.0	10.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	8.0 9.0	9.5 11.0	12.5 14.0	7.0 8.0	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	6.5 4.5	8.5 6.5	11.5 9.5	5.5 4.0	13.0 10.5	ns

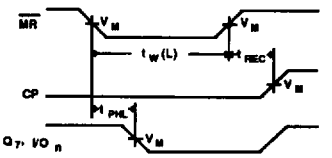
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{RE}$ to CP	Waveform 3	8.0 12.5			9.5 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{RE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	4.0 4.5			6.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SE}$ to CP	Waveform 3	5.5 5.0			7.0 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S/$\overline{P}$ to CP	Waveform 3	10.5 9.5			11.0 10.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 3	4.0 8.5			4.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S or S/$\overline{P}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

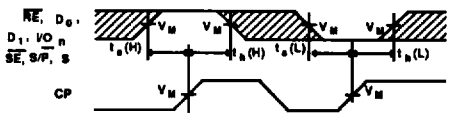
AC WAVEFORMS



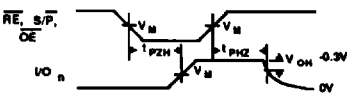
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



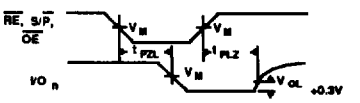
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

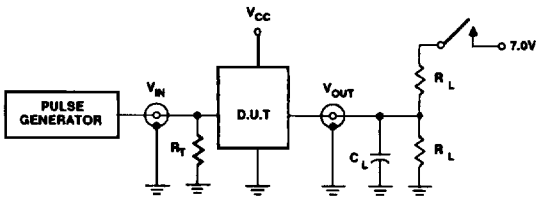


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

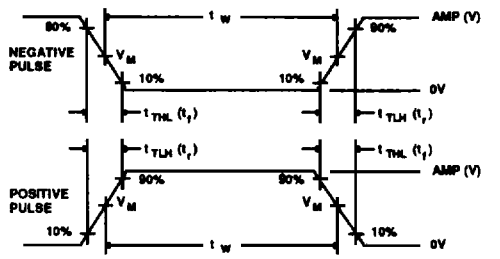
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns