

DN74LS109 *N74LS109*

Dual J-K̄ Positive Edge-Triggered Flip-Flops (with Set and Reset)

Description

DN74LS109 contains two positive-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

Features

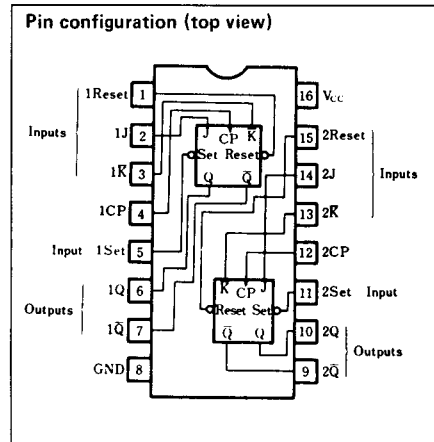
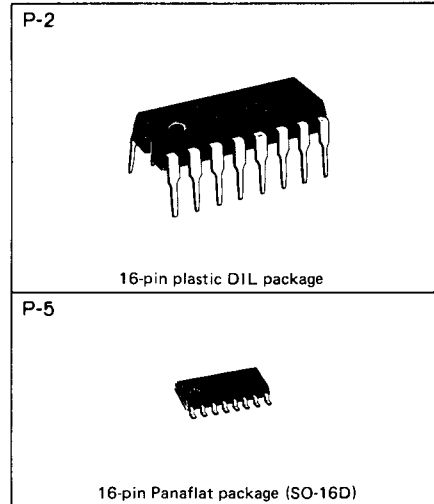
- Positive-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set and reset inputs
- J and K inputs
- Q and \bar{Q} outputs
- Wide operating temperature range ($T_a = -20$ to $+75^\circ\text{C}$)

Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	\bar{K}	Q	\bar{Q}
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	×	×	Q_0	\bar{Q}_0

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↑: Change from LOW to HIGH.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0 : Q level prior to determination of input condition shown in table.
6. \bar{Q}_0 : \bar{Q} level prior to determination of input condition shown in table.
7. Toggle: With ↑ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and \bar{Q} are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and \bar{Q} cannot be predicted.



Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			-400	μA
	I_{OL}			8	mA
Operating temperature range	T_{opr}	-20	25	75	$^\circ\text{C}$
Clock frequency	f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	25		ns
	Set or Reset Low	t_w	25		ns
Set-up time	HIGH data	t_{su}	20 ↑		ns
	LOW data	t_{su}	20 ↑		ns
Hold time	t_h	5 ↑			ns

Notes 1. ↑: Indicates rise edge of standard clock pulse.

■ DC characteristics (Ta = -20 ~ +75°C)

Parameter	Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage	V _{IH}		2.0			V
	V _{IL}				0.8	V
Output voltage	V _{OH}	V _{CC} = 4.75V, V _{IH} = 2V V _{IL} = 0.8V, I _{OH} = -400 μA	2.7	3.4		V
	V _{OL1}	V _{CC} = 4.75V V _{IH} = 2V V _{IL} = 0.8V		0.25	0.4	V
	V _{OL2}			0.35	0.5	V
Input current	J- \bar{K}	I _{IH} V _{CC} = 5.25V V _I = 2.7V			20	μA
	Reset				40	μA
	Set				40	μA
	Clock				20	μA
	J- \bar{K}	I _{IL} V _{CC} = 5.25V V _I = 0.4V			-0.4	mA
	Reset				-0.8	mA
	Set				-0.8	mA
	Clock				-0.4	mA
	J- \bar{K}	I _I V _{CC} = 5.25V V _I = 5.5V			0.1	mA
	Reset				0.2	mA
	Set				0.2	mA
	Clock				0.1	mA
Output short circuit current**	I _{OS}	V _{CC} = 5.25V, V _O = 0V	-15		-100	mA
Input clamp voltage	V _{IK}	V _{CC} = 4.75V I _I = -18mA			-1.5	V
Supply current***	I _{CC}	V _{CC} = 5.25V		4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** Measured with all outputs open, Q and \bar{Q} outputs alternately HIGH, and clock inputs grounded.

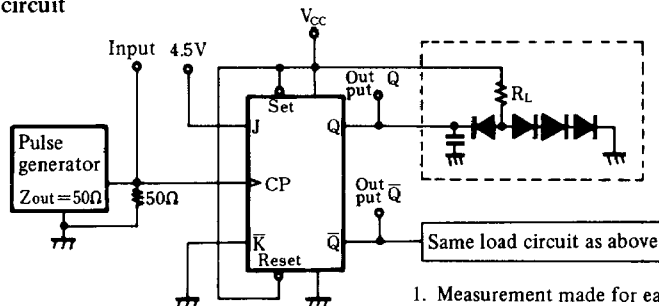
■ Switching characteristics (V_{CC} = 5V, Ta = 25°C)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit	
Maximum clock frequency	f _{max}			C _L = 15pF R _L = 2kΩ	25	33		MHz	
Propagation delay time	t _{PLH}	Reset Set Clock	Q, \bar{Q}				13	25	ns
	t _{PHL}					25	40		ns

※ Switching parameter measurement information

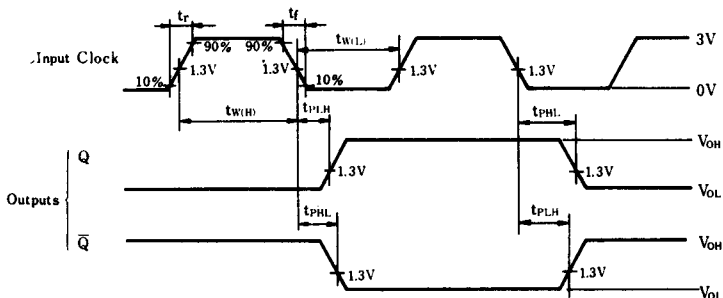
[1] f_{max}, t_{PLH}, t_{PHL} (Clock → Q, \bar{Q})

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms

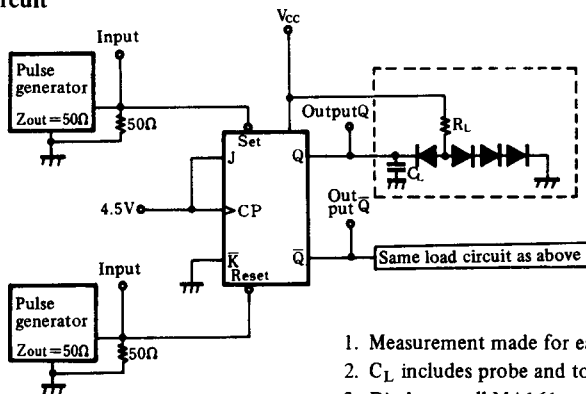


Notes

1. Clock input waveform: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, $\text{PRR}=1\text{MHz}$, duty cycle 50%
2. When measuring t_{max} , t_r and $t_f \leq 2.5\text{ns}$.

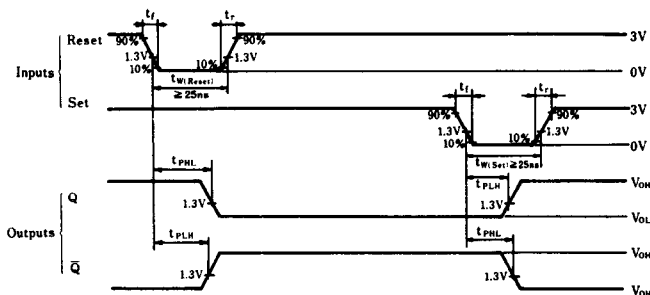
[2] t_{PLH} , $t_{\text{PHL}}(\text{Reset, Set} \rightarrow \text{Q, } \bar{\text{Q}})$

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

2. Waveforms



Notes

1. Set and clock waveforms: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, $\text{PRR} = 1\text{MHz}$.