FAIRCHILD SEMICONDUCTOR®

May 2004

RMBA19500

PCS 2 Watt Linear GaAs MMIC Power Amplifier

General Description

The RMBA19500 is a highly linear Power Amplifier. The circuit uses our pHEMT process. It has been designed for use as a driver stage for PCS base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for CDMA operation.

Features

- 2 Watt Linear output power at 36dBc ACPR1 for CDMA operation
- Small signal gain of 30dB typ.
- Small outline SMD package

Device

Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Drain Supply Voltage[1]	+10	V
Vg	Gate Supply Voltage	-5	V
P_{RF}	RF Input Power (from 50Ω source)	+5	dBm
T_C	Operating Case Temperature Range	-30 to +85	°C
T_S	Storage Temperature Range	-40 to +100	°C

Note:
1. Only under quiescent conditions—no RF applied.

Electrical Characteristics[2]

Parameter	Min	Typ	Max	Units
Frequency Range	1930		1990	MHz
Gain (Small Signal) Over 1930–1990MHz		30		dB
Gain Variation: Over Frequency Range Over Temperature Range		 ±1.0 ±1.5		 dB dB
Noise Figure		6		dB
Linear Output Power: for CDMA[3]	33			dBm
OIP3[4]		43		dBm
PAE @ 33dBm Pout		24		%
Input VSWR (50Ω)		2:1		
Drain Voltage (Vdd)		7.0		V
Gate Voltage (VG1, 2 and VG3)[5]	-2		-0.25	V
Quiescent Currents ($I_{DQ1, 2}$ and I_{DQ3})[5]		180, 445		mA
Thermal Resistance (Channel to Case) R_{JC}		11		°C/W

Notes:

2. V_{DD} = 7.0V, T_C = 25°C. Part mounted on evaluation board with input and output matching to 50Ω.
3. 9 Channel Forward Link QPSK Source; 1.23Mbps modulation rate. CDMA ACPR1 is measured using the ratio of the average power within the 1.23MHz channel at band center to the average power within a 30KHz bandwidth at an 885KHz offset. Minimum CDMA output power is met with ACPR1 > 36dBc.
4. OIP3 specifications are achieved for power output levels of 27 and 30dBm per tone with tone spacing of 1.25MHz at band-center with adjusted supply and bias conditions of Vdd = 6.5V and IdqTotal = 625mA (see Note 5).
5. VG1,2 and VG3 must be individually adjusted to achieve IDQ1,2 and IDQ3. A single VGG bias supply adjusted to achieve IDQTOTAL = 625mA can be used with nearly equivalent performance. Values for IDQ1,2 and IDQ3 shown have been optimized for CDMA operation. IDQ1, 2 and IDQ3 (or IDQTOTAL) can be adjusted to optimize the linearity of the amplifier for other modulation systems.

The device requires external input and output matching to 50Ω as shown in Figure 3 and the Parts List.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

The following describes a procedure for evaluating the RMBA19500, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for PCS Base station or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. The RMBA19500 requires external passive components for DC bias and RF input and output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the three stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of Figure 3. The following designations should be noted:

(1) Pin designations are as shown in Figure 2.

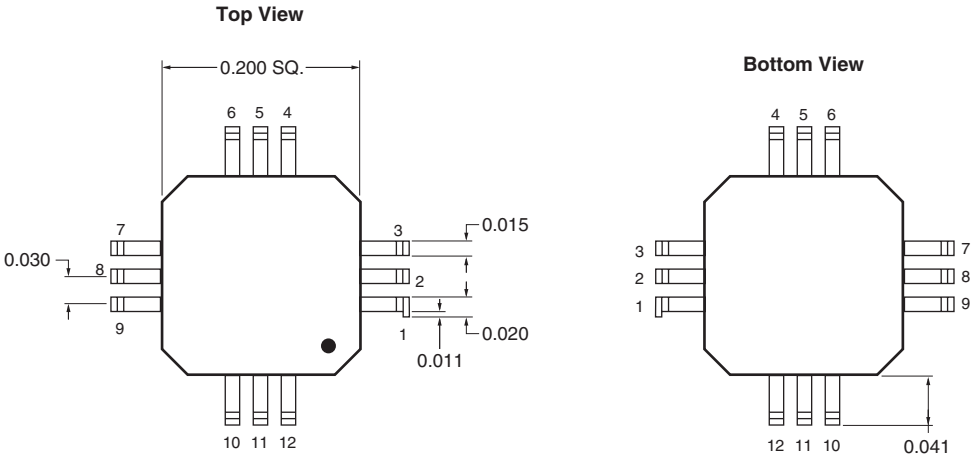
(2) Vg1, Vg2, and Vg3 are the Gate Voltages (negative) applied at the pins of the package.

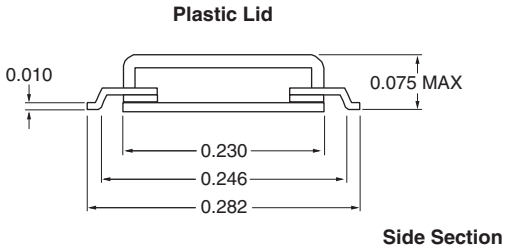
(3) Vgg1, Vgg2 and Vgg3 are the negative supply voltages at the evaluation board terminals (Vg1 and Vg2 are tied together).

(4) Vd1, Vd2 and Vd3 are the Drain Voltages (positive) applied at the pins of the package.

(5) Vdd is the positive supply voltage at the evaluation board terminal (Vd1, Vd2, and Vd3 are tied together).

Note: The base of the package must be soldered on to a heat sink for proper operation.





Dimensions in inches

Pin	Description
1	RF Out & Vd3
2	RF Out & Vd3
3	RF Out & Vd3
4	VD1
5	GND
6	VG1
7	RF In
8	GND
9	VG2
10	VD2
11	GND
12	VG3
13	GND

Figure 1. 12 Lead Plastic Air Cavity Package with Integral Heat Sink

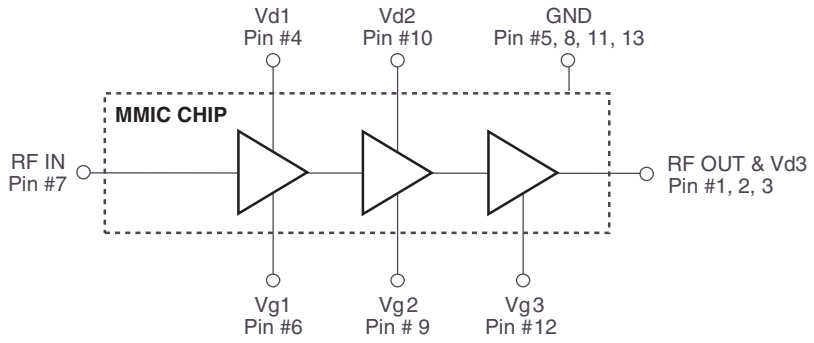


Figure 2. Functional Block Diagram of Packaged Product

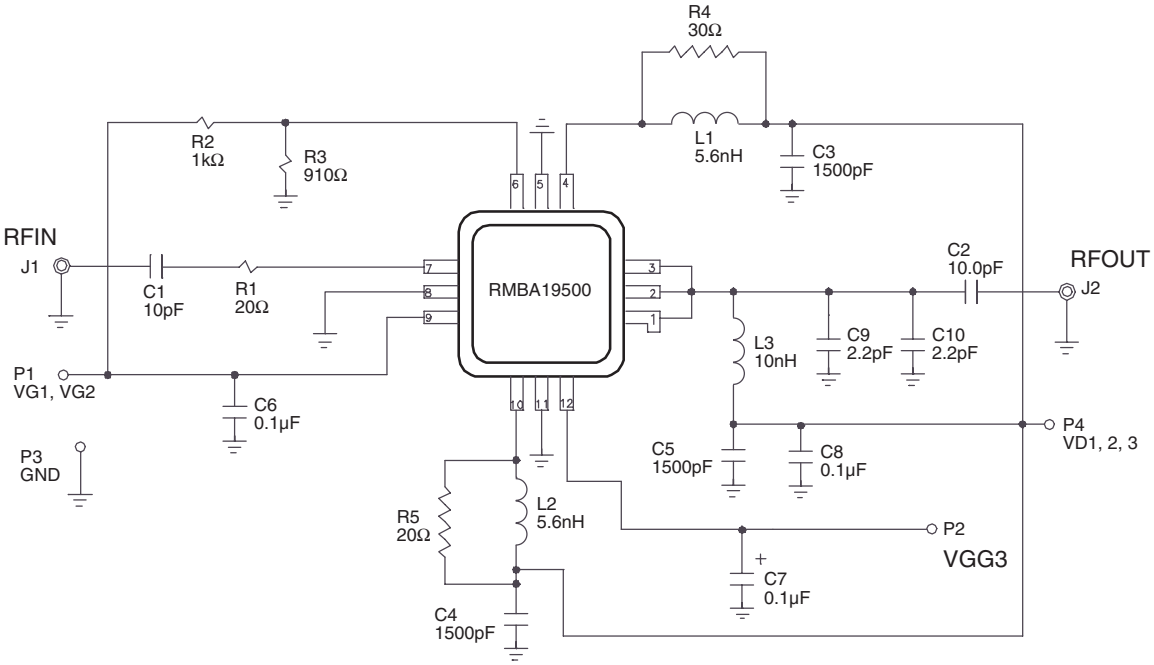


Figure 3. Schematic of Application Circuit Showing External Components

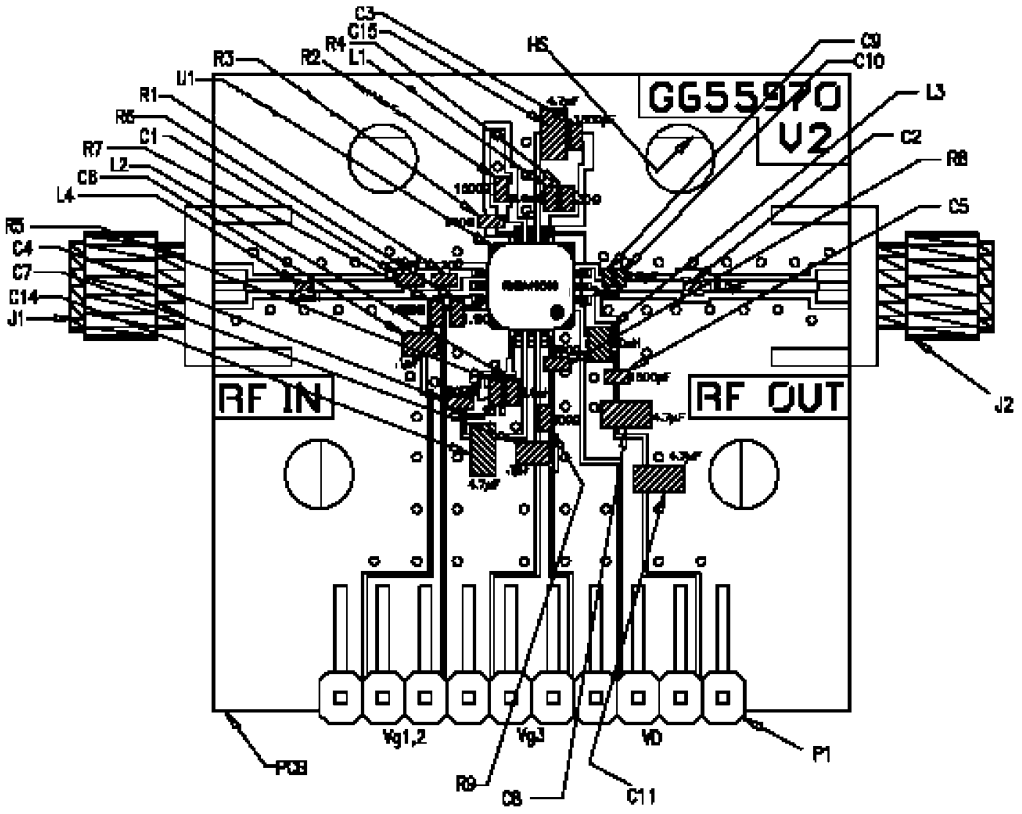


Figure 4. Layout of Test Evaluation Board (RMBA19500-TD, G655971)

Test Procedure for the Evaluation Board (RMBA19500-TB)

CAUTION: LOSS OF GATE VOLTAGES (Vg1, Vg2, Vg3) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA19500.)

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Set Vgg1, Vgg2 and Vgg3 to -3V (pinch-off).

Step 3: Slowly apply drain supply voltages of +7V to the board terminal Vdd ensuring that there is no short.

Step 4: Adjust Vgg12 up from -3V until the drain current (with no RF applied) increases to Idq12 as per supplied result sheet. Then adjust Vgg3 until the total drain current becomes equal to the sum of Idq12 and Idq3.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 6: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltage Vdd.

(iii) Turn down and off gate voltages Vgg1, Vgg 2 and Vgg3.

Parts List for Test Evaluation Board (RMBA19500-TB, G6655917)

Part	Value	Size (EIA)	Vendor(s)
L1, L2, L4	5.6nH	.06" x .03"	Toko (LL1608-F5N6)
L3	10nH	.085" x .060"	Coilcraft (0805HT-10NTKBC)
C1	10pF	.067" x .036"	Murata (GRM39COG100J050AD)
C9	2.2pF	.042" x .022"	Murata (GRM36COG2R2J050BD)
C3, C4, C5	1500pF	.067" x .036"	Murata (GRM39Y5V152Z50V)
C10	2.0pF		Murata (GRM36COG2R20J050BD)
C2	15.0pF	.042" x .022"	Murata (GRM36COG150J050)
C8, C11, C14, C15	4.7µF	.134" x .071"	TDK (C3216XR1A475KT)
C6, C7	0.1µF	.183" x .054"	Murata (GRM39Y5V104Z50)
R1, R5	20Ω	.069" x .037"	IMS (RCI-0603-20R0J)
R2, R7	1000Ω	.069" x .037"	IMS (RCI-0603-1001J)
R3	910Ω	.069" x .037"	IMS (RCI-0603-9100J)
R4	30Ω	.069" x .037"	IMS (RCI-0603-30R0J)
R6	1.1KΩ	.069" x .037"	IMS (RCI-0603-1101J)
R8	390Ω		IMS (RCI-0603-3900J)
R9	300Ω		IMS (RCI-0603-3000J)
U1	RMBA19500	.31" x .41"	Fairchild
HS	Heatsink		Fairchild, G655548
P1	Terminals		3M (2340-5211TN)
J1, J2	SMA Connectors		E.F. Johnson (142-0701-841)
Board FR4			Fairchild Dwg# G654187/G654941

Thermal Considerations for Heat Sinking the RMBA19500

The PWB must be prepared with either an embedded copper slug in the board where the package is to be mounted or a heat sink should be attached to the backside of the PWB where the package is to be mounted on the front side. The slug or the heat sink should be made of a highly electrically and thermally conductive material such as copper or aluminum. The slug should be at least the same thickness as the PWB. In the case of the heat sink, a small pedestal should protrude through a hole in the PWB where the package bottom is directly soldered. In either configuration, the top surface of the slug or the pedestal should be made coplanar with the package lead mounting plane i.e., the top surface of the PWB. Use Sn96 solder (96.5% Sn and 3.5% Ag) at 220°C for 20 seconds or less to attach the heat sink to the backside of the PWB. Then, using Sn63, the package bottom should be firmly soldered to the slug or the pedestal while the pins are soldered to the respective pads on the front side of the PWB without causing any stress on the pins. Remove flux completely if used for soldering.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	Power247™	SuperFET™
ActiveArray™	FASTr™	LittleFET™	PowerSaver™	SuperSOT™-3
Bottomless™	FPS™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
CoolFET™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
DOME™	GTO™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
EcoSPARK™	HiSeC™	MSX™	Quiet Series™	TINYOPTO™
E^2CMOS™	I^2C™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	*i-Lo*™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	µSerDes™	UltraFET®
FACT Quiet Series™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Across the board. Around the world.™		OPTOPLANAR™	SMART START™	
The Power Franchise®		PACMAN™	SPM™	
Programmable Active Droop™		POP™	Stealth™	

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.