ICS8537-01

HEX, LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-3.3V/2.5V LVPECL CLOCK BUFFER

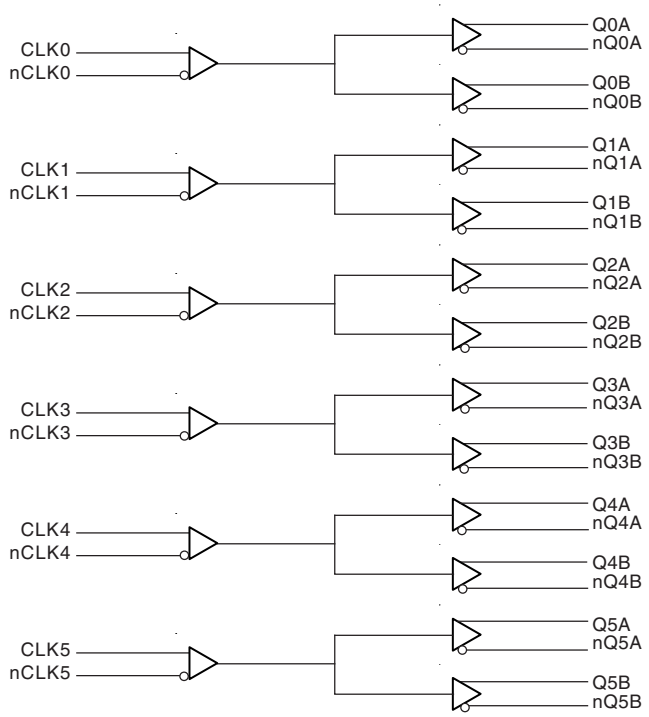
GENERAL DESCRIPTION

The ICS8537-01 is a Hex low skew, high performance 1-to-2 Differential-to-3.3V/2.5 LVPECL Clock Buffer. The ICS8537-01 has six selectable clock inputs. The CLKx, nCLKx pairs can accept most differential input levels and translate them to 3.3V or 2.5V LVPECL output levels.Guaranteed output and part-to-part skew specifications make the ICS8537-01 ideal for those applications demanding well defined performance and repeatability.

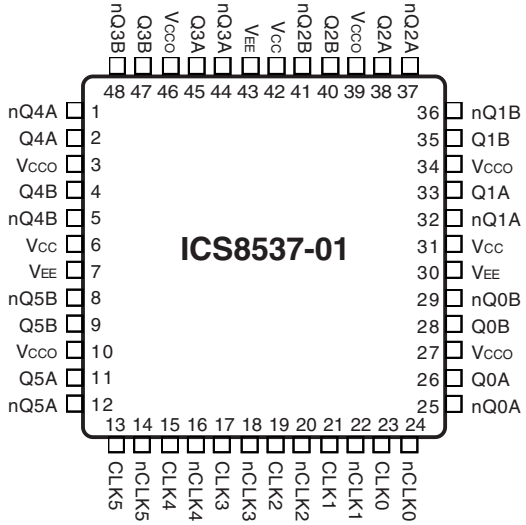
FEATURES

- Twelve LVPECL outputs
- Selectable differential CLKx, nCLKx inputs
- CLKx, nCLKx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVHSTL, SSTL, DCM) to LVPECL levels without external bias networks
- Translates any single-ended input signal to LVPECL with resistor bias on nCLKx input
- Output skew: 130ps (maximum)
- Bank skew: 20ps (maximum)
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 1.5ns (maximum)
- 3.3V or 2.5V operating supply
- 0°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ4A, Q4A	Output		Differential output pair. LVPECL interface levels.
3, 10, 27, 34, 39, 46	V_{CCO}	Power		Output supply pins.
4, 5	Q4B, nQ4B	Output		Differential output pair. LVPECL interface levels.
6, 31, 42	V_{CC}	Power		Core supply pins.
7, 30, 43	V_{EE}	Power		Negative supply pins.
8, 9	nQ5B, Q5B	Output		Differential output pair. LVPECL interface levels.
11, 12	Q5A, nQ5A	Output		Differential output pair. LVPECL interface levels.
13	CLK5	Input	Pullup	Inverting differential clock input.
14	nCLK5	Input	Pulldown	Non-inverting differential clock input.
15	CLK4	Input	Pullup	Non-inverting differential clock input.
16	nCLK4	Input	Pulldown	Inverting differential clock input.
17	CLK3	Input	Pullup	Non-inverting differential clock input.
18	nCLK3	Input	Pulldown	Inverting differential clock input.
19	CLK2	Input	Pullup	Non-inverting differential clock input.
20	nCLK2	Input	Pulldown	Inverting differential clock input.
21	CLK1	Input	Pullup	Non-inverting differential clock input.
22	nCLK1	Input	Pulldown	Inverting differential clock input.
23	CLK0	Input	Pullup	Non-inverting differential clock input.
24	nCLK0	Input	Pulldown	Inverting differential clock input.
25, 26	nQ0A, Q0A	Output		Differential output pair. LVPECL interface levels.
28, 29	Q0B, nQ0B	Output		Differential output pair. LVPECL interface levels.
32, 33	nQ1A, Q1A	Output		Differential output pair. LVPECL interface levels.
35, 36	Q1B, nQ1B	Output		Differential output pair. LVPECL interface levels.
37, 38	nQ2A, Q2A	Output		Differential output pair. LVPECL interface levels.
40, 41	Q2B, nQ2B	Output		Differential output pair. LVPECL interface levels.
44, 45	nQ3A, Q3A	Output		Differential output pair. LVPECL interface levels.
47, 48	Q3B, nQ3B	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLKx	nCLKx	Q0A:Q5A, Q0B:Q5B	nQ0A:nQ5A, nQ5B:nQ5B		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single ended levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, V_O	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 2.375V TO 3.465V, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				130	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 2.375V TO 3.465V, TA = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKx	$V_{IN} = V_{CC}$ = 3.465V			150	µA
		nCLKx	$V_{IN} = V_{CC}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLKx	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nCLKx	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended appliations, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 2.375V TO 3.465V, TA = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

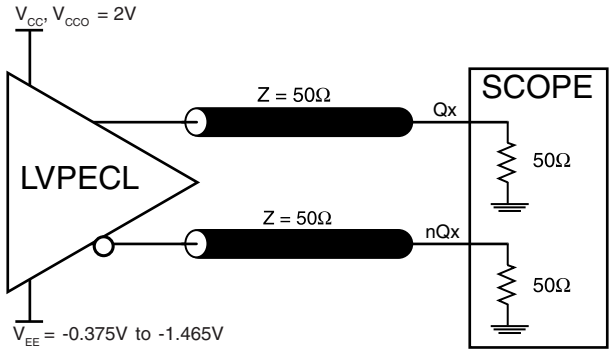
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 2.375V TO 3.465V, T_A = 0°C TO 85°C

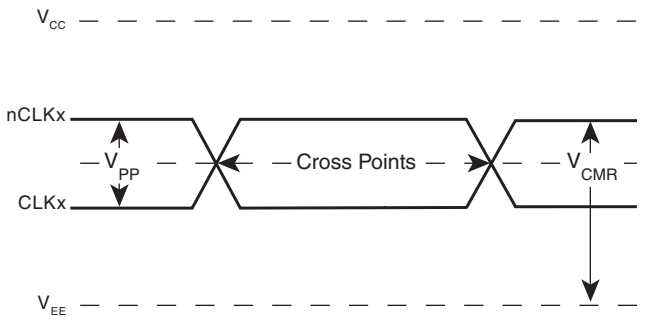
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 700MHz	1.1	1.3	1.5	ns
*t*sk(o)	Output Skew; NOTE 2, 5				130	ps
*t*sk(b)	Bank Skew; NOTE 3, 5				20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5				350	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle	$f \leq$ 300MHz	47		53	%
		$f >$ 300MHz, $f \leq$ 500MHz	45		55	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured from at the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 4: Defined as between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

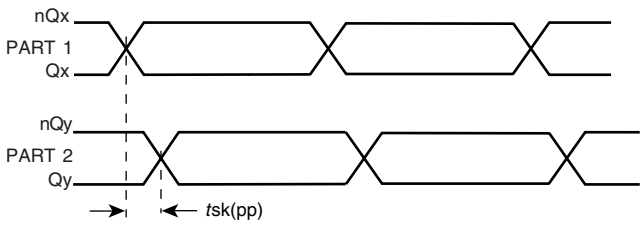
PARAMETER MEASUREMENT INFORMATION



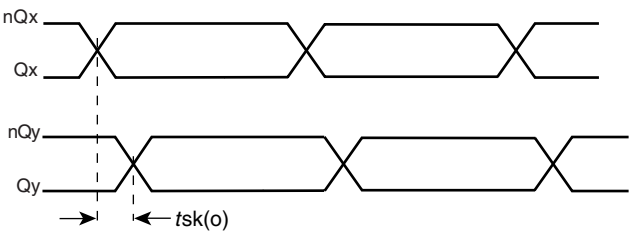
OUTPUT LOAD AC TEST CIRCUIT



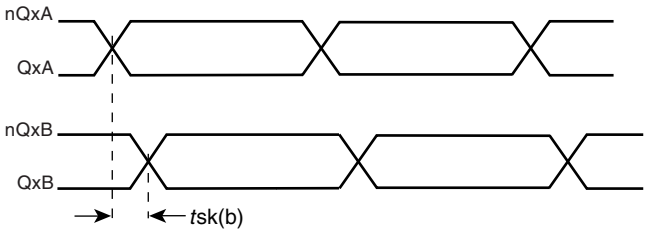
DIFFERENTIAL INPUT LEVEL



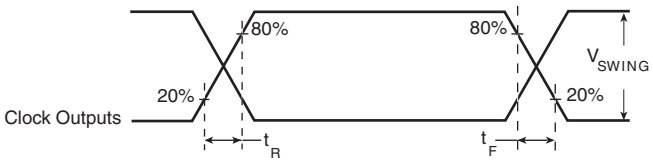
PART-TO-PART SKEW



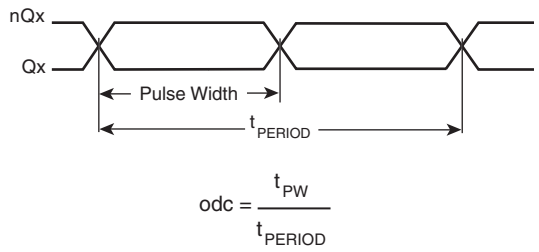
OUTPUT SKEW



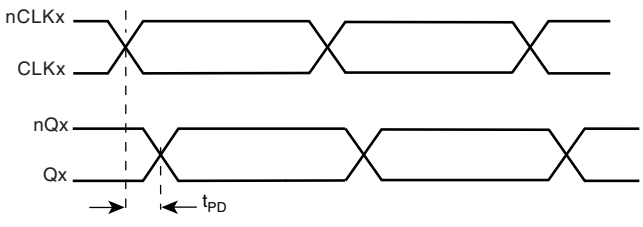
BANK SKEW



OUTPUT RISE/FALL TIME



odc & t_{PERIOD}



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

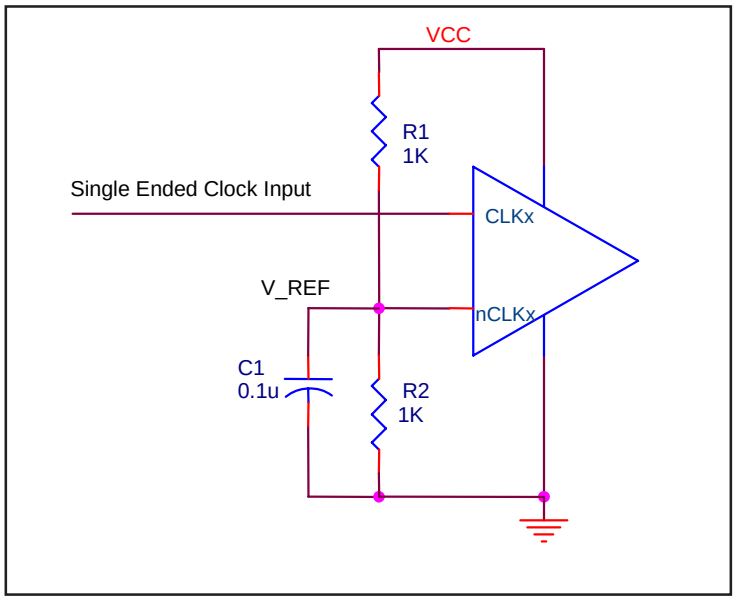


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

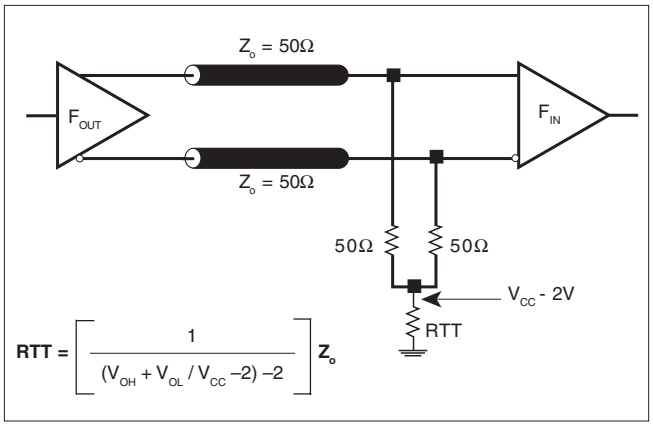


FIGURE 2A. LVPECL OUTPUT TERMINATION

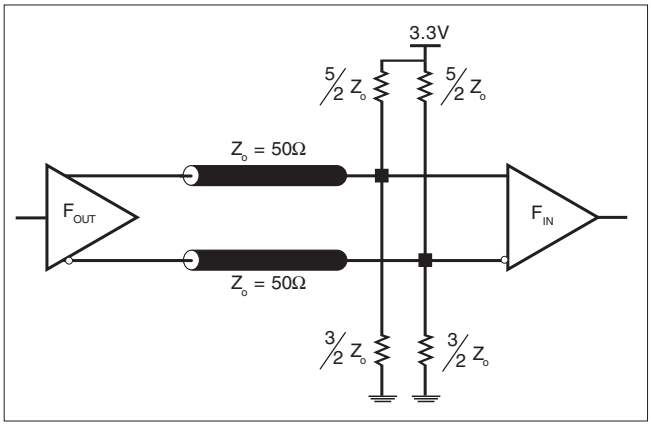


FIGURE 2B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8537-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8537-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 130mA = **450.5mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 12 * 30mW = **360mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 450.5mW + 360mW = **810.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.811W * 42.1°C/W = 119.1°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 3.*

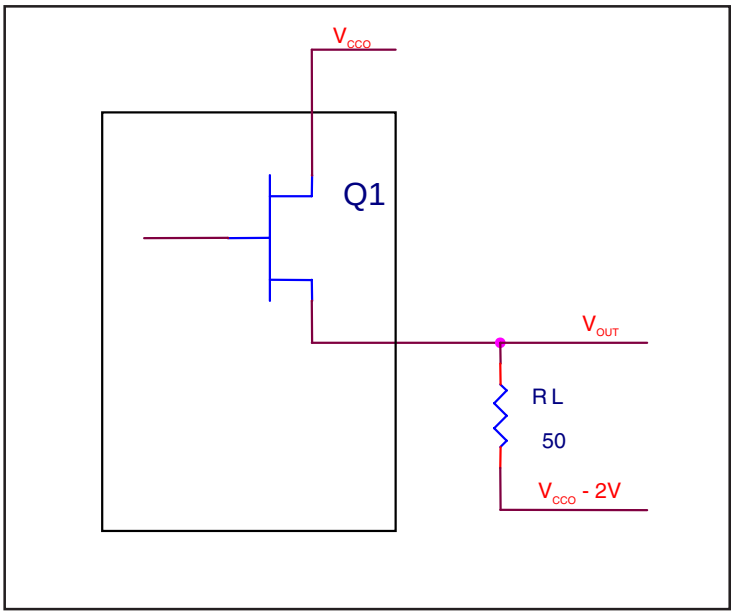


FIGURE 3. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8537-01 is: 1201

PACKAGE OUTLINE - Y SUFFIX

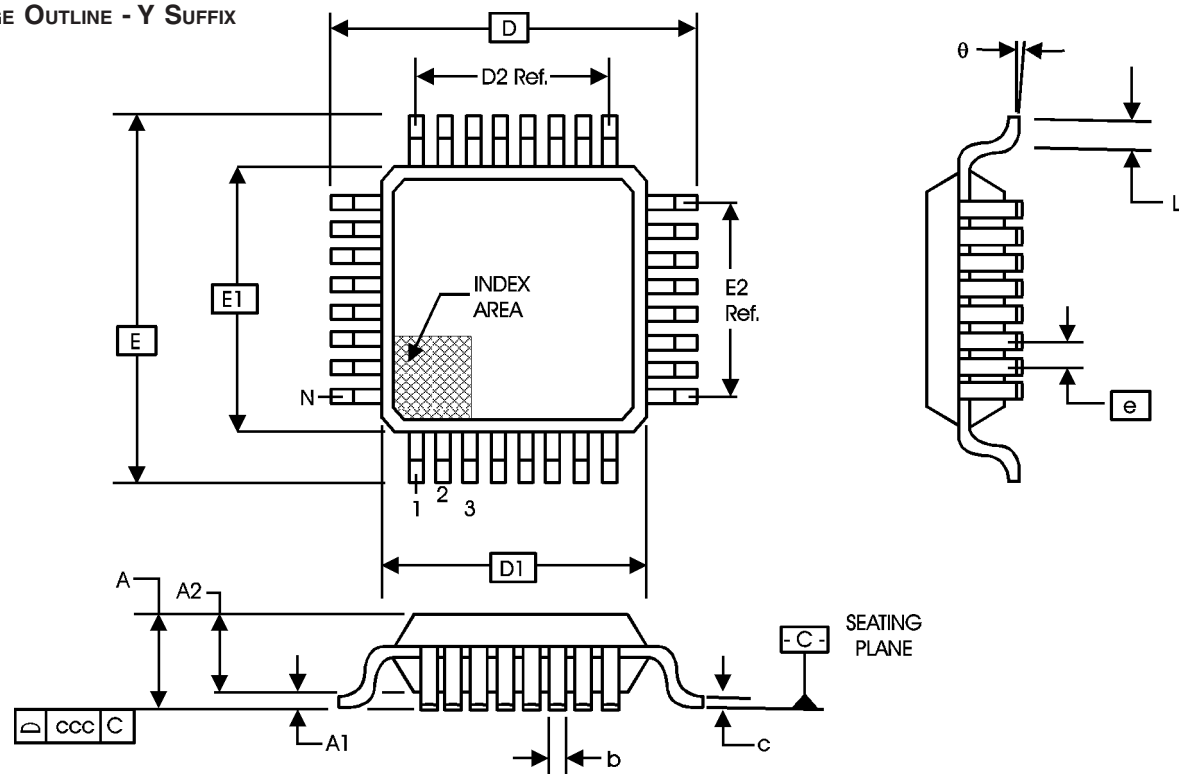


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8537AY-01	ICS8537AY-01	48 Lead LQFP	tray	0°C to 85°C
8537AY-01T	ICS8537AY-01	48 Lead LQFP	1000 tape & reel	0°C to 85°C
8537AY-01LF	ICS8537AY01L	Lead-Free, 48 Lead LQFP	tray	0°C to 85°C
8537AY-01LFT	ICS8537AY01L	Lead-Free, 48 Lead LQFP	1000 tape & reel	0°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B		1	Features Section - added lead-free bullet.	4/12/07
	T2	3	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical.	
	T4C	4	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V.	
		8 - 9	Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 3D.	
	T9	12	Ordering Information Table - added lead-free Part/Order Number, marking and note.	
B	T9	12 14	Updated datasheet's header/footer with IDT from ICS. Ordering Information Table - removed ICS prefix from Part/Order Number column. Added lead-free marking. Added Contact Page.	11/22/10

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