Am9338

8-Bit Multiple Port Register

inctive Characteristics:

word x 1 bit simultaneous read-write three ddress register.

ccess time of 48 ns typical.

lave enable allows scanning of memory contents.

- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded hermetic dual in-line or hermetic flat package

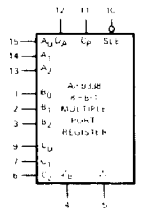
FUNCTIONAL DESCRIPTION

The Am9338 is a three-address eight-bit register organized as eight words of one bit per word. The register is designed for high-speed memory applications and is particularly suitable as the high-speed scratch pad memory in military and commercial three-address computers. Data can be written into one location and simultaneously read from any two locations.

The register is organized in a master slave arrangement where there are eight master latches and two slave latches. Data on the D_A input is stored in the master latch selected by the write address field A during the clock LOW time. Data from the eight masters is then selected by the two independent read address fields B, C and stored in the two slave latches during the clock HIGH time. This eight master two slave arrangement makes the register indistinguishable from an eight master eight slave system and allows both the two read addresses B and C and the write address A to be simultaneously applied to the register at the start of a clock cycle.

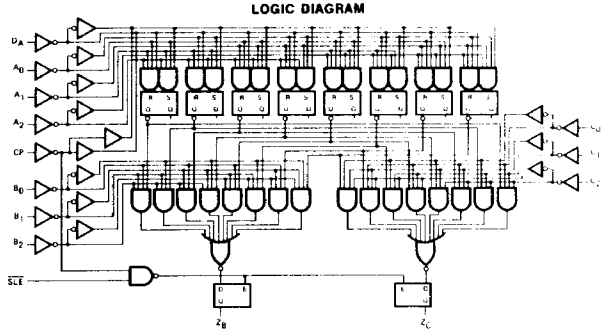
A slave enable is provided which if held LOW continuously enables the two slave latches and immediately transfers information from the master latches to the outputs so that the memory contents can be scanned asynchronously.

LOGIC SYMBOL



V = PIN 16
GND = PIN 8

LOGIC DIAGRAM



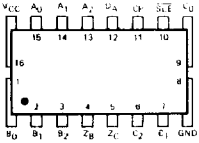
Am9338 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M933859X
Hermetic DIP	0°C to +75°C	U7B933859X
Hermetic DIP	−55°C to +125°C	U7B933851X
Hermetic Flat Pak	−55°C to +125°C	U4L933851X
Dice	Note	UXX9338XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM

Top View



NOTE: PIN 1 is marked for orientation

MAXIMUM R. **3S** (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93S658X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am93S861X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−10	−35	−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		64	99	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C) (V_{CC} = 5.0 V, C_L = 15 pF)

Parameters		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay CP to Output	$A_{0,1,2}$ = $B_{0,1,2}$ = $C_{0,1,2}$ $\overline{SLE}$ = H	12	24	42	ns
t_{pd-}	Turn On Delay CP to Output		10	19	40	ns
t_{pd+} (D_A-Z)	Turn Off Delay Data to Output	$\overline{SLE}$ = L, C_p = L	17	35	75	ns
t_{pd-} (D_A-Z)	Turn On Delay Data to Output		20	42	68	ns
t_{pd+} (B,C-Z)	Turn Off Delay Address to Output	C_p = H	13	26	43	ns
t_{pd-} (B,C-Z)	Turn On Delay Address to Output		24	48	81	ns
t_{sH} (D_A)	Set Up Time HIGH Data		7	15	23	ns
t_{sL} (D_A)	Set Up Time LOW Data		3	8	13	ns
t_s (A)	Set Up Time, Address Inputs		3	10	23	
CP_{pw} 'L'	Minimum LOW Clock Pulse Width			11	16	ns
CP_{pw} 'H'	Minimum HIGH Clock Pulse Width			10	15	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Input Current Versus Input Voltage $D_A A_0 A_1 A_2 C_0 C_1 C_2 B_0 B_1 B_2$

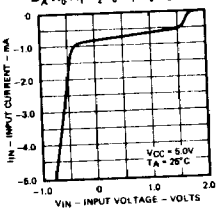


Figure 1

Input Current Versus Input Voltage $\overline{SLE}$

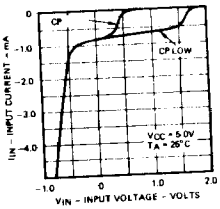


Figure 2

Output Current Versus Output Voltage Z_B and Z_C (Low State)

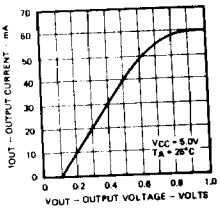


Figure 3

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

A_{0-2} Write address field. Data on D_A is written into the location specified by the A address field.

B_{0-2} Read address field. Data stored in the master latch specified by the B Read Address Field is transferred to the B slave latch and appears at the Z_B output when the clock pulse goes from a LOW logic level to a HIGH logic level.

C_{0-2} Read Address Field. Data stored in the master latch specified by the C Read Address Field is transferred to the C slave latch and appears at the Z_C output when the clock pulse goes from a LOW logic level to a HIGH logic level.

CP Clock Pulse. On going from a HIGH logic level to a LOW logic level the information on the D_A input is stored in the master latch specified by the Write A Address Field. When the clock pulse goes from a LOW logic level to a HIGH logic level information from the master latch or latches specified by the B and C Read Address Fields are stored in the two slave latches and appears at the outputs Z_B, Z_C.

D_A Information on the D_A input is written into the master latch specified by the A Address Field when the clock goes from a HIGH logic level to a LOW logic level.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T'L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

$\overline{SLE}$ Slave Enable. When LOW continuously allows information from the master latch addressed by the two read fields B, C to appear at the outputs Z_B, Z_C.

Z_B The B read address output.

Z_C The C read address output.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS

t_{pd+} The propagation delay from the clock input LOW to HIGH transition to the Z output LOW to HIGH transition. Refer to Figure 4.

t_{pd-} The propagation delay from the clock input HIGH to LOW transition to the Z output HIGH to LOW transition. Refer to Figure 4.

t_{sL} (D_A) The time required for a LOW logic level to be present at the D_A input prior to the clock input transition from LOW to HIGH in order for the master latch to retain a LOW logic level. Refer to Figure 7. LOW data must be present at all times between t_{sL} max. and t_{sH} min.

t_{sH} (D_A) The time required for a HIGH logic level to be present at the D_A input prior to the clock input transition from LOW to HIGH in order for the master latch to retain a HIGH logic level. Refer to Figure 7. HIGH data must be present at all times between t_{sH} max. and t_{sL} min.

t_s(A) The time, relative to either clock edge, required for the device to respond to changes on the A address inputs.

t_{pd+} (D_A) The propagation delay from the data input LOW to HIGH transition to the Z output LOW to HIGH transition. Refer to Figure 5.

t_{pd-} (D_A) The propagation delay from the data input HIGH to LOW transition to the Z output HIGH to LOW transition. Refer to Figure 5.

t_{pd+}(B,C-Z) The propagation delay from the B or C address input transition to the Z output LOW to HIGH transition. Refer to Figure 6.

t_{pd-}(B,C-Z) The propagation delay from the B, C address input transition to the Z output HIGH to LOW transition. Refer to Figure 6.

CP_{pw} 'L' The minimum LOW clock pulse width required to write data into the master latch. Refer to Figure 8.

CP_{pw} 'H' The minimum HIGH clock pulse width required to store information into the slave latch. Refer to Figure 9.

TYPICAL SWITCHING TIME CHARACTERISTICS

All inputs and outputs loaded with 15 pF capacitance only. Output capacitance is referred to as C_L.

Propagation Delay Versus Ambient Temperature (CP to Z)

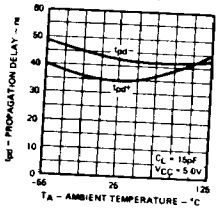


Figure 4

Propagation Delay Versus Ambient Temperature (D_A to Z)

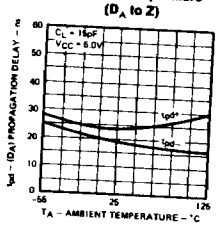


Figure 5

Propagation Delay Versus Ambient Temperature (Read Address to Z)

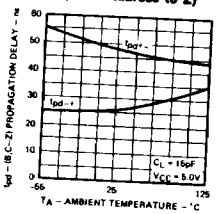


Figure 6

Set Up, Release Time Versus Ambient Temperature

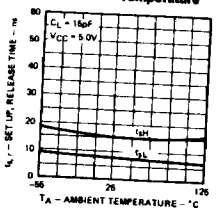


Figure 7

Minimum LOW Clock Pulse Width

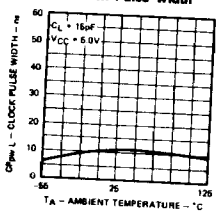


Figure 8

Minimum HIGH Clock Pulse Width

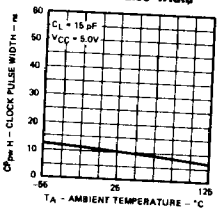
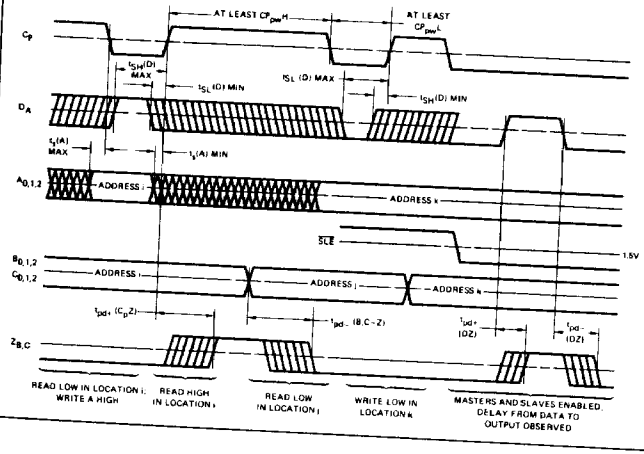


Figure 9

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

MSI INTERFACING RULES

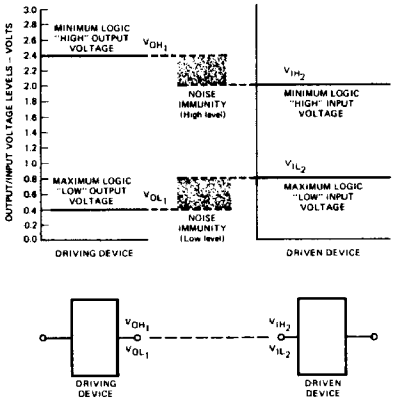
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am9338 LOADING RULES (in unit loads)

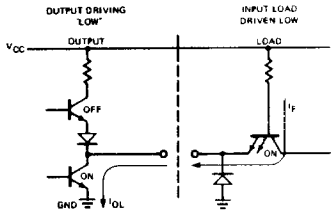
Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	LOW
B_0	1	0.625	—	—
B_1	2	0.625	—	—
B_2	3	0.625	—	—
Z_B	4	—	20	10
Z_C	5	—	20	10
C_2	6	0.625	—	—
C_1	7	0.625	—	—
GND	8	—	—	—
C_0	9	0.625	—	—
$\overline{SLE}$	10	0.625	—	—
CP	11	0.625	—	—
DA	12	0.625	—	—
A_2	13	0.625	—	—
A_1	14	0.625	—	—
A_0	15	0.625	—	—
V_{CC}	16	—	—	—

INPUT/OUTPUT INTERFACE CONDITIONS

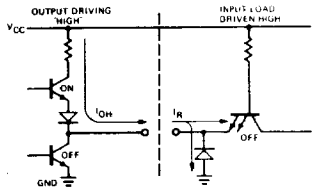
Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW

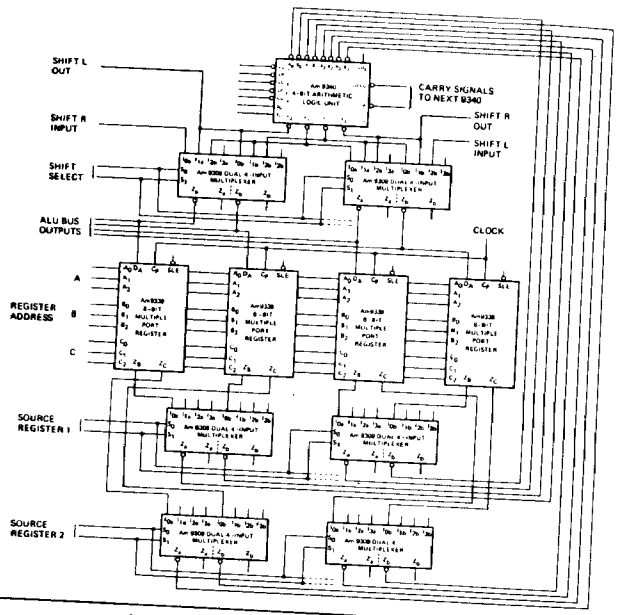


Current Interface Conditions — HIGH



Am9338 APPLICATION

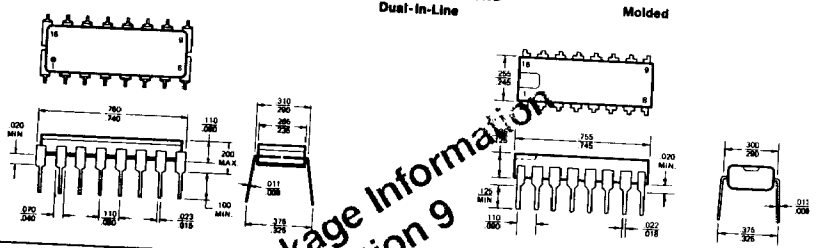
THREE ADDRESS ARITHMETIC REGISTER 4-BIT SLICE



A typical three address arithmetic register system where two operands can be taken from any two registers, operated upon, and the result written in to any register in the system.

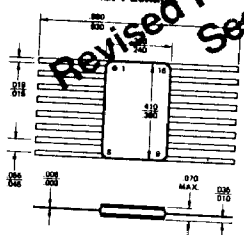
PHYSICAL DIMENSIONS

Hermetic — **Dual-In-Line** — **Molded**



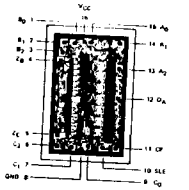
PHYSICAL DIMENSIONS

Flat Package



Metallization and Pad Layout

77 x 125 Mils



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901 Thompson Place
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(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

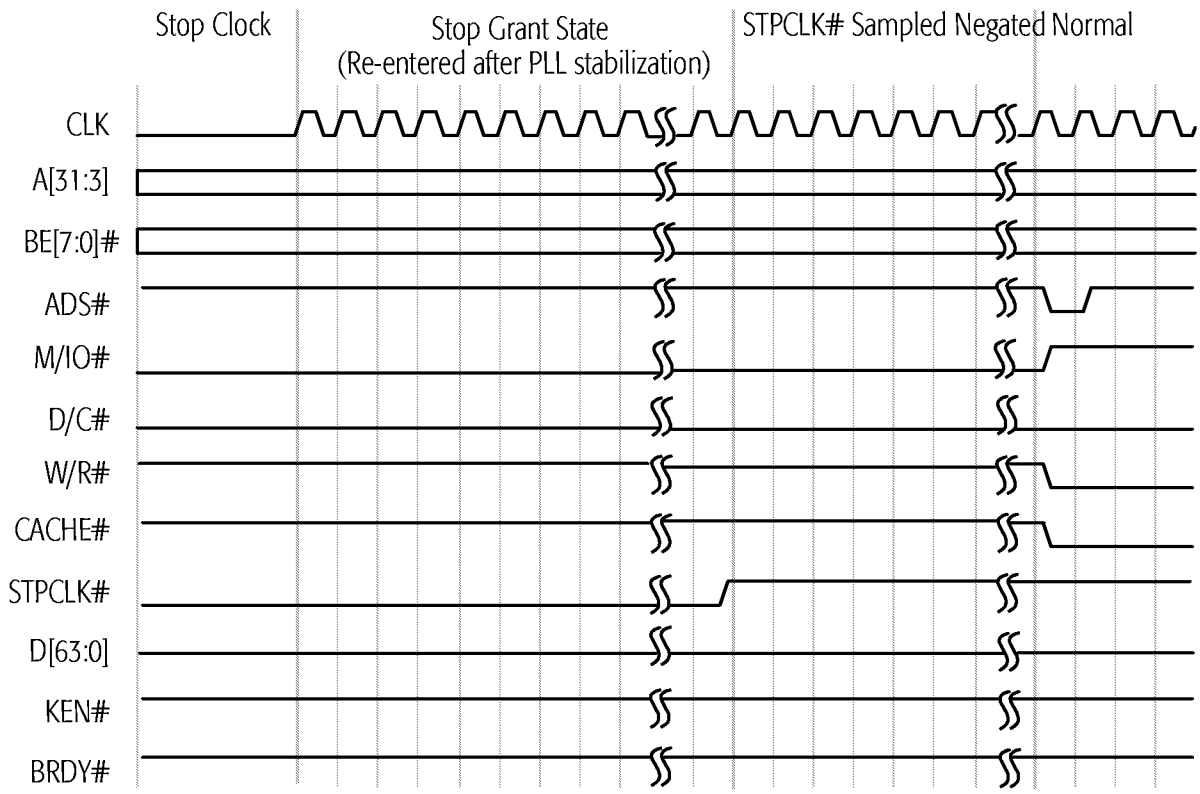

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

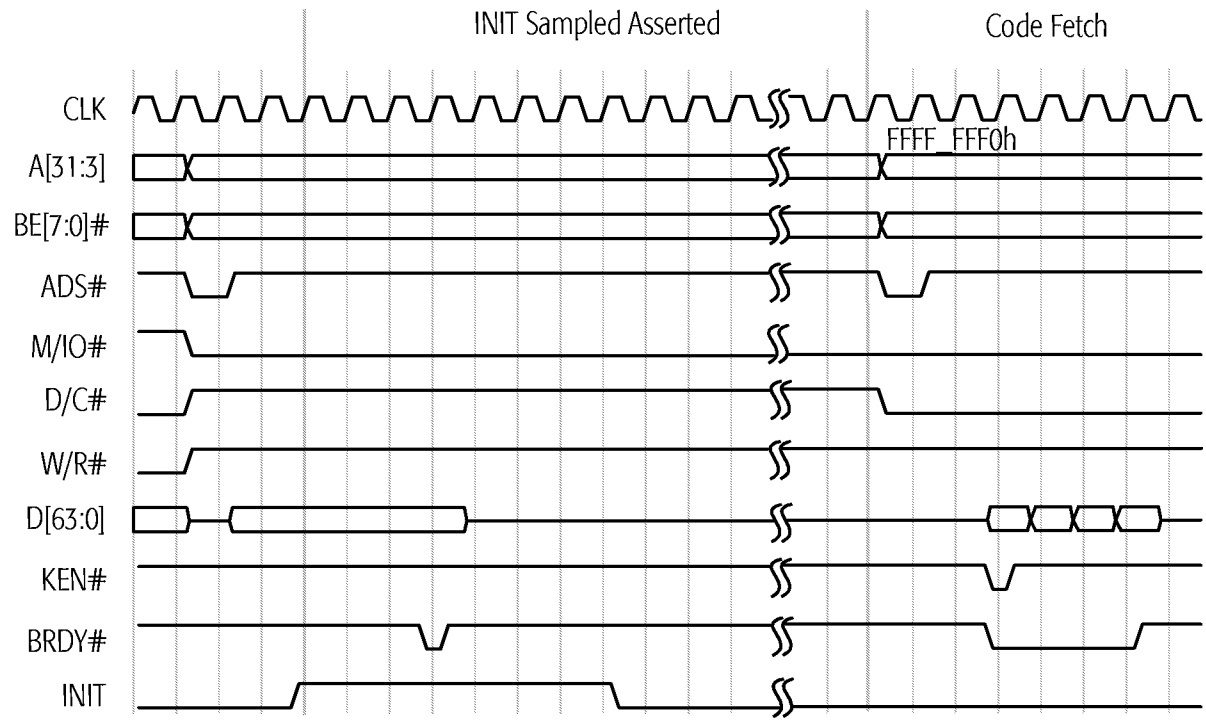

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.