

**8/16-bit Data Bus
Mask ROM Card**

**MF72M1 - G7DATXX
MF74M1 - G7DATXX**

Connector Type

Two-piece 68-pin

DESCRIPTION

Mitsubishi's MASK ROM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm×54mm×3.3mm). The cards use a 8/16-bit data bus. Available 2 MB, 4 MB capacities. Mitsubishi's MASK ROM cards are available with a 68 pin, two-piece connector.

- 68-pin connector
- 8/16 bit controllable data bus width
- JEIDA ver 4/4.1 (PCMCIA2.0) compatible
- No attribute memory

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size
- Electrostatic discharge protection to 15kV

APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

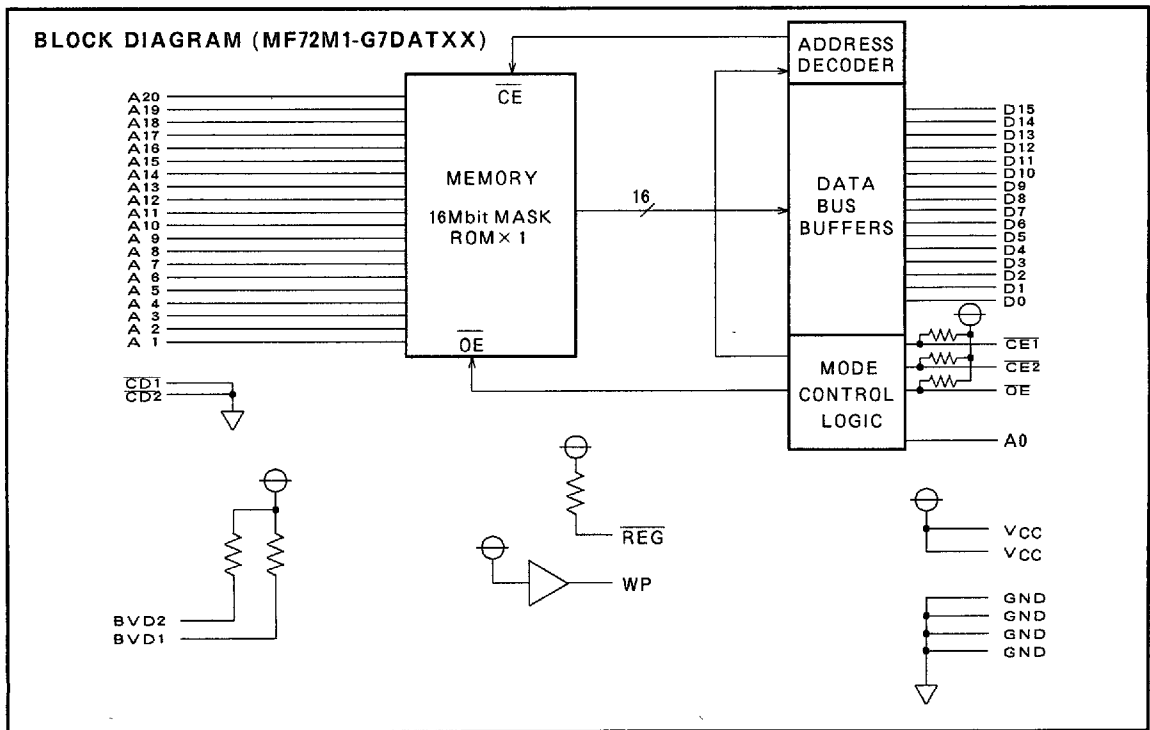
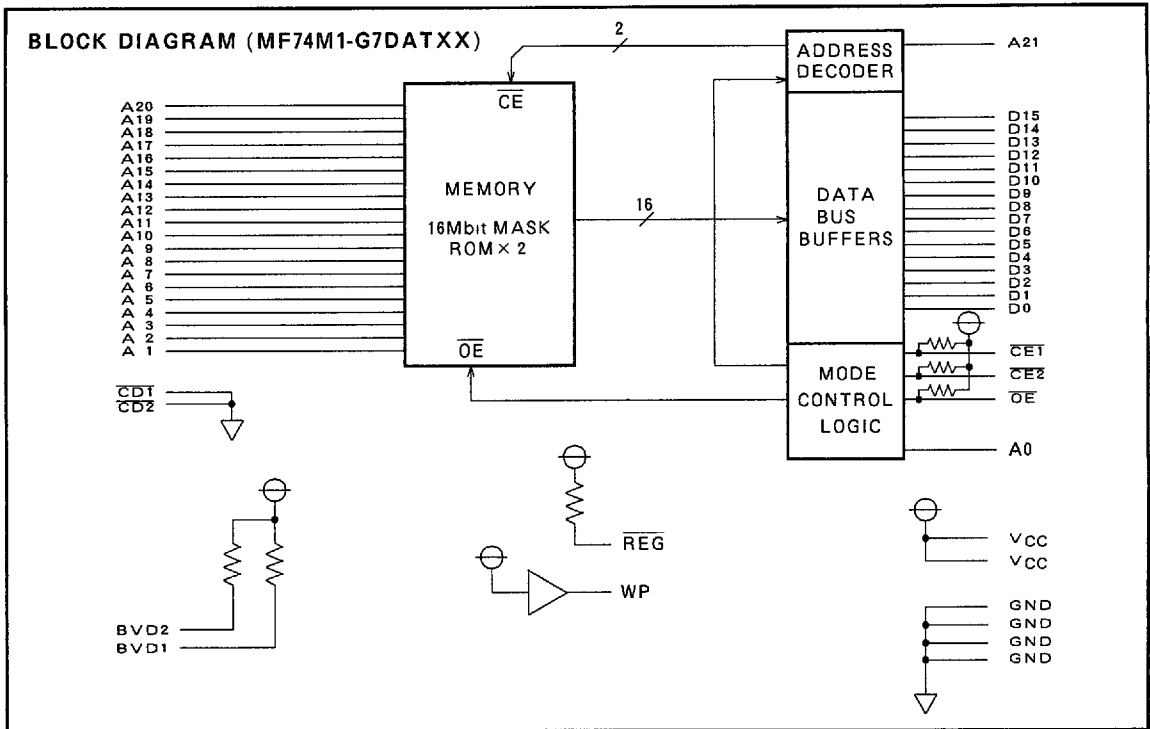
PRODUCT LIST

Type name	Item	Memory capacity	Data Bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF72M1-G7DATXX		2 MB	8/16	200	Two-piece	68	68P-001
MF74M1-G7DATXX		4 MB					

MASK ROM CARDS

PIN ASSIGNMENT
Two-Piece Type (68-pin)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3	} Data I/O	36	CD 1	Card detect 1
3	D 4		37	D11	} Data I/O
4	D 5		38	D12	
5	D 6		39	D13	
6	D 7		40	D14	
7	CE 1		41	D15	
8	A10	Card enable 1	42	CE 2	Card enable 2
9	OE	Output enable	43	NC	} No connection
10	A11	} Address input	44	NC	
11	A 9		45	NC	
12	A 8		46	A17	} Address input
13	A13		47	A18	
14	A14		48	A19	
15	NC	No connection	49	A20	} A21 (NC for ≤ 2 MB types) Power supply voltage
16	NC	No connection	50	A21	
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	} No connection
19	A16	} Address input	53	NC	
20	A15		54	NC	
21	A12		55	NC	
22	A 7		56	NC	
23	A 6		57	NC	
24	A 5		58	NC	
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	REG	REG function
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0	63	BVD 1	Battery voltage detect 1	
30	D 0	} Data I/O	64	D 8	} Data I/O
31	D 1		65	D 9	
32	D 2		66	D10	
33	WP	Write protect	67	CD 2	Card detect 2
34	GND	Ground	68	GND	Ground



MASK ROM CARDS

FUNCTION TABLE

Mode	CE 1	CE 2	OE	A 0	I/O (D15~D 8)	I/O (D 7 ~D 0)	Icc
Standby	H	H	X	X	High-impedance	High-impedance	Standby
Read A (16bit) Common	L	L	L	X	Odd byte Data out	Even Byte Data out	Active
Read B (8 bit) Common	L	H	L	L	High-impedance	Even Byte Data out	Active
	L	H	L	H	High-impedance	Odd byte Data out	Active
Read C (8 bit) Common	H	L	L	X	Odd byte Data out	High-impedance	Active
Output disable	X	X	H	X	High-impedance	High-impedance	Active

Note 1 : H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-0.3 ~ + 6.0	V
V _I	Input voltage		-0.3 ~ V _{CC} + 0.3	V
V _O	Output voltage		0 ~ V _{CC}	V
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-30 ~ 80	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	V _{CC} supply voltage	4.75	5	5.25	V
T _a	Operating temperature	0		55	°C

MASK ROM CARDS

DC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = V_{pp} = 4.75 \sim 5.25\text{V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	High input voltage		2.4		V_{CC}	V
V_{IL}	Low input voltage		0		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1.0\text{mA}$ (except BVD1, 2)	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2.0\text{mA}$			0.4	V
I_{IH}	High input current	$V_I = V_{CC}$ V			10	μA
I_{IL}	Low input current	$V_I = 0\text{V}$	$\overline{CE}1, \overline{CE}2, \overline{OE}, \text{REG}$	-10	-70	μA
			Other inputs		-10	
I_{OZH}	High output current in off state	$\overline{CE}1 = \overline{CE}2 = V_{IH}$ or $\overline{OE} = V_{IH}$, $V_O = V_{CC}$			10	μA
I_{OZL}	Low output current in off state	$\overline{CE}1 = \overline{CE}2 = V_{IH}$ or $\overline{OE} = V_{IH}$, $V_O = 0\text{V}$			-10	μA
$I_{CC1 \cdot 1}$	Active supply current 1	$CE1 = CE2 = V_{IL}$, Other inputs = V_{IH} or V_{IL} , Outputs = open	2MB		140	mA
			4MB		150	
$I_{CC1 \cdot 2}$	Active supply current 2	$CE1 = CE2 \leq 0.2\text{V}$, Other inputs $\leq 0.2\text{V}$ or $\geq V_{CC} - 0.2\text{V}$, Outputs = open	2MB		120	mA
			4MB		130	
$I_{CC2 \cdot 1}$	Standby supply current	$CE1 = CE2 = V_{IH}$, Other inputs = V_{IH} or V_{IL}	2MB		10	mA
			4MB			
$I_{CC2 \cdot 2}$	Standby supply current	$CE1 = CE2 \geq V_{CC} - 0.2\text{V}$, Other inputs ≤ 0.2 or $\geq V_{CC} - 0.2\text{V}$	2MB		0.5	mA
			4MB		1	

Note 2 : Direction for currents flowing into IC card is indicated as positive (no mark).

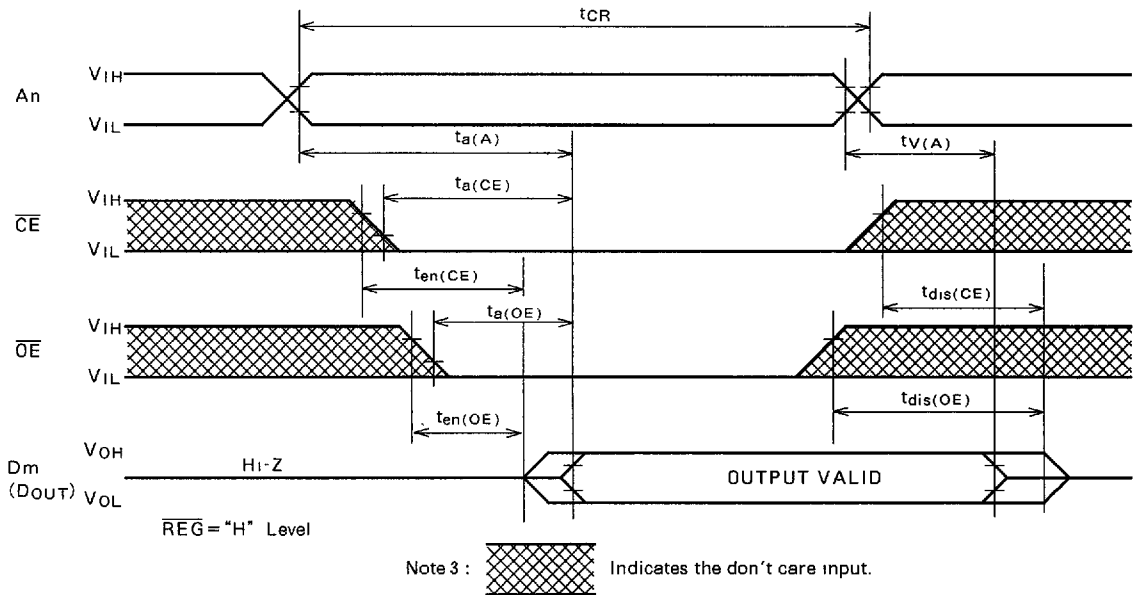
AC ELECTRICAL CHARACTERISTICS (COMMON MEMORY)

Read Cycle ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 4.75 \sim 5.25\text{V}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CR}	Read cycle time	200			ns
$t_{a(A)}$	Address access time			200	ns
$t_{a(CE)}$	Card select access time			200	ns
$t_{a(OE)}$	Output enable access time			100	ns
$t_{dis(CE)}$	Output disable time (from \overline{CE})			90	ns
$t_{dis(OE)}$	Output disable time (from \overline{OE})			90	ns
$t_{en(CE)}$	Output enable time (from \overline{CE})	5			ns
$t_{en(OE)}$	Output enable time (from \overline{OE})	5			ns
$t_{v(A)}$	Data valid time after address change	0			ns

TIMING DIAGRAM (COMMON MEMORY)

Read Cycle



Note 4 : Test Conditions

Input pulse levels : $V_{IL}=0.4V$, $V_{IH}=2.8V$

Input pulse rise, fall time : $t_r=t_f=20ns$

Reference voltage

Input : $V_{IL}=0.8V$, $V_{IH}=2.4V$

Output : $V_{OL}=0.8V$, $V_{OH}=2.0V$

(t_{en} and t_{dis} are measured when output voltage is $\pm 500mV$ from steady state.)

Load : 100pF + 1 TTL gate

5 pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

5 : \overline{CE} indicates as follows :

Read A/Write A : $\overline{CE} = \overline{CE1} = \overline{CE2}$

Read B/Write B : $\overline{CE} = \overline{CE1}$, $\overline{CE2} = "H"$ level

Read C/Write C : $\overline{CE} = \overline{CE2}$, $\overline{CE1} = "H"$ level

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C _i	Input capacitance	V _i =GND, V _i =25mVrms, f=1MHz, T _a =25°C	2 MB		50	pF
			4 MB			
C _o	Output capacitance	V _o =GND, V _o =25mVrms, f=1MHz, T _a =25°C	2 MB		45	pF
			4 MB			

Note 6 : These items are not 100% tested.