## MN6147

## COMS PLL Frequency Synthesizer for FM-AM Stereo Tuners

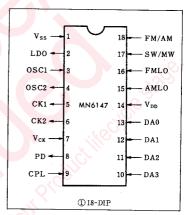
#### Outline

The MN6147 is a high-performance LSI designed for the PLL frequency synthesizer system for FM-AM stereo tuners. It is capable of directly processing an FM signal and has various functions for Hi-Fi stereo tuners. It can also process SW and LW signals. It operates on single +5V power. A clock circuit can be backed up by a battery.

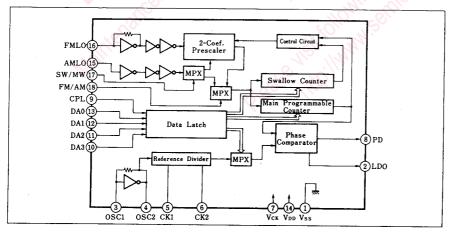
#### **■** Features

- Capable of selecting 6 kinds of reference frequencies; 25, 10, 9, 5, 2.5, and 1 kHz.
- FM filter frequency shift: ±25 Hz, Resolution: 25 kHz, IF filter frequency shift: ±25 kHz, ±50 kHz, ±75 kHz
- •5 pins for 4-bit parallel data input, and data input clock 1 input and data input
- •2 input pins for programmable frequency divider; for FM and for SW/MW/LW
- With 562.5 kHz and 250 Hz output pins as control output

#### Pin Configuration



## Block Diagram



### ■ Absolute Maximum Ratings(V<sub>SS</sub>=OV, Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	-0.3~+10	V
Input voltage	VI	$-0.3 \sim V_{DD} + 0.3$	v
Output voltage ;	Vo	$-0.3 \sim V_{DD} + 0.3$	v
Power dissipation	PD	250	$\mathbf{m}\mathbf{W}$
Operating ambient temperature	Topr	-30~+70	°C
Storage temperature	Tstg	-55~+100	°C

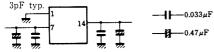
## ■ Operating Conditions( $V_{SS}=0V$ , $T_a=-30$ to $+70^{\circ}C$ )

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage(1) .	V <sub>DD</sub>		4.5	5	5.5	V
Supply voltage(2)	V <sub>(CK)</sub>	Clock Supply	3.5	5	5.5	v

## ■ Electrical Characteristics( $V_{DD} = +4.5$ to 6.0 V, $V_{SS} = 0$ V, $T_{a} = -30$ to $+70^{\circ}$ C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply current	IDD	T	100	20	30	mA
Total power consumption	Ptot	$V_{DD} = 5V$ , $Ta = 25$ °C	2,	100	150	mW
Supply current	I(CK)	Clock current, V(CK) = +5V, Ta = 25°C		0.6	1.5	mA
Input Pins(DA0-DA3, CPL,	FM/AM, S	W/MW)				
Input voltage high level	V <sub>IH(1)</sub>	N CV	2.4		VDD	V
Input voltage low level	V <sub>1L(1)</sub>	$V_{DD}=5V$	Vss		0.8	V
Input current	I <sub>I(1)</sub>	$V_I = V_{SS} \sim V_{DD}$			±10	μA
Input Pin(FMLO)		So on all so			3	41,
Input voltage	VI(1)	- S . M. H.	1.0		. 20	$V_{p-p}$
Input current	I <sub>1(2)</sub>	V <sub>I(1)</sub> =0 V or 5 V	±10	± 50	± 250	μA
Input frequency(max.)	fi(FM)	V <sub>DD</sub> =4.5~5.5V	120	76		MHz
Input Pin(AMLO)		The grant of the state of	(17)	10,	50	
Input voltage	V <sub>1(2)</sub>	16, 16, 11, 20, 18	1.0		100	<b>V</b> <sub>p-p</sub>
Input current	I1(3)	$V_{I(2)} = 0$ or 5 V	±1	±5	± 25	μA
Input frequency(max.)	fi(AM)	$V_{DD} = 4.5 \sim 5.5 V$	30	70.		MHz
Oscillator Circuit Pins(OSC	1, OSC2)	10 20 11	- Oc			
Oscillation frequency	fosc	90, 0, 70	-01	4.5		MHz
Output Pin(PD)	3	Mi di	9			
Output current high level	IOH(1)	$V_{DD}=5V$ , $V_0=3V$	-0.8			mA
Output current low level	I <sub>OL(1)</sub>	$V_{DD}=5V$ , $V_0=2V$	0.8			mA
Output current(Open)	Io	$V_{DD}=5V$ , $V_0=V_{SS}-V_{DD}$			+0.1	nA
Output Pins(CK1, CK2)		-81 - 1/14				
Output voltage high level	V <sub>OH(1)</sub>	$V_{DD} = 5V, I_{OH(1)} = 100 \mu A$	4.0			V
Output voltage low level	V <sub>OL(1)</sub>	$V_{DD} = 5V$ , $I_{OL(1)} = 100 \mu A$			0.4	V
Output Pin(LDO)						
Output voltage high level	V <sub>OH(2)</sub>	$V_{\rm DD} = 5  \text{V},  I_{\rm OH} = -200  \mu  \text{A}$	4.0			V
Output voltage low level	V <sub>OL(2)</sub>	$V_{DD} = 5V$ , $I_{OL} = 200 \mu A$			0.4	V

Note) Connect a capacitor to each of the power supply pins VDD, V(CK) and Vss for use. Input capacitance(FMLO, AMLO) =

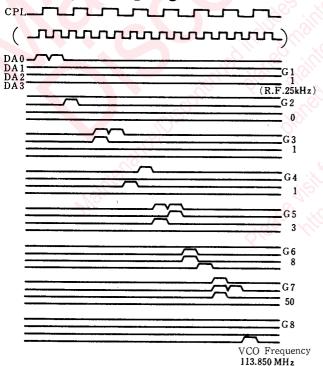


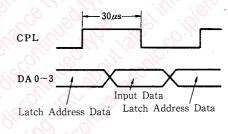
## ■ Pin Descriptions

Pin No.	Symbol	Description					
1	Vss	Ground					
2	LDO(QO)	Lock detector output(oscillator circuit output)					
3	OSC1						
4	OSC2	4.5 MHz crystal oscillation					
5	CK1	Clock output 1(562.5 kHz*)					
6	CK2	Clock output 2(250 Hz)					
7	V <sub>CK</sub>	Frequency divider circuit for real time clock battery backup(5 V)					
8	PD	Phase detector output(3-state)					
9	CPL	Latch clock					
10	DA3	Data and address input(MSB)					
11	DA2	D-4 1 11					
12	DA1	Data and address input					
13	DA0	Data and address input(LSB)					
14	V <sub>DD</sub>	Main power(5 V)					
15	AMLO	AM local oscillation signal input					
16	FMLO	FM local oscillation signal input					
17	SW/MW	SW/MW switching					
18	FM/AM	FM/AM switching					

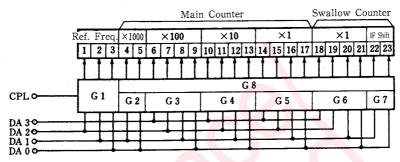
Following three clock frequencies, 187.5 kHz, 375 kHz and 1.125 MHz, can also be available by changing inner wiring.

## ■ Data Input Timing Diagram





#### ■ Relations between Data Input Pins and Programmable Counters



#### Latch Group Selector Code Table

Latch Input Code	G1	G2	G3	G4	G5	G6	G7	G8
DA3	L	L	L	L	L	L	L	Н
DA2	L	L	L	H	H	H	Н	X
DA1	L	Н	Н	L	L	H	Н	×
DA0	Н	L	Н	L	Н	L	Н	×

Ref. Frequency(rl) Selector Code Table

kHz Input Code	2.5	25	9	10	5	1
DA2	L	L	L	L	Н	Н
DA1	L	L	Н	Н	L	Н
DA0	L	Н	L	Н	X	×

## ■ Data Input Example

1 2 3 4 5 6	7 8 9 10 11 12 13 14	15 16 17 18 19 20 21 22 23
		4 2 1) (8 4 2 1) (21)
Freq. ×1000	×100 ×10	×1 ×1 IF Shift
	Main Counter	Swallow Counter

[Example I] For FM;

Bit 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Data (0 0 1)(0 0) (0 0 0 0) (1 0 0 1) (0 1 0 1) (0 0 1 0) (0 0)

0 0 9 5 2 0

Freq. dividing ratio N = 952×4+0=3808
25 kHz VCO freq. f=3808×25 kHz=95.200 MHz

[Example 2] For FM;

Freq. dividing ratio  $N=1268\times4+2=5074$ 25 kHz VCO freq.:  $f=5074\times25$  kHz=126.850 MHz

Freq. dividing ratio N = 29585 kHz VCO freq.  $f = 2958 \times 5 \text{ kHz} = 14.790 \text{ MHz}$ 

IF Shift Table

3				0
kHz Input Code	0	25	50	75
DA1	L	L	Н	Н
DA0	L	Н	L	Н

# FM, SW and MW(LW) Signal Processing Switching Table

Input Si	gnal	Selector Pin Code		
Signal	Pin	FM/AM®	SW/MW10	
FM	16	Н	X	
SW	15	L	€ H	
MW(LW)	15)	L so	L	

#### [Example 4] For SW;

Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

Data (1 1 ×) (0 1) (0 1 1 0 0) (1 0 0 1) (0 1 0 1) (0 0 0 1 1 1)

1 6 9 5 7

Freq. dividing ratio N=169571 kHz VCO freq.  $f=16957 \times 1 \text{ kHz}=16.957 \text{ MHz}$ 

#### (Example 5) For MW;

Bit 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Data (0, 1, 1) (0, 0) (0, 0, 0, 1) (0, 0, 1, 0) (0, 1, 1, 0) (0, 0, 0, 0, 0)

0, 1, 2, 6

Freq. dividing ratio N=126 10 kHzVCO frequency=126×10 kHz=1260 kHz

#### [Example 6] For MW:

Bit 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,

Data (0.10)(00)(00001)(0001)(10001)(10001)(00000)
0 1 1 9

Freq. dividing ratio N = 1199 kHz VCO freq  $f = 119 \times 9 \text{ kH z} = 1071 \text{ kHz}$ 

## ■ Receive Frequency Example

## (FM Band)

Region	Frequenc	y Band <b>IHz</b> )	Channel Width (kHz)	Ref. Frequency (kHz)	Interm	ediate Fred	quency
Japan	76.1	89.9	100	25	-10.700,	-10.675,	-10.650
America 1	87.9	107.9	200	25			
America 2	87.9	107.9	100	25	10.700,	10.725,	10.750
Europe	87.50	108.00	50	25	10.700,	10.725,	10.750

## (AM Band)

Region	Frequency	y Band	Channel Width (kHz)	Ref. Frequency (kHz)	Intermediate Frequency (kHz)
Japan	522	1611	9	9	450
America 1	530	1620	10	10	450
America 2	522	1611	9	9	450
Europe 1	522	1611	9	9	450
Europe 2	530	1620	10	10	450

## [LW Band]

Region	Frequency	Band	Channel Width (kHz)	Ref. Frequency (kHz)	Intermediate Frequency (kHz)
	146	353	9,5	i	450

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