KS82C88A

MICROPROCESSOR BUS CONTROLLER

FEATURES/BENEFITS

- **Pin and functional compatibility with the Industry standard 8288**
- **Very high speed — 8MHz and 10MHz**
- **Low power CMOS implementation**
- **Bipolar drive capability**
- **TTL I/O compatibility**
- **3-state command output drivers**
- **Configurable for use with an I/O bus**
- **Facilitates interface to one or two multi-master buses**

DESCRIPTION

The KS82C88A Bus Controller is a 20-pin CMOS component which includes command and control timing generation as well as a bipolar bus drive capability while optimizing system performance. A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

The KS82C88A is manufactured using advanced CMOS technology. Fully static, with very high speed operation, the KS82C88A is designed for use in medium-to-large 8088/86 microprocessor systems.

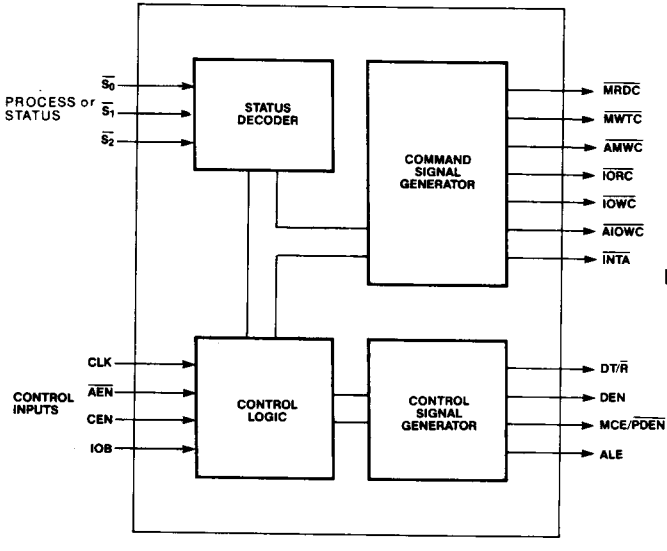

Figure 2: KS82C88 Block Diagram

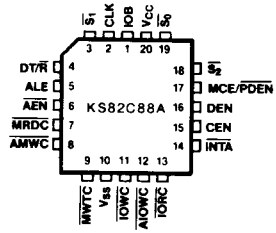

Figure 1a: 20-Pin PLCC Configuration

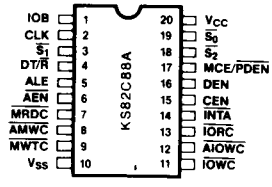

Figure 1b: 20-Pin DIP Configuration

Table 1a: PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{IOWC}$
2	I	CLK	12	O	$\overline{AIOWC}$
3	I	$\overline{S}_1$	13	O	$\overline{IORC}$
4	O	DT/$\overline{R}$	14	O	$\overline{INTA}$
5	O	ALE	15	I	CEN
6	I	$\overline{AEN}$	16	O	DEN
7	O	$\overline{MRDC}$	17	O	MCE/$\overline{PDEN}$
8	O	$\overline{AMWC}$	18	I	$\overline{S}_2$
9	O	$\overline{MWTC}$	19	I	$\overline{S}_0$
10	—	V_{SS}	20	—	V_{CC}

Table 1b: 20-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{IOWC}$
2	I	CLK	12	O	$\overline{AIOWC}$
3	I	$\overline{S}_1$	13	O	$\overline{IORC}$
4	O	DT/$\overline{R}$	14	O	INTA
5	O	ALE	15	I	CEN
6	I	$\overline{AEN}$	16	O	DEN
7	O	$\overline{MRDC}$	17	O	MCE/$\overline{PDEN}$
8	O	$\overline{AMWC}$	18	I	$\overline{S}_2$
9	O	$\overline{MWTC}$	19	I	$\overline{S}_0$
10	—	V_{SS}	20	—	V_{CC}

Table 2: Pin Descriptions

Symbol	Type	Name and Function
$\overline{AEN}$	I	**Address Enable:** $\overline{AEN}$ enables the KS82C88 command outputs at least t_{AELCV} (Table 4) after it becomes active (LOW). When $\overline{AEN}$ goes inactive, the command output drivers are immediately 3-stated. $\overline{AEN}$ does not affect the I/O command lines if the KS82C88 is in the I/O Bus mode (IOB tied HIGH).
$\overline{AIOWC}$	O	**Advanced I/O Write Command:** The $\overline{AIOWC}$ issues an I/O Write command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. This signal is active LOW.
ALE	O	**Address Latch Enable:** This signal serves to strobe an address into the address latches. It is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AMWC}$	O	**Advanced Memory Write Command:** This active LOW signal is used to issue a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal.
CEN	I	**Command Enable:** When LOW all KS82C88 command outputs, and the control outputs DEN and $\overline{PDEN}$ are forced to the inactive state. When HIGH, these outputs are enabled.
CLK	I	**Clock:** This clock signal from the KS82C88 clock generator is used to determine when command and control signals are generated.
DEN	O	**Data Enable:** This active HIGH signal enables data transceivers onto either the local or system data bus.
DT/$\overline{R}$	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. HIGH indicates Transmit (write to I/O or memory), LOW indicates Receive (Read).
$\overline{INTA}$	O	**Interrupt Acknowledge:** This active LOW signal tells an interrupting device that its interrupt has been acknowledged and that it should drive vector information onto the data bus.
IOB	I	**Input/Output Bus Mode:** When IOB is strapped HIGH the KS82C88 functions in the I/O Bus mode. When strapped LOW, the KS82C88 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes)

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{IORC}$	O	**I/O Read Command:** This active LOW signal instructs an I/O device to drive its data onto the data bus.
$\overline{IOWC}$	O	**I/O Write Command:** This active LOW signal instructs an I/O device to read the data on the data bus.
MCE/$\overline{PDEN}$	O	**MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. **$\overline{PDEN}$ (IOB is tied HIGH):** Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs.
$\overline{MRDC}$	O	**Memory Read Command:** This active LOW signal instructs the memory to drive its data onto the data bus.
$\overline{MWTC}$	O	**Memory Write Command:** This active LOW signal instructs the memory to record the data present on the data bus.
$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$	I	**Status Input Pins:** These are status input pins from 8088/86/89 processors. The KS82C88 decodes these inputs to generate command and control signals at the appropriate time. These pins are HIGH when not in use. Internal pull-up resistors hold these lines HIGH when no other driving source is present.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

Command and Control Logic

The KS82C88A decodes the status line signals ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) common to the 8086/88/89 processors to determine what command is to be issued, (Table 3).

Table 3: KS82C88A Commands

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Processor State	8288A Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Operating Modes

The KS82C88A can be operated in one of two modes, I/O Bus Mode or System Bus Mode according to the system hardware configuration.

I/O Bus Mode: *(IOB Strapped HIGH)*

In the I/O Bus (IOB) mode the I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the KS82C88A immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ control the I/O bus transceiver. Since no arbitration is present, the I/O command lines should not be used to control the sytem bus in this mode. This mode allows one KS82C88A to handle two external buses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a Bus Ready signal ($\overline{AEN}$ LOW) before proceeding. The IOB mode is aimed at applications where I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode: *(IOB Strapped LOW)*

In this mode no commands are issued until t_{AELCV} (Table 4) after the $\overline{AEN}$ Line is activated (LOW). This mode assumes that bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists, and both I/O and memory are shared by more than one processor.

Table 4: Command Outputs

$\overline{MRDC}$	Memory Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{IORC}$	I/O Read Command
$\overline{IOWC}$	I/O Write Command
$\overline{AMWC}$	Advanced Memory Write Command
$\overline{AIOWC}$	Advanced I/O Write Command
$\overline{INTA}$	Interrupt Acknowledge

Command Outputs

Advanced write commands prevent the processor from entering unnecessary wait states. They are available to initiate write procedures early in the machine cycle.

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. $\overline{INTA}$ informs an interrupting device that it should place service vectors onto the data bus.

Control Outputs

KS82C88A control outputs include Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). DEN determines when the external bus should be enabled onto the local bus and DT/$\overline{R}$ determines the direction of data transfer. These two signals are usually connected to the transceiver chip select and direction pins.

MCE/$\overline{PDEN}$ alters its function with the operating mode. In the IOB mode, the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

In the System Bus Mode, MCE is used during interrupt acknowledge cycles. Two interrupt acknowledge cycles occur back to back during interrupt sequences, with no data or address transfers during the first cycle. Thus logic should be provided to mask off MCE. Just before the second cycle, MCE gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, MCE is not used and the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable (ALE) and Halt

ALE occurs every machine cycle and strobes the current address into the address latches. ALE also strobes $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ into a latch for halt state decoding.

Command Enable (CEN)

CEN is a command qualifier for the KS82C88A. If CEN is HIGH, the KS82C88A functions normally, and all command lines are held in their inactive state (note 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus and resident bus devices.

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Table 5: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 6: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS}-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits Min	Limits Max	Units
C_{IN}	Input Capacitance		Freq. = 1MHz		5	pF
C_{OUT}	Output Capacitance		Unmeasured pins at V_{SS}		15	pF
I_{BHH}	Input Leakage Current (Bus Hold High)		V_{IN} = 2.0V (Notes 3, 4)	-50	-300	μA
I_{BHHO}	Bus Hold High Overdrive		(Notes 3, 5)	-600		μA
I_{CC}	Operating Supply Current *		V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded, Freq 5MHz		5	mA
I_{CCS}	Standby Supply Current		V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded		100	μA
I_{LI}	Input Leakage Current		0V ≤ V_{IN} ≤ V_{CC} (Notes 1, 2)		±10	μA
I_{LO}	Output Leakage Current		0V ≤ V_{OUT} ≤ V_{CC}		±10	μA
V_{CH}	V_{IH} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$			3.0	V_{CC}+0.3	V
V_{CL}	V_{IL} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$				0.2V_{CC}	V
V_{IH}	Input High Voltage			2.2	V_{CC}+0.3	V
V_{IL}	Input Low Voltage			-0.3	0.8	V
V_{OH}	Output High Voltage	Command Outputs	I_{OH} = -5mA I_{OH} = -1mA	3.7 3.7		V V
		Control Outputs	I_{OH} = -4mA I_{OH} = -2.5mA	3.0 V_{CC}-0.4		V V
V_{OL}	Output LOW Voltage		I_{OL} = 12mA I_{OL} = 8mA		0.45 0.44	V V

Notes: 1. Except $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$.
2. During input leakage test, maximum input rise and fall time should be 15ns between V_{CC} and V_{SS}.
3. $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$ only.
4. Raise inputs to V_{CC}, then lower to 2.0V.
5. An external driver must sink at least I_{BHHO} to toggle a status line from HIGH to LOW.

Table 8: AC Characteristics, (T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

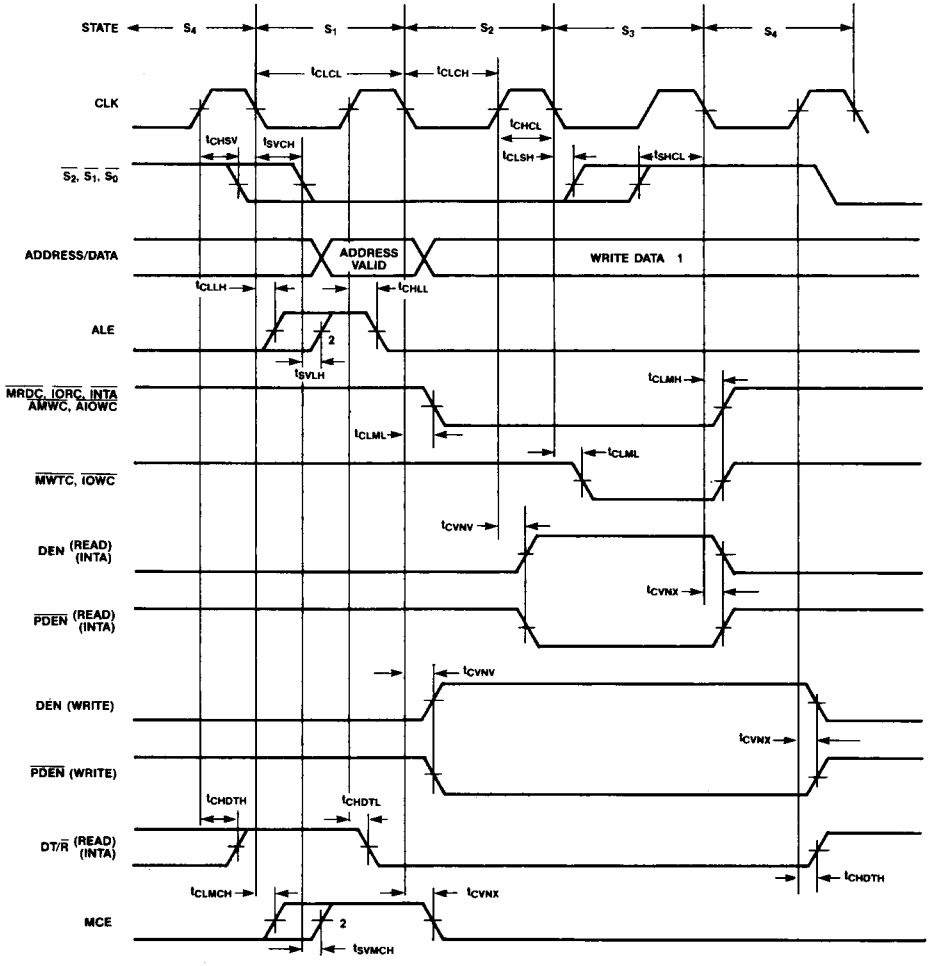
Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AEHCZ}	Command Disable Time	D (Note 2)		40		40	ns
t_{AELCH}	Command Enable Time	C (Note 1)		40		40	ns
t_{AELCV}	Enable Delay Time	B	100	250	100	200	ns
t_{AEVNV}	$\overline{AEN}$ to DEN	A		25		20	ns
t_{CELRH}	CEN to Command	B		t_{CLML}+10		t_{CLML}	ns
t_{CEVNV}	CEN to DEN, $\overline{PDEN}$	A		25		25	ns
t_{CHCL}	CLK High Time		40		30		ns
t_{CHDTH}	Direction Control Inactive Delay	A		30		30	ns
t_{CHDTL}	Direction Control Active Delay	A		50		50	ns
t_{CHLL}	ALE Inactive Delay	A (Note 3)	2	25	2	15	ns
t_{CHSV}	Status Inactive Hold Time		10		10		ns
t_{CLCH}	CLK Low Time		66		50		ns
t_{CLCL}	CLK Cycle Period		125		100		ns
t_{CLLH}	ALE Active Delay (from CLK)	A		20		20	ns
t_{CLMCH}	MCE Active Delay (from CLK)	A		25		20	ns
t_{CLMH}	Command Inactive Delay	B	2	35	2	35	ns
t_{CLML}	Command Active Delay	B	5	35	5	35	ns
t_{CLSH}	Status Active Hold Time		10		10		ns
t_{CVNV}	Control Active Delay	A	2	45	2	45	ns
t_{CVNX}	Control Inactive Delay	A	5	45	5	45	ns
t_{MHNL}	Command Inactive to DEN Low Delay	Command: B, DEN: E	t_{CLCH}-5		t_{CLCH}-5		ns
t_{OHOL}	Output, Fall Time	From 2.0V to 0.8V		15		20	ns
t_{OLOH}	Output, Rise Time	From 0.8V to 2.0V		15		12	ns
t_{SHCL}	Status Inactive Setup Time		35		35		ns
t_{SVCH}	Status Active Setup Time		35		35		ns
t_{SVLH}	ALE Active Delay (from Status)	A		20		20	ns
t_{SVMCH}	MCE Active Delay (from Status)	A		30		20	ns

Refer to Figure 5 for Test Conditions Definition Table.

Notes: 1. t_{AELCH} measurement is between 1.5V and 2.5V.
2. t_{AEHCZ} measured at 0.5V change in V_{OUT}.
3. In 5MHz 80C86/88 systems, minimum ALE HIGH time = t_{CLCL} - (t_{CHSV}(max) + t_{SVLH}) + t_{CHLL}(min) = 74ns.

Figure 3: Timing Diagrams

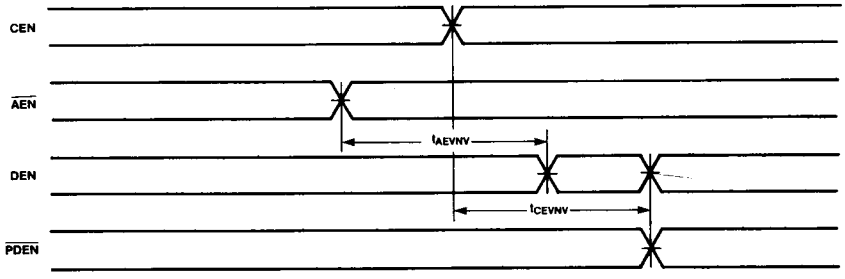
a) Read/Write Timing



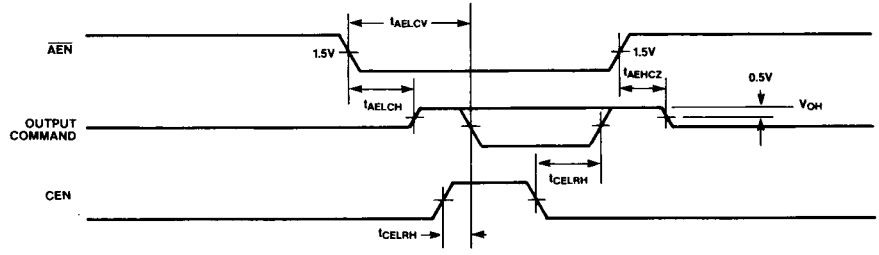
Notes: 1. Address/Data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or STATUS going active, whichever occurs last.

Figure 3: Timing Diagrams (Continued)

b) DEN, PDEN Qualification Timing

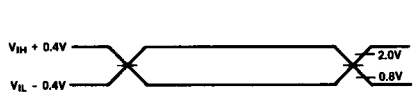


c) Address Enable Timing (3-State Enable/Disable)



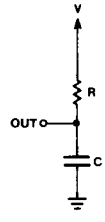
Note: CEN must be LOW or valid prior to S_2 to prevent the command from being generated.

Figure 4: AC Testing I/O Waveform



AC Testing: Inputs are driven at V_{IH} + 0.4V for a logic "1", and V_{IL} - 0.4V for a logic "0". The clock is driven at 3.9V and 0.4V. Timing measurements are made at 2.0V and 0.8V. Input rise and fall times should be ≤15ns measured between 0.8V and 2.0V.

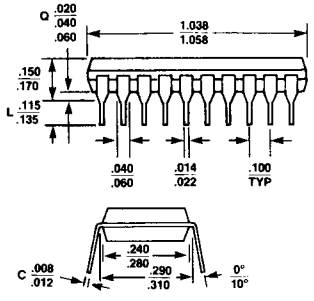
Figure 5: Test Load Circuits 3-State Command Output Test Load



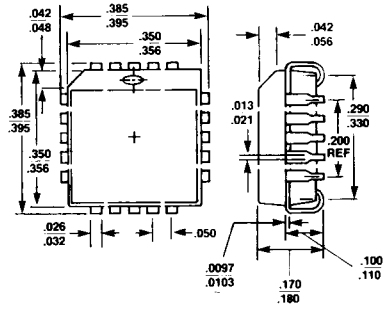
Test Condition	I_{OH}	I_{OL}	V (V)	R (Ω)	C (pF)
A	-4.0mA	+8.0mA	2.13	220	80
B	-8.0mA	+20.0mA	2.29	91	300
C	-8.0mA	—	1.5	187	300
D	-8.0mA	—	1.5	187	50
E	-1.0μA	+1.0μA	2.13	870K	30

PACKAGE DIMENSIONS

Units: Inches



Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C88A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.