

MC54F/74F192 MC54F/74F193

Product Preview

UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

DESCRIPTION — The MC54F/74F192 is an up/down BCD decade (8241) counter. The MC54F/74F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

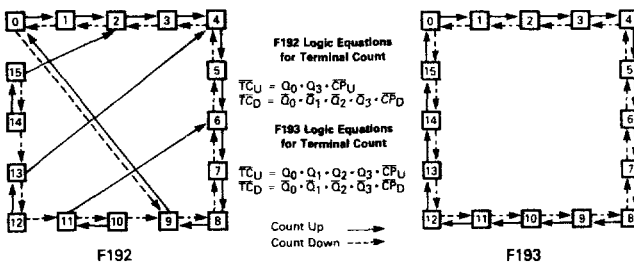
FUNCTION TABLE

MR

	PL	CP _U	CP _D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌋	H	Count Up
L	H	H	⌋	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

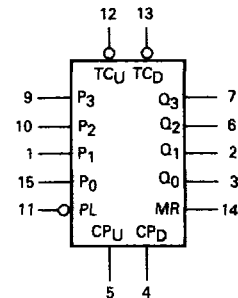
STATE DIAGRAMS



UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

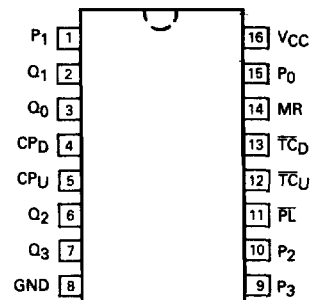
FAST™ SCHOTTKY TTL

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

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FUNCTIONAL DESCRIPTION

The 'F192, 193 are asynchronously presettable counters. The 'F192 is a decade counter while the 'F193 is organized for 4-bit binary operation. They both contain four edge triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When the cir-

cuit has reached the maximum count state; 9 ('F192) or 16 ('F193), the reset HIGH-to-LOW transition of the Count Up Clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the \overline{TC} outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Both the 'F192 and the 'F193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0 - P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54, 74	2.5		V	$I_{OL} = -1.0 \text{ mA}$
		74	2.7		V	$I_{OL} = -1.0 \text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20 \text{ mA}$, $V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current (MR, PL and P_n inputs) (CP inputs)			-0.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5 \text{ V}$
				-1.2		
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current		38	55	mA	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	Maximum Count Frequency	100	125				90		MHz
t _{PLH}	Propagation Delay C _{PJ} or C _{PD} to T _{CU} or T _{CH}	4.0	7.0	9.0			4.0	10	ns
t _{PHL}	Propagation Delay C _{PJ} or C _{PD} to Q _n	3.5	6.0	8.0			3.5	9.0	ns
t _{PLH}	Propagation Delay P _n to Q _n	4.0	6.5	8.5			4.0	9.5	ns
t _{PHL}	Propagation Delay P _n to Q _n	5.5	9.5	12.5			5.5	13.5	ns
t _{PLH}	Propagation Delay P _n to Q _n	3.0	4.5	7.0			3.0	8.0	ns
t _{PHL}	Propagation Delay P _n to Q _n	6.0	11	14.5			6.0	15.5	ns
t _{PLH}	Propagation Delay P _L to Q _n	5.0	8.5	11			5.0	12	ns
t _{PHL}	Propagation Delay P _L to Q _n	5.5	10	13			5.5	14	ns
t _{PHL}	Propagation Delay MR to Q _n	6.5	11	14.5			6.5	15.5	ns
t _{PLH}	Propagation Delay MR to T _{CU}	6.0	10.5	13.5			6.0	14.5	
t _{PHL}	Propagation Delay MR to T _{CD}	7.0	11.5	14.5			7.0	15.5	
t _{PLH}	Propagation Delay P _L to T _{CU} or T _{CD}	7.0	12	15.5			7.0	16.5	ns
t _{PHL}	Propagation Delay P _L to T _{CU} or T _{CD}	7.0	11.5	14.5			7.0	15.5	
t _{PLH}	Propagation Delay P _n to T _{CU} or T _{CD}	7.0	11.5	14.5			7.0	15.5	ns
t _{PHL}	Propagation Delay P _n to T _{CU} or T _{CD}	6.5	11	14			6.5	15	

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F			54F		74F		UNITS
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _s (H)	Set up Time, HIGH or LOW P _n to P _L	6.0					6.0		ns
t _s (L)	Set up Time, HIGH or LOW P _n to P _L	6.0					6.0		
t _h (H)	Hold Time, HIGH or LOW P _n to P _L	4.0					4.0		ns
t _h (L)	Hold Time, HIGH or LOW P _n to P _L	4.0					4.0		
t _w (L)	P _L Pulse Width LOW	6.0					6.0		ns
t _w (L)	C _{PJ} or C _{PD} Pulse Width LOW	5.0					5.0		ns
t _w (L)	C _{PJ} or C _{PD} Pulse Width LOW (Change of Direction)	10					10		ns
t _w (H)	MR Pulse Width HIGH	6.0					6.0		ns
t _{rec}	Recovery Time P _L to C _{PJ} or C _{PD}	6.0					6.0		ns
t _{rec}	Recovery Time MR to C _{PJ} or C _{PD}	4.0					4.0		ns

AC TEST CIRCUIT

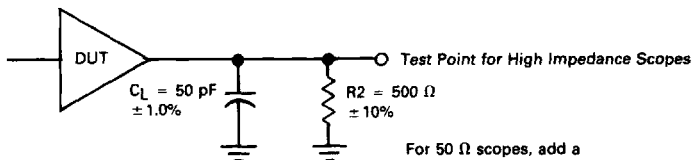


Fig. 1