AGC Transimpedance Amplifier

SONET OC-3
Preliminary
REV 0

FEATURES

- Single +5 Volt Supply
- To Package Compatible
- Automatic Gain Control
- Wide Dynamic Range

APPLICATIONS

- SONET OC-3 Receiver
- FDDI, Ethernet Fiber LAN
- Low Noise RF Amplifier

ELECTRICAL CHARACTERISTICS

(1) (T_A = 25°C, V_{DD} = +5.0V ± 10%, $C_{DIODE}+C_{STRAY}$ = 0.5 pF, DET. CATHODE TO I_{IN})

PARAMETER	MIN	TYP	MAX	UNIT
Transresistance (R_L=∞,I_{DC} <500nA)		17		KΩ
Transresistance (R_L=50Ω) (1)	5.5	8	10	KΩ
Bandwidth -3dB	150	175		MHz
Input Resistance (2)		500		Ω
Output Resistance	30	50	60	Ω
Supply Current		30	45	mA
Input Offset Voltage	1.5	1.6	1.9	Volts
Output Offset Voltage		1.8		Volts
AGC Threshold (I_{IN}) (3)	15	30		µA
Optical Overload (4)	-3	0		dBm
Input Noise Current (5)		14	20	nA
AGC Time Constant (6)		16		µsec
Offset Voltage Drift		1		mV/°C
Optical Sensitivity (7)		- 38		dBm
Operating Voltage Range	+ 4.5	+ 5.0	+ 6.0	Volts
Operating Temperature Range	- 40		85	°C

NOTES

(1) f = 50MH
(2) Measured with I_{IN} below AGC Threshold. During AGC, input impedance will decrease proportionally to I_{IN}.
(3) Defined as the I_{IN} where Transresistance has decreased by 50%.
(4) See note on "Indirect Measurement of Optical Overload".
(5) See note on "Measurement of Input Referred Noise Current".
(6) C_{AGC} = 220 pF
(7) Parameter is guaranteed (not tested) by design and characterization data @155Mb/s, assuming detector responsivity of 0.9.

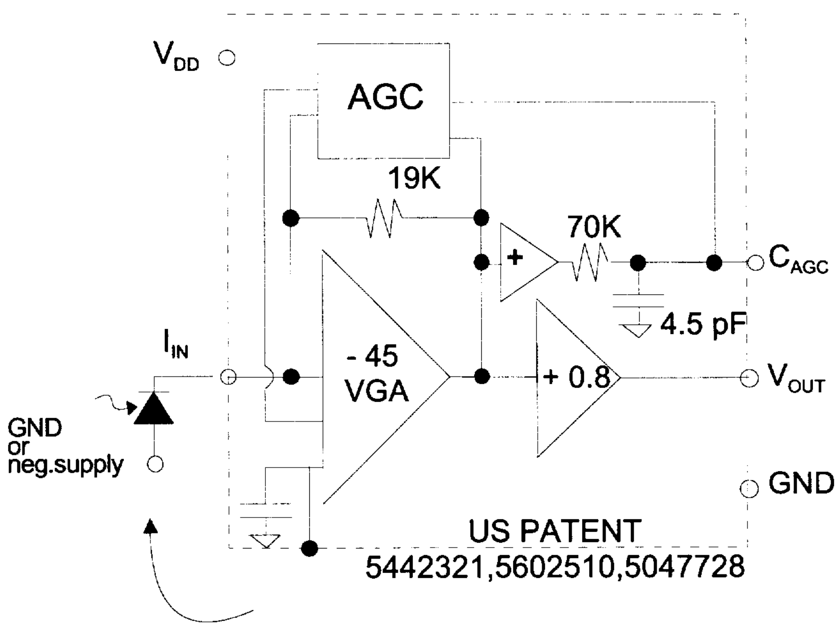
ABSOLUTE MAXIMUM RATINGS

V_{DD}	7.0 V
I_{IN}	5 mA
T_A	Operating Temp. - 40 ^{o}C to 125 ^{o}C
T_S	Storage Temp. - 65 ^{o}C to 150 ^{o}C

PAD DESCRIPTION

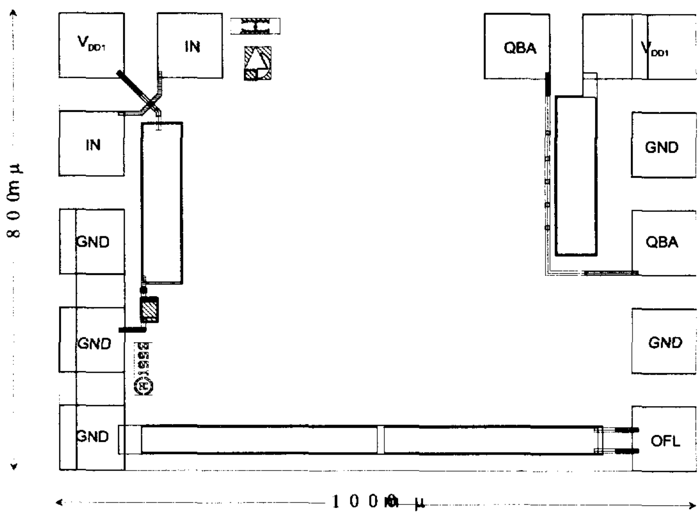
PAD	Description	Comment
V_{DD}	V_{DD}	Positive supply for input gain stage
I_{IN}	TIA Input Current	Connect detector cathode for proper operation
V_{OUT}	TIA Output Voltage	Requires external DC block
C_{AGC}	External AGC Capacitor	70K * (C_{AGC} * 4.5 pF) = AGC time constant

ATA01504D1C EQUILVALENT CIRCUIT

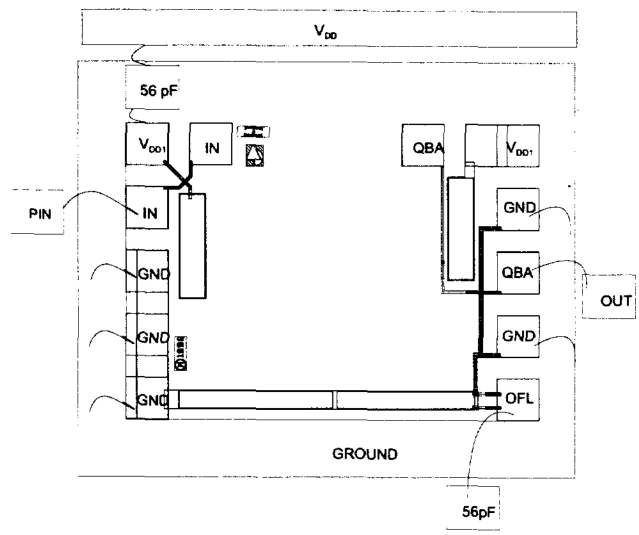


Photodector cathode must be connected to I_{IN} for proper AGC operation

BONDING PADS



TYPICAL BONDING



POWER SUPPLY CONSIDERATIONS

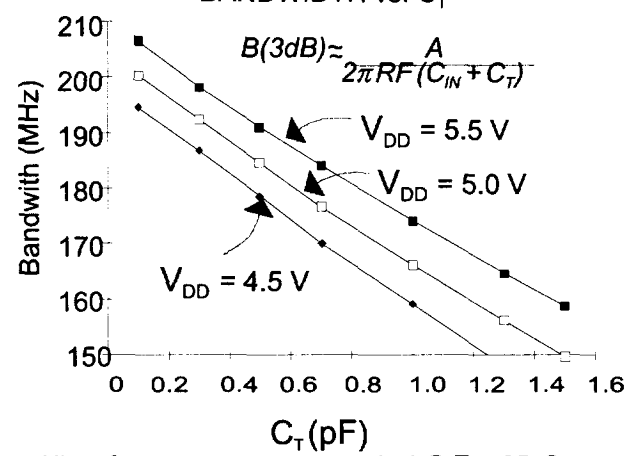
The ATA01504D1C may be operated from a positive supply as low as + 4.5 V and as high as + 6.0 V. Below + 4.5 V, bandwidth, overload and sensitivity will degrade, while at + 6.0 V, bandwidth, overload and sensitivity improves. Use of surface mount (preferably MIM type capacitors), low inductance power supply bypass capacitors (>=56pF) are essential for good high frequency and low noise performance. The power supply bypass capacitors should be mounted on or connected to a good low inductance ground plane.

GENERAL LAYOUT CONSIDERATIONS

The ATA01504D1C has been designed with two bond pads for the I_{IN}, V_{OUT}, and V_{DD} connections. These multiple bond pads are arranged in such a way to offer the greatest flexibility in bonding configurations of the die. Furthermore, it is only necessary to bond to one of the two pads as they are connected on-chip. Thus, the need to cross bond wires has been eliminated making the ATA01504D1C TO package compatible.

Since the gain stages of the transimpedance amplifier have an open loop bandwidth in excess of 1.0 GHz, it is essential to maintain good high frequency layout practices. To prevent oscillations, a low inductance RF ground plane should be made available for power supply bypassing. Traces that can be made short should be made short, and the utmost care should be taken to maintain very low capacitance at the photodiode TIA interface (I_{IN}), as excess capacitance at this node will cause a degradation in bandwidth and sensitivity (see Bandwidth vs C_T curves).

BANDWIDTH vs. C_T



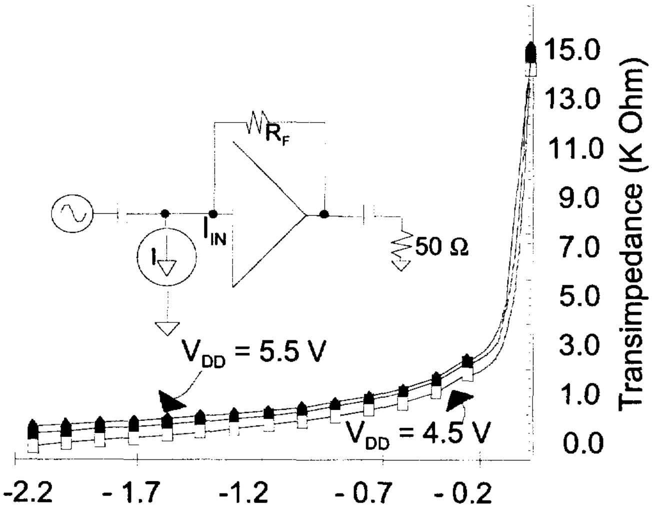
Note: All performance curves are typical @ T_A =25°C unless otherwise noted

ATA

I_{IN} CONNECTION

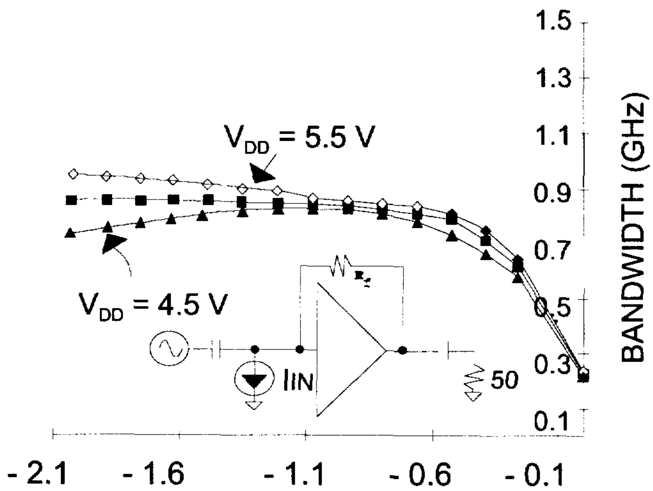
(Refer to the equivalent circuit diagram.) Bonding the detector cathode to I_{IN} (and thus drawing current from the ATA01504) improves the dynamic range. Although the detector may be used in the reverse direction for input currents not exceeding 250 mA, the specifications for optical overload will not be met.

Transimpedance vs I_{IN}



I_{IN} (mA DC)

Bandwidth vs I_{IN}



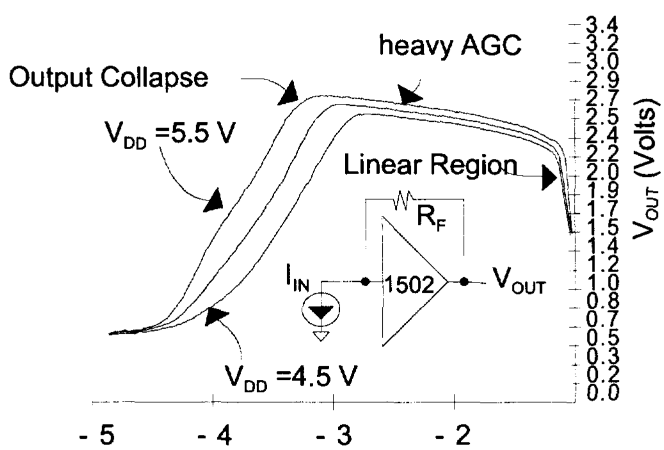
I_{IN} (mA DC)

ATA

V_{OUT} CONNECTION

The output pad should be connected via a coupling capacitor to the next stage of the receiver channel (filter or decision circuits), as the output buffers are not designed to drive a DC coupled 50 ohm load (this would require an output bias current of approximately 36 mA to maintain a quiescent 1.8 Volts across the output load). If V_{OUT} is connected to a high input impedance decision circuit (>500 ohms), then a coupling capacitor may not be required, although caution should be exercised since DC offsets of the photo detector/TIA combination may cause clipping of subsequent gain or decision circuits.

V_{OUT} vs I_{IN}



I_{IN} (mA DC)

SENSITIVITY AND BANDWIDTH

In order to guarantee sensitivity and bandwidth performance, the TIA is subjected to a comprehensive series of tests at the die sort level (100% testing at 25 °C) to verify the DC parametric performance and the high frequency performance (i.e. adequate |S21|) of the amplifier. Acceptably high |S21| of the internal gain stages will ensure low amplifier input capacitance and hence low input referred noise current. Transimpedance sensitivity and bandwidth are then guaranteed by design and correlation with RF and DC die sort test results.

INDIRECT MEASUREMENT OF OPTICAL OVERLOAD

Optical overload can be defined as the maximum optical power above which the BER (bit error rate) increases beyond 1 error in 10^{10} bits. The ATA01504D1C is 100% tested at die sort by a DC measurement which has excellent correlation with an PRBS optical overload measurement. The measurement consists of sinking a negative current (see V_{OUT} vs I_{IN} figure) from the TIA and determining the point of output voltage collapse. Also the input node virtual ground during "heavy AGC" is checked to verify that the linearity (i.e. pulse width distortion) of the amplifier has not been compromised.

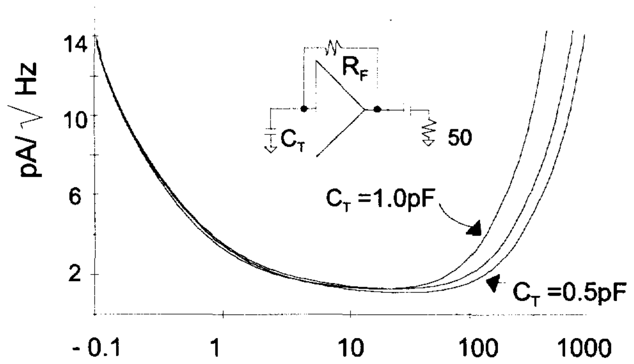
MEASUREMENT OF INPUT REFERRED NOISE CURRENT

The "Input Noise Current" is directly related to sensitivity. It can be defined as the output noise voltage (V_{OUT}), with no input signal, (including a 110 MHz lowpass filter at the output of the TIA) divided by the AC transresistance.

AGC CAPACITOR

It is important to select an external AGC capacitor of high quality and appropriate size. The ATA01504D1C has an on-chip 70KW resistor with a shunt 4.5 pF capacitor to ground. Without external capacitance the chip will provide an AGC time constant of 280 nS. For the best performance in a typical 155MB/s SONET receiver, a minimum AGC capacitor of 56pF is recommended. This will provide the minimum

Input Referred Noise Spectral Density
vs
Frequency



amount of protection against pattern sensitivity and pulse width distortion on repetitive data sequences during high average optical power conditions. Conservative design practices should be followed when selecting an AGC capacitor, since unit to unit variability of the internal time constant and various data conditions can lead to data errors if the chosen value is too small.

PHASE RESPONSE

At frequencies below the 3 dB bandwidth of the device, the transimpedance phase response is characteristic of a single pole transfer function (as shown in the Phase vs Frequency curve). The output impedance is essentially resistive up to 1000 MHz.

Phase (I_{IN} to V_{OUT})