Integrated Device Technology, Inc.

128K x 8 CMOS STATIC RAM MODULE

IDT8MP824L

FEATURES:

- High-density 1 megabit CMOS static RAM module
- Fast access time
  — 70ns (max.)
- Low-power consumption
  — Active: less than 400mW (typ.)
  — Standby: less than 50µW (typ.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 30-pin SIP (Single In-line Package) for maximum space-savings
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

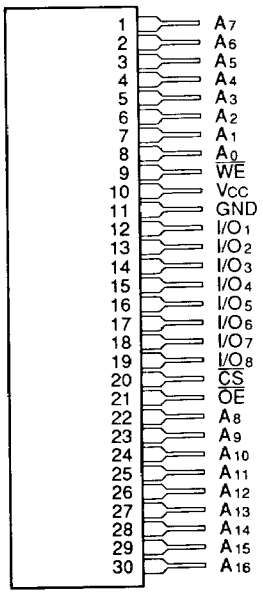
The IDT8MP824L is 128K x 8 high-speed CMOS static RAM constructed on an epoxy laminate substrate using four 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} and A_{16} to select one of the four 32K x 8 RAMs.

The IDT8MP824L is available with maximum access times as fast as 70ns for commercial range, with maximum power consumption of 660mW. The module also offers a full standby mode of 2.2mW (max.).

The IDT8MP824L is offered in a 30-pin SIP (Single In-line Package). For the 32-pin JEDEC sidebrazed DIP, refer to the IDT8M824S module.

All inputs and outputs of the IDT8MP824L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

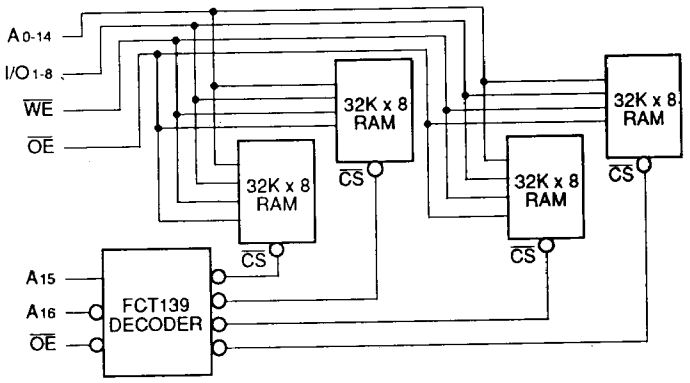
PIN CONFIGURATION[1]



2716 drw 01

SIP
BACK VIEW

FUNCTIONAL BLOCK DIAGRAM



2716 drw 02

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power Supply
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

2716 tbl 01

NOTE:
1. For module dimensions, please refer to module drawing M36 in the packaging section.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2716 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2716 tbl 03

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2716 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP824L Min.	IDT8MP824L Typ.(1)	IDT8MP824L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS} \le V_{IL}$ V_{CC} = Max., Output Open f = 0	—	10	80	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS} \le V_{IL}$ V_{CC} = Max., Output Open f = f_{MAX}	—	80	120	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \ge V_{IH}$ V_{CC} = Max., Output Open f = f_{MAX}	—	6	12	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or < 0.2V	—	10	400	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA, V_{CC} = Min.	2.4	—	—	V

NOTE: 2716 tbl 05

1. V_{CC} = 5V, T_A = +25°C

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2716 tbl 06

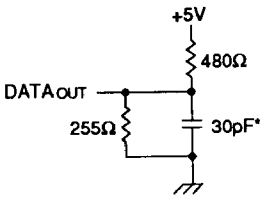
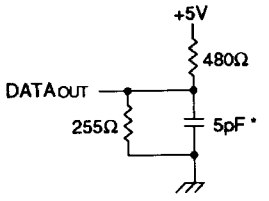


Figure 1. Output Load



2716 drw 03

Figure 2. Output Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameters	IDT8MP824L70 Min.	IDT8MP824L70 Max.	IDT8MP824L85 Min.	IDT8MP824L85 Max.	IDT8MP824L100 Min.	IDT8MP824L100 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	70	—	85	—	100	—	ns
tAA	Address Access Time	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	70	—	85	—	100	ns
tCLZ (1)	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
tOE	Output Enable to Output Valid	—	40	—	50	—	60	ns
tOLZ (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
tCHZ (1)	Chip Select to Output in High Z	—	30	—	35	—	40	ns
tOHZ (1)	Output Disable to Output in High Z	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	70	—	85	—	100	ns
WRITE CYCLE								
tWC	Write Cycle Time	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	65	—	75	—	90	—	ns
tAW	Address Valid to End of Write	65	—	75	—	90	—	ns
tAS	Address Setup Time	5	—	5	—	5	—	ns
tWP	Write Pulse Width	60	—	70	—	80	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	ns
tWHZ (1)	Write Enable to Output in High Z	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time	5	—	5	—	5	—	ns
tOW (1)	Output Active from End of Write	5	—	5	—	5	—	ns

2716 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

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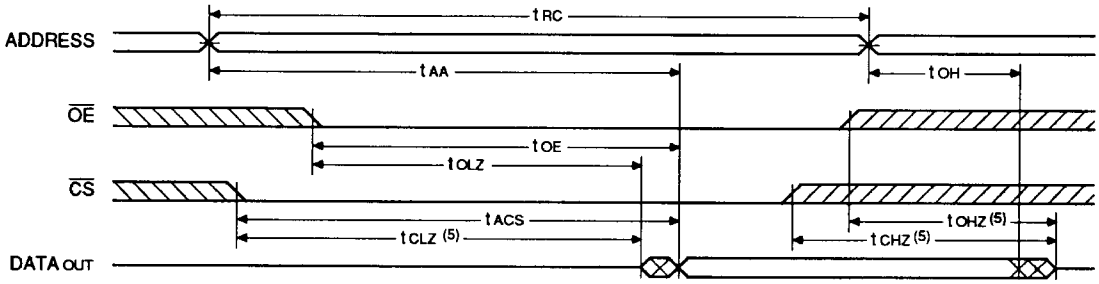
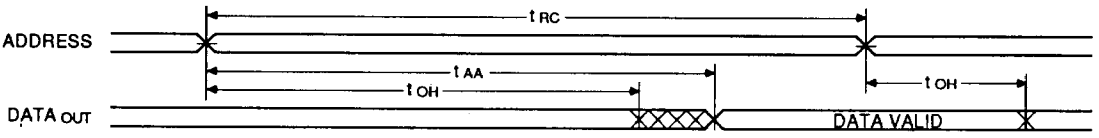
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



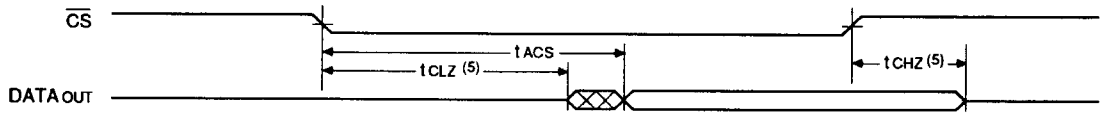
2716 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2716 drw 05

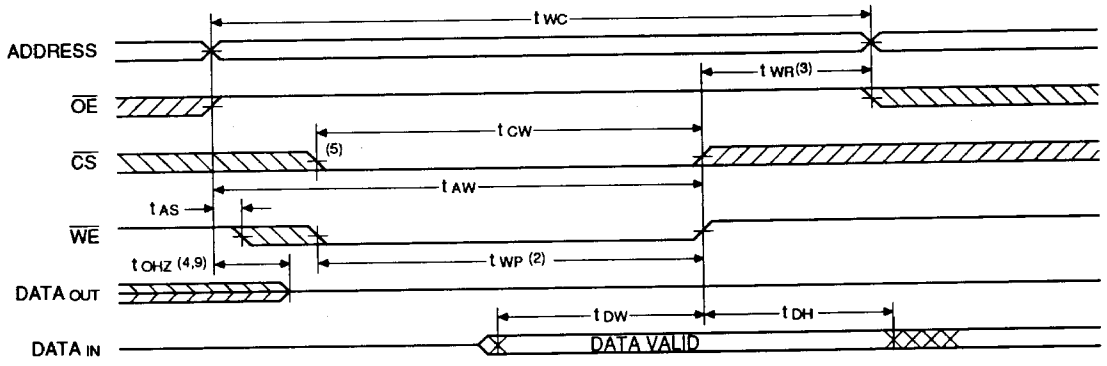
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2716 drw 06

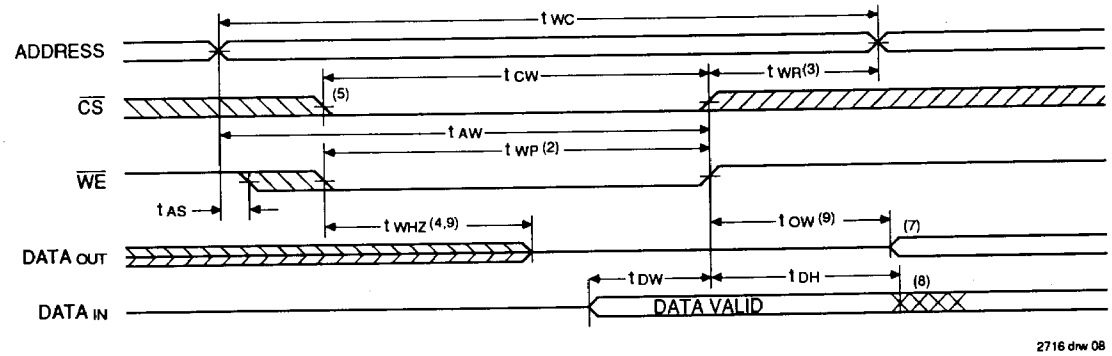
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2716 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2716 drw 08

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DIN	Active

2716 tbl 08

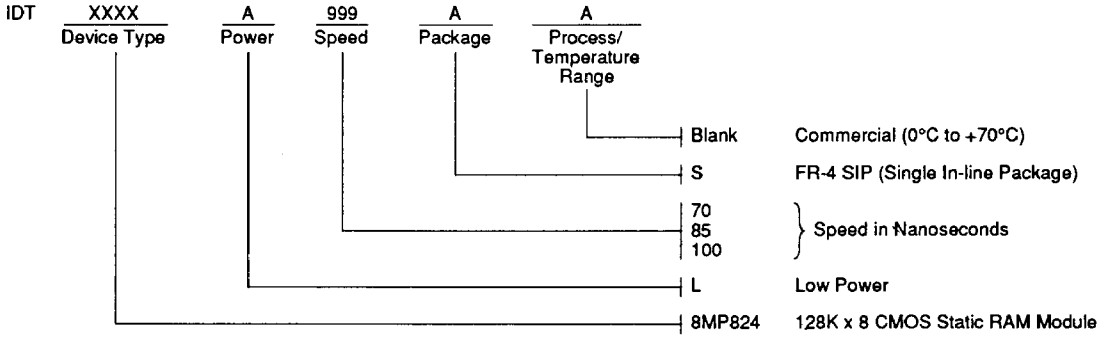
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2716 tbl 09

ORDERING INFORMATION



2716 drw 10