MH25632XJ,SXJ-8,-10

MITSUBISHI (MEMORY/ASIC)

FAST PAGE MODE 8388608-BIT(262144-WORD BY 32-BIT)DYNAMIC RAM

DESCRIPTION

MH25632XJ, SXJ is 262144-word by 32-bit dynamic RAM module. This consists of two industry standard 256K × 16bit dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package. This is a socket-type memory module, suitable for easy interchange or addition of module.

FEATURES

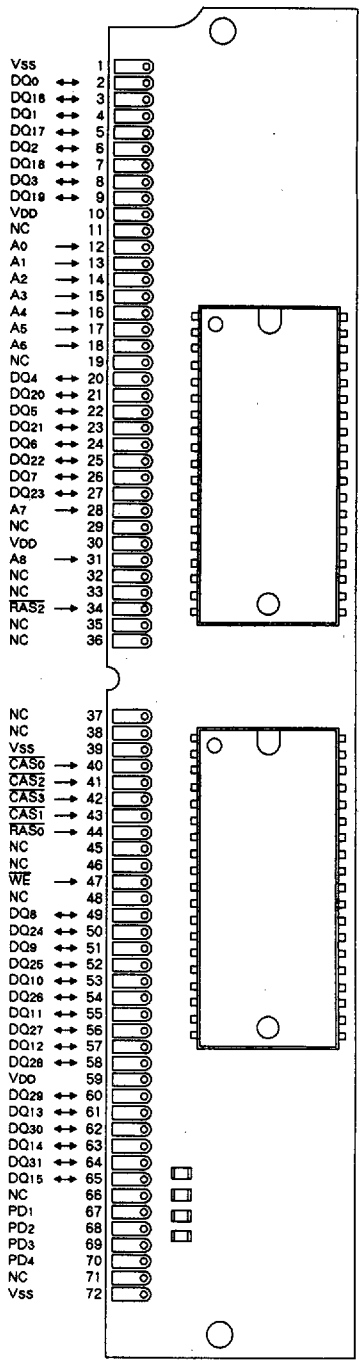
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH25632XJ, SXJ-8	80	20	40	160	1160
MH25632XJ, SXJ-10	100	25	50	190	1000

- 72-pins single in-line package
- Single 5V ± 10% supply
- Low stand-by power dissipation
  22.0mW (max) ·····CMOS Input level
- Operating power dissipation
  MH25632XJ, SXJ-8 ····· 1540mW (max)
  MH25632XJ, SXJ-10 ····· 1320mW (max)
- Fast-page mode, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- All inputs, output TTL compatible and low capacitance
- 512 refresh cycle every 8ms (A_0~A_8)
  MH25632XJ is gold contact
  MH25632SXJ is solder contact

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



	-8	-10
PD1	Vss	Vss
PD2	NC	NC
PD3	NC	Vss
PD4	Vss	Vss

Outline 72N9

NC : NO CONNECTION

MITSUBISHI ELECTRIC

FUNCTION

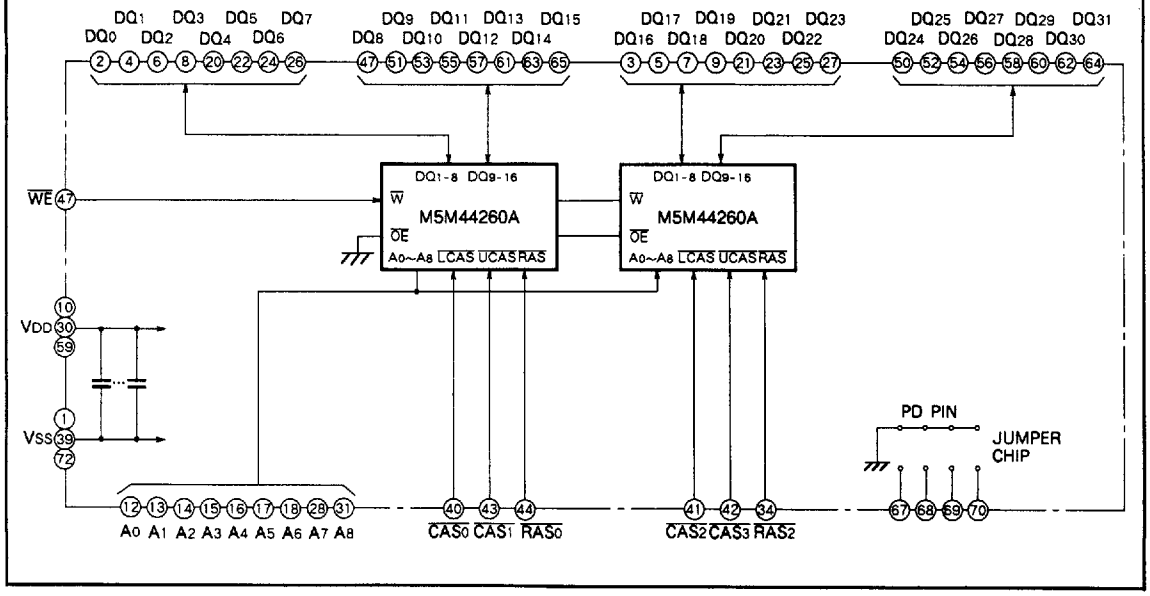
MH25632XJ, SXJ provide, in addition to normal read, write and operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh. The input conditions for each shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs							Input/Output			
	$\overline{RAS_0}$	$\overline{RAS_2}$	$\overline{CAS_0}$	$\overline{CAS_1}$	$\overline{CAS_2}$	$\overline{CAS_3}$	$\overline{W}$	DQ_0~ DQ_7	DQ_8~ DQ_{15}	DQ_{16}~ DQ_{23}	DQ_{24}~ DQ_{31}
DQ_0~ DQ_7 read	ACT	NAC	ACT	NAC	NAC	NAC	NAC	DOUT	OPN	OPN	OPN
DQ_8~ DQ_{15} read	ACT	NAC	NAC	ACT	NAC	NAC	NAC	OPN	DOUT	OPN	OPN
DQ_{16}~DQ_{23} read	NAC	ACT	NAC	NAC	ACT	NAC	NAC	OPN	OPN	DOUT	OPN
DQ_{24}~DQ_{31} read	NAC	ACT	NAC	NAC	NAC	ACT	NAC	OPN	OPN	OPN	DOUT
DQ_0~ DQ_{15} read	ACT	NAC	ACT	ACT	NAC	NAC	NAC	DOUT	DOUT	OPN	OPN
DQ_{16}~DQ_{31} read	NAC	ACT	NAC	NAC	ACT	ACT	NAC	OPN	OPN	DOUT	DOUT
DQ_0~ DQ_{31} read	ACT	ACT	ACT	ACT	ACT	ACT	NAC	DOUT	DOUT	DOUT	DOUT
DQ_0~ DQ_7 write	ACT	NAC	ACT	NAC	NAC	NAC	ACT	DIN	OPN	OPN	OPN
DQ_8~ DQ_{15} write	ACT	NAC	NAC	ACT	NAC	NAC	ACT	OPN	DIN	OPN	OPN
DQ_{16}~DQ_{23} write	NAC	ACT	NAC	NAC	ACT	NAC	ACT	OPN	OPN	DIN	OPN
DQ_{24}~DQ_{31} write	NAC	ACT	NAC	NAC	NAC	ACT	ACT	OPN	OPN	OPN	DIN
DQ_0~ DQ_{15} write	ACT	NAC	ACT	ACT	NAC	NAC	ACT	DIN	DOUT	OPN	OPN
DQ_{16}~DQ_{31} write	NAC	ACT	NAC	NAC	ACT	ACT	ACT	OPN	OPN	DIN	DIN
DQ_0~ DQ_{31} write	ACT	ACT	ACT	ACT	ACT	ACT	ACT	DIN	DIN	DIN	DIN
$\overline{RAS}$-only refresh	ACT	ACT	NAC	NAC	NAC	NAC	DNC	OPN	OPN	OPN	OPN
Hidden refresh	ACT	ACT	ACT	ACT	ACT	ACT	DNC	DOUT	DOUT	DOUT	DOUT
	ACT	NAC	ACT	ACT	ACT	ACT	DNC	DOUT	DOUT	DOUT	DOUT
	NAC	ACT	ACT	ACT	ACT	ACT	DNC	DOUT	DOUT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$	ACT	ACT	ACT	ACT	ACT	ACT	DNC	OPN	OPN	OPN	OPN
refresh stand by	NAC	NAC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	2	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 6.5V Other input pins = 0V	−20		20	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3, 4, ∗)	MH25632XJ, SXJ-8	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open			280	mA
		MH25632XJ, SXJ-10				240	
I_{CC2}	Supply current from Vcc, stand-by		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			4	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5			2	
$I_{CC3(AV)}$	Average supply current from Vcc refreshing (Note 3, ∗)	MH25632XJ, SXJ-8	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min output open			280	mA
		MH25632XJ, SXJ-10				240	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3, 4, ∗)	MH25632XJ, SXJ-8	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min, output open			280	mA
		MH25632XJ, SXJ-10				240	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH25632XJ, SXJ-8	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open			280	mA
		MH25632XJ, SXJ-10				240	

Note 2 : Current flowing into an IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
∗ : Column Address can be changed once or less while $\overline{RAS}n$ = V_{IL} and $\overline{CAS}n$ = V_{IH}. (n = 0~3)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_I = 25mVrms			25	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				29	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				22	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				22	pF
$C_{I/O}$	Input/Output capacitance, data ports				22	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10 %, V_{SS} = 0V, unless otherwise noted. See notes 5, 12, 13)

Symbol	Parameter		Limits				Unit
			MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		80		100	ns
t_{AA}	Column Address time	(Note 6, 9)		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		45		55	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	12	0	25	ns

Note 5 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 8 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.

7 : Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8 : Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table. t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

9 : Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

10 : Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11 : $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10\ \mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 5V ± 10 %, V_{SS} = 0V, unless otherwise noted. See notes 12, 13)

Symbol	Parameter		Limits				Unit
			MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
			Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8	ms
t_{RP}	RAS high pulse width		60		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		20		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note 18)	20		25		ns
t_T	Transition time	(Note 19)	1	50	1	50	ns

Note 12 : The timing requirements are assumed t_T = 5ns.

13 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14 : $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.

15 : $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

16 : $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

17 : Either t_{DZC} or t_{DZO} must be satisfied.

18 : Either t_{CDD} or t_{ODD} must be satisfied.

19 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	150		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time $\overline{CAS}$ high (Note 20)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	40		50		ns

Note 20 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter	Limits				Unit
		MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	150		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		20		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	20		25		ns
t_{WP}	Write pulse width	15		20		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	15		20		ns

Read-Write Cycles

Symbol	Parameter	Limits				Unit
		MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 21)	205		245		ns
t_{RAS}	$\overline{RAS}$ low pulse width	125	10000	155	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	65	10000	80	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	125		155		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	65		80		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 22)	40		50		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 22)	100		125		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 22)	60		75		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	20		25		ns
t_{RWL}	$\overline{RAS}$ hold time, after $\overline{W}$ low	20		25		ns
t_{WP}	Write pulse width	15		20		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	15		20		ns

Note 21 : t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.
22 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle, If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Cycle) (Note 23)

Symbol	Parameter	Limits				Unit
		MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	50		60		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	100		115		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	135	100000	160	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	10	20	10	25	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	45		55		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	45		55		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24 : $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
25 : $t_{CP(max)}$ is specified as a reference point only.

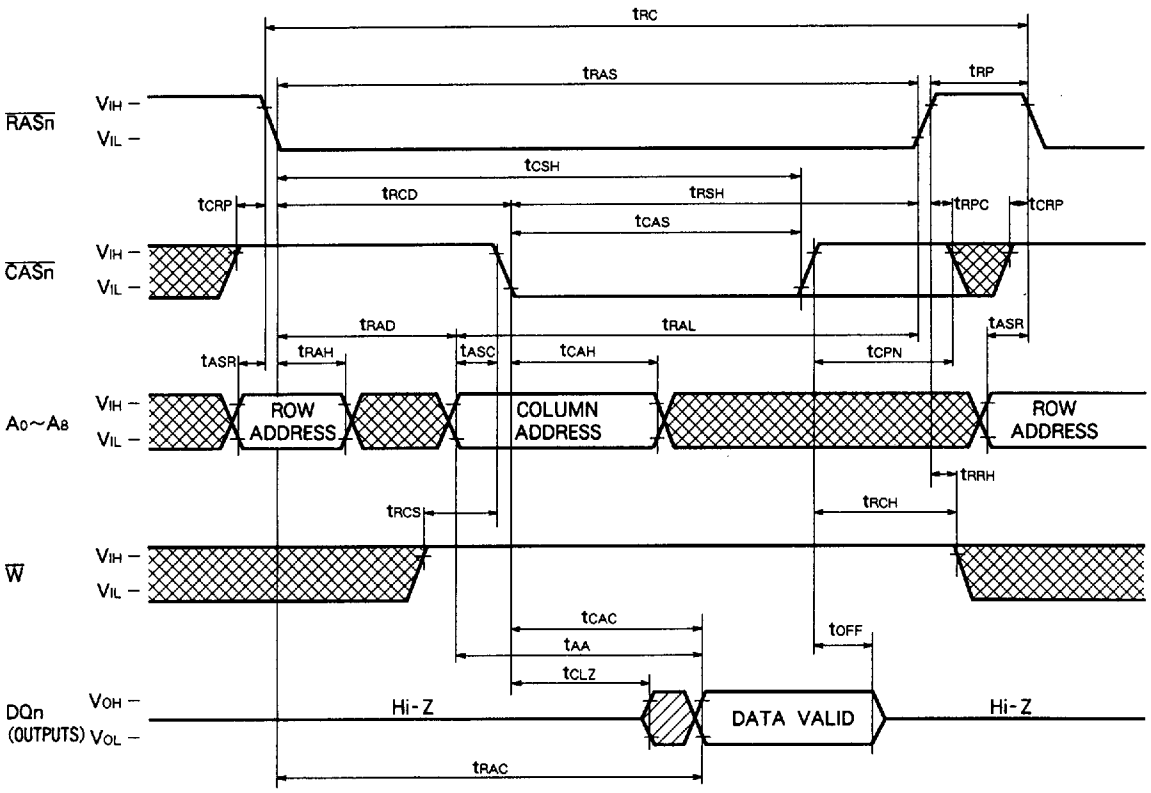
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		MH25632XJ, SXJ-8		MH25632XJ, SXJ-10		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		20		ns
t_{RSR}	Read set up time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	15		20		ns

Note 26 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 27)

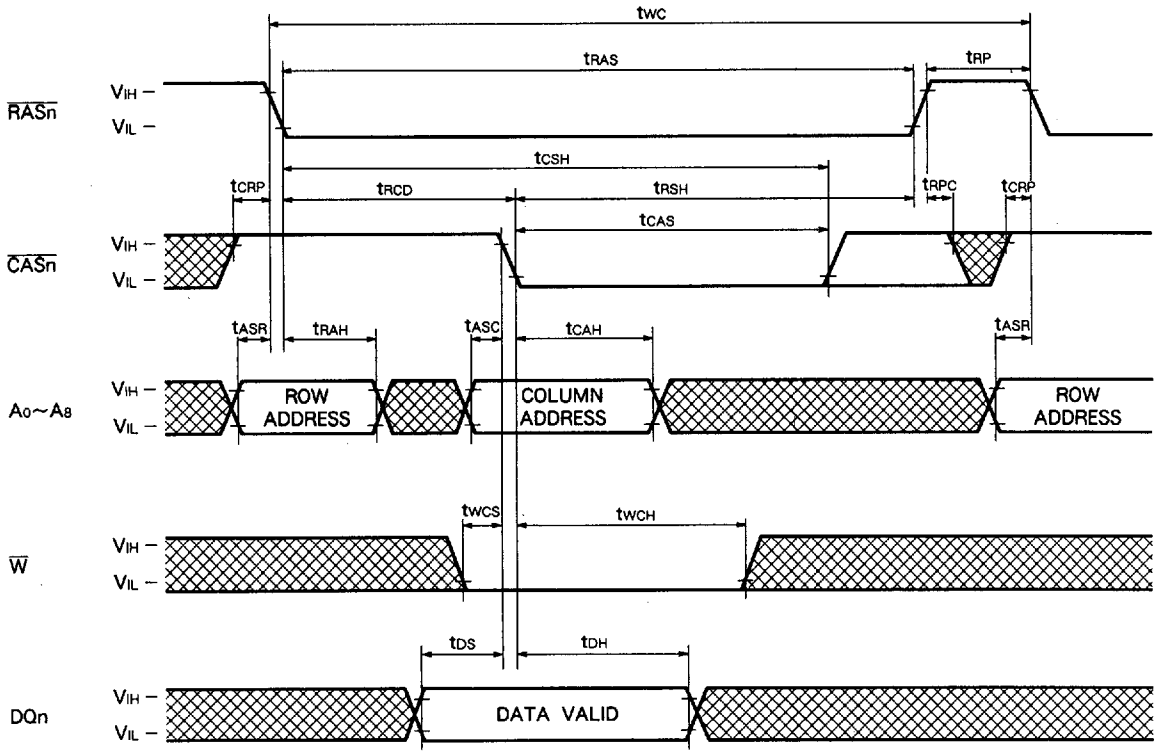
Read Cycle



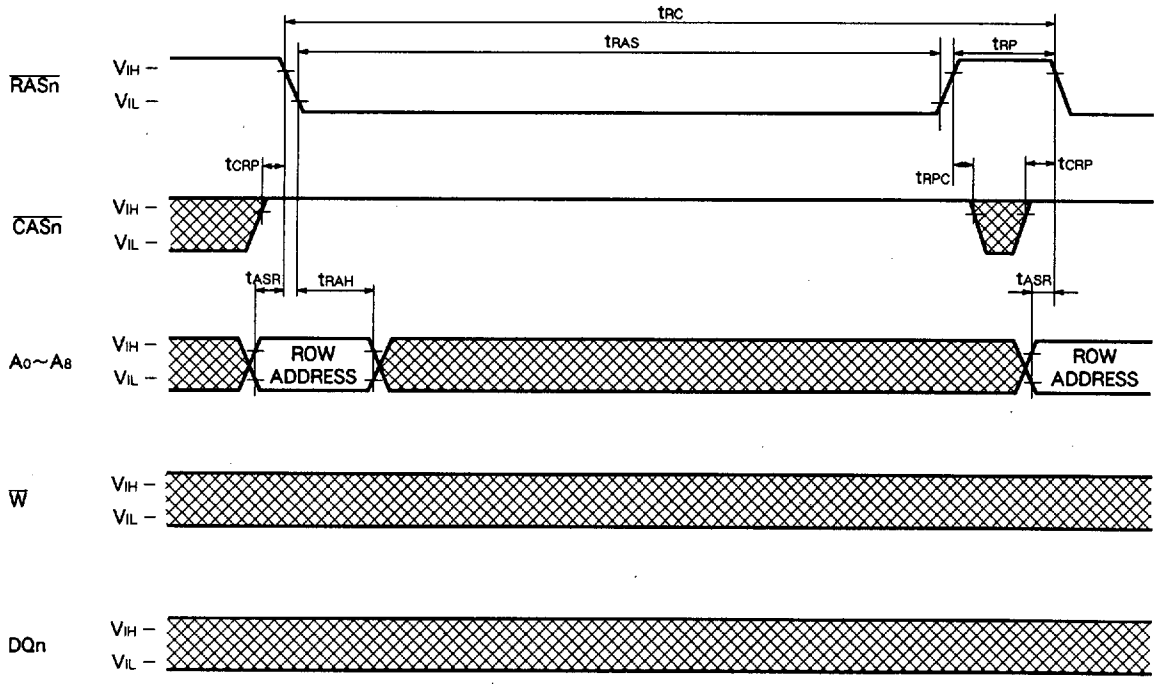
Note 27. Indicates the don't care input.
$V_{IH}(min) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min) \leq V_{IN} \leq V_{IL}(max)$

Indicates the invalid output.

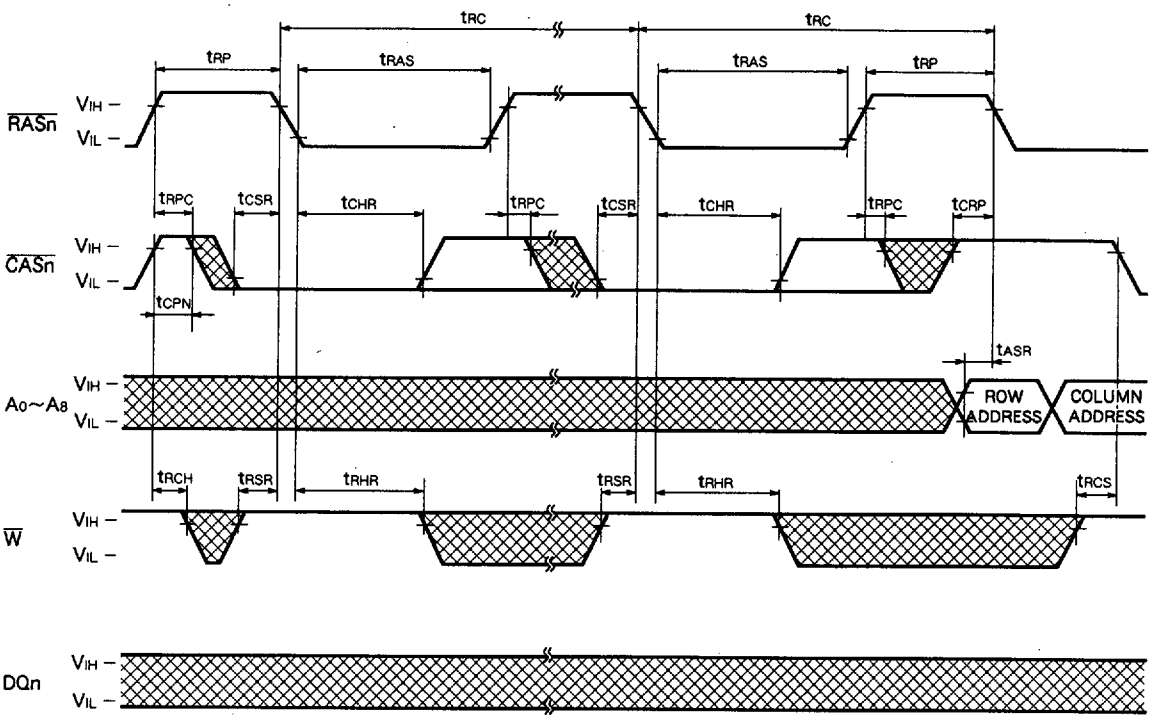
Write Cycle (Early Write)



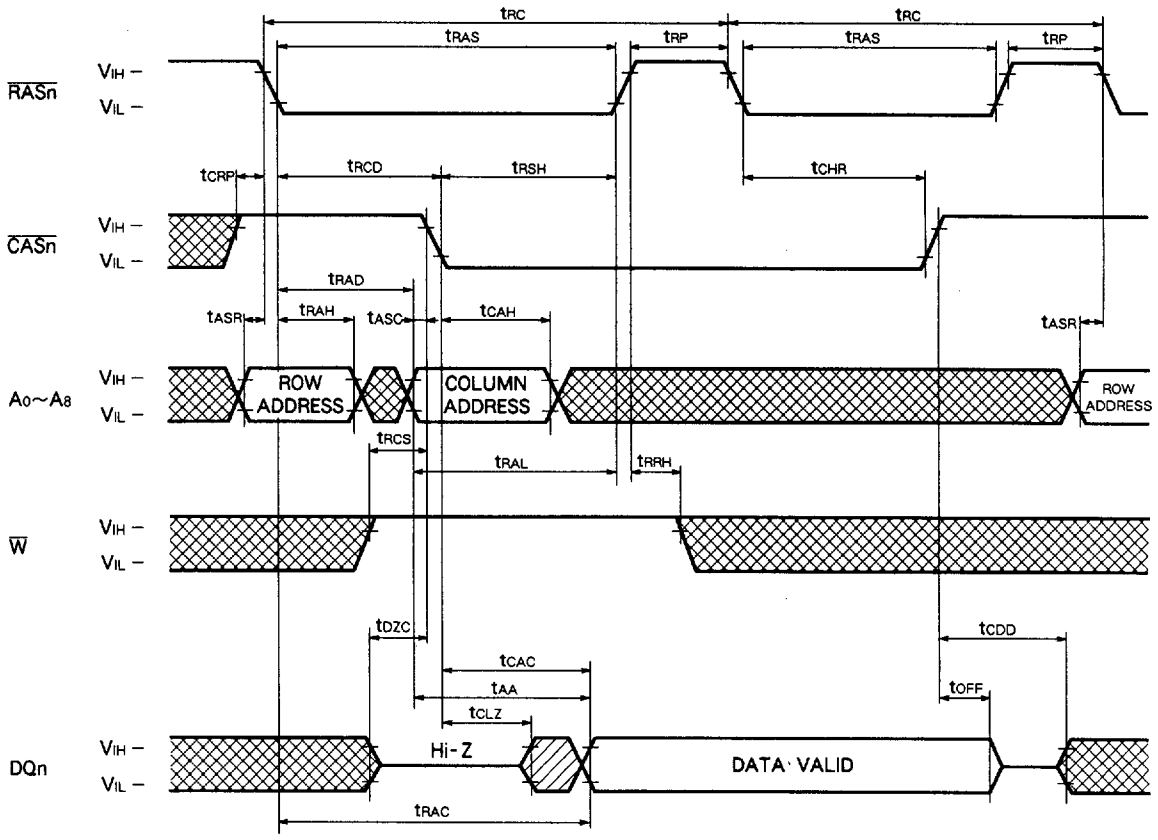
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

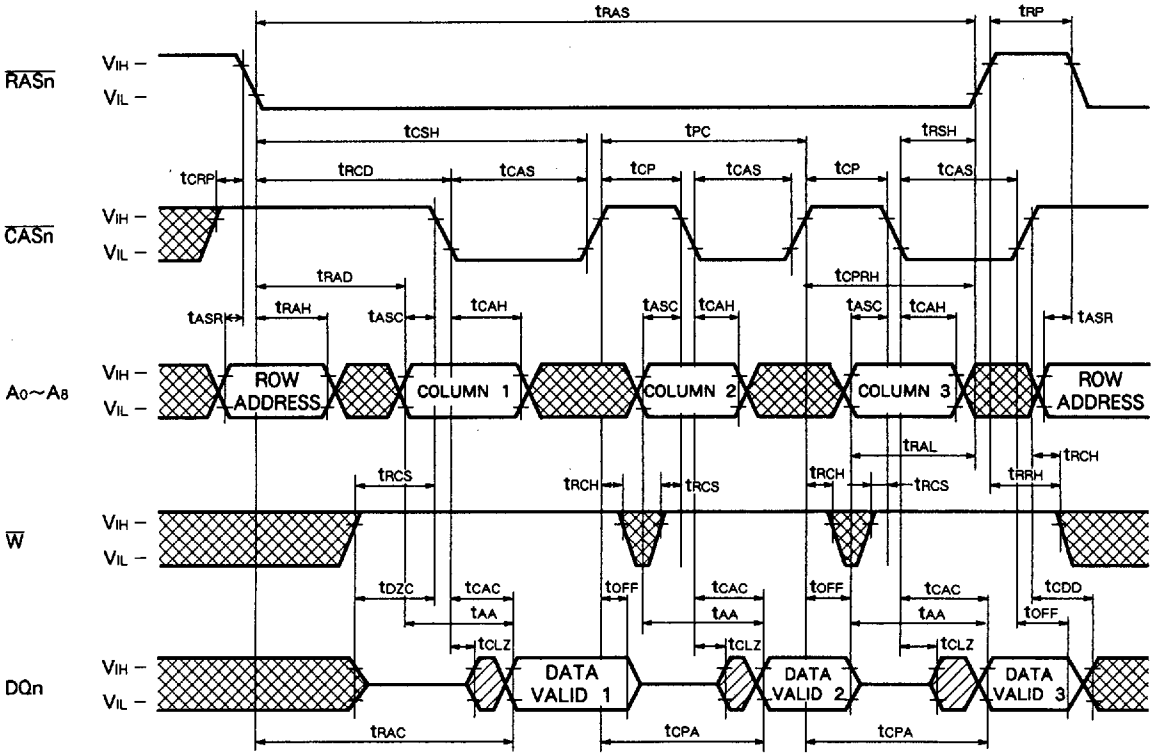


Hidden Refresh Cycle (Read) (Note 28)



Note 28 : Early write, read write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)