

**FEATURES**

**40 MSPS Conversion Speed**  
**Low Power: < 1 W**  
**On-Board T/H**  
**2 V p-p Analog Input**  
**Fully Characterized Dynamic Performance**

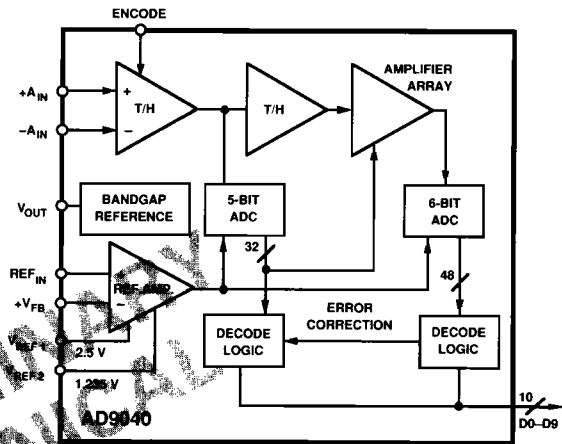
**APPLICATIONS**

**Medical Imaging**  
**Digital Oscilloscopes**  
**Professional Video**  
**Communications**  
**Advanced Television (MUSE Decoders)**

**GENERAL DESCRIPTION**

The AD9040 is a complete 10-bit sampling analog-to-digital converter (ADC) with on-board track-and-hold. The unit is designed for low cost, high performance applications and requires only an encode signal to achieve 40 MSPS sample rates with 10-bit resolution.

Digital inputs and outputs are TTL/CMOS compatible. The analog input requires a signal of 2 V p-p amplitude and can be driven differentially. The two-step architecture used in the AD9040 is optimized to provide the best dynamic performance available while maintaining low power requirements.

**FUNCTIONAL BLOCK DIAGRAM**


# AD9040—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = V_{CC} = +5\text{ V}$ ;  $V_{SS} = V_{EE} = -5\text{ V}$ ; ENCODE = 40.5 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9040JN/JP			AD9040KN/KP			AD9040TE/TQ			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			10			10			10			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		TBD	TBD		0.5	1.0		0.5	1.0	LSB
	Full	VI			TBD			1.0			1.0	LSB
Integral Nonlinearity	-25°C	I		TBD	TBD		0.5	1.0		0.5	1.0	LSB
	Full	VI			TBD			1.0			1.0	LSB
No Missing Codes	Full	VI				Guaranteed			Guaranteed			
Gain Error	+25°C	I		TBD	TBD		TBD	TBD		TBD	TBD	% FS
	Full	VI			TBD			TBD			TBD	% FS
Gain Tempo	Full	V		TBD			TBD			TBD		ppm/°C
ANALOG INPUT												
Input Voltage Range	+25°C	V		2			2			2		V p-p
Input Offset Voltage	+25°C	I			20			20			20	mV
	Full	VI			25			25			40	mV
Input Bias Current	+25°C	I			1.0			1.0			1.0	μA
	Full	VI			2.0			2.0			2.0	μA
Input Resistance	+25°C	III		100			100			100		kΩ
Input Capacitance	+25°C	III			10			10			10	pF
Analog Bandwidth	+25°C	III	50			50			50			MHz
BANDGAP REFERENCE												
Output Voltage	+25°C	I	TBD	1.2	TBD	TBD	1.2	TBD	TBD	1.2	TBD	V
	Full	VI	TBD		TBD	TBD		TBD	TBD		TBD	V
Temperature Coefficient	Full	V		TBD			TBD			TBD		ppm/°C
SWITCHING PERFORMANCE												
Conversion Rate	+25°C	I	40			40			40			MSPS
Aperture Delay ( $t_A$ )	+25°C	V		5			5			5		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5			5		ps rms
Output Delay ( $t_{OD}$ ) <sup>1</sup>	+25°C	I	TBD	4	TBD	TBD	4	TBD	TBD	4	TBD	ns
	Full	VI	TBD		TBD	TBD		TBD	TBD		TBD	ns
Output Time Skew <sup>1</sup>	+25°C	IV		2			2			2		ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		TBD			TBD			TBD		ns
Overshoot Recovery Time	+25°C	V		TBD			TBD			TBD		ns
Effective Number of Bits (ENOB)												Bits
$f_{IN} = 2.3\text{ MHz}$	+25°C	I	9.0			9.0			9.0			Bits
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	9.0			9.0			9.0			Bits
Signal-to-Noise Ratio <sup>2</sup>												dB
$f_{IN} = 2.3\text{ MHz}$	+25°C	I	56	58		56	58		56	58		dB
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	56	58		56	58		56	58		dB
Signal-to-Noise Ratio <sup>2</sup> (without harmonics)												dB
$f_{IN} = 2.3\text{ MHz}$	+25°C	I	56	58		56	58		56	58		dB
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	56	58		56	58		56	58		dB
2nd Harmonic Distortion												dBc
$f_{IN} = 2.3\text{ MHz}$	+25°C	I	70			70			70			dBc
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	62			62			62			dBc
3rd Harmonic Distortion												dBc
$f_{IN} = 2.3\text{ MHz}$	+25°C	I	70			70			70			dBc
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	62			62			62			dBc
Two-Tone Intermodulation Distortion Rejection <sup>3</sup>	+25°C	V		TBD			TBD			TBD		dBc
Differential Phase	+25°C	III		0.5			0.5			0.5		Degree
Differential Gain	+25°C	III		1			1			1		%

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter (Conditions)	Temp	Test Level	AD9040JN/JP			AD9040KN/KP			AD9040TE/TQ			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>ENCODE INPUT</b>												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI		0.8			0.8			0.8		V
Logic "1" Current	Full	VI		10			10			10		μA
Logic "0" Current	Full	VI		10			10			10		μA
Input Capacitance	+25°C	V		5			5			5		pF
Encode Pulse Width (High) ( $t_{EH}$ ) <sup>4</sup>	+25°C	IV	TBD			TBD			TBD			ns
Encode Pulse Width (Low) ( $t_{EL}$ ) <sup>4</sup>	+25°C	IV	TBD			TBD			TBD			ns
<b>DIGITAL OUTPUTS</b>												
Logic "1" Voltage ( $I_{OH} = 2$ mA)	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage ( $I_{OL} = 10$ mA)	Full	VI		0.4			0.4			0.4		V
<b>POWER SUPPLY</b>												
$V_{DD}$ Supply Current	Full	VI		TBD			TBD			TBD		mA
$V_{CC}$ Supply Current	Full	VI		TBD			TBD			TBD		mA
$V_{SS}$ Supply Current	Full	VI		TBD			TBD			TBD		mA
$V_{EE}$ Supply Current	Full	VI		TBD			TBD			TBD		mA
Power Dissipation	Full	VI	0.9	1.2		0.9	1.2		0.9	1.2		W
Power Supply Rejection Ratio (PSRR) <sup>5</sup>	+25°C	I	TBD	TBD		TBD	TBD		TBD	TBD		mV/V

**NOTES**

<sup>1</sup>Output delay measured as worst-case time from 50% point of the falling edge of ENCODE to 50% point of the slowest rising or falling edge of D0-D9.

Output skew measured as worst-case difference in output delay among D0-D9.

<sup>2</sup>RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

<sup>3</sup>Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

<sup>4</sup>For rated performance at 40 MSPS, duty cycle of encode command should be 50% ± 5%.

<sup>5</sup>Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in  $V_{CC}$  or  $V_{EE}$ .

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

+ $V_S$  ( $V_{DD}$  and  $V_{CC}$ ) ..... +7 V

- $V_S$  ( $V_{SS}$  and  $V_{EE}$ ) ..... -7 V

Analog In ..... - $V_S$  to + $V_S$

Digital Inputs ..... 0 V to + $V_S$

Digital Output Current ..... 20 mA

**Operating Temperature**

AD9040JN/JP/KN/KP ..... 0°C to +70°C

AD9040TE/TQ ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Maximum Junction Temperature<sup>2</sup> ..... +175°C

Lead Soldering Temp (10 sec) ..... +300°C

**NOTES**

<sup>1</sup>Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

<sup>2</sup>Typical thermal impedances: "N" Package (Plastic DIP):  $\theta_{JC} = 7^\circ\text{C/W}$ ;  $\theta_{JA} = 42^\circ\text{C/W}$ ; "P" Package (PLCC):  $\theta_{JC} = 10^\circ\text{C/W}$ ;  $\theta_{JA} = 48^\circ\text{C/W}$ ; "E" Package (Ceramic LCC):  $\theta_{JC} = 23^\circ\text{C/W}$ ;  $\theta_{JA} = 69^\circ\text{C/W}$ ; "Q" Package (Ceramic DIP):  $\theta_{JC} = 25^\circ\text{C/W}$ ;  $\theta_{JA} = 75^\circ\text{C/W}$ .

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