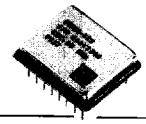
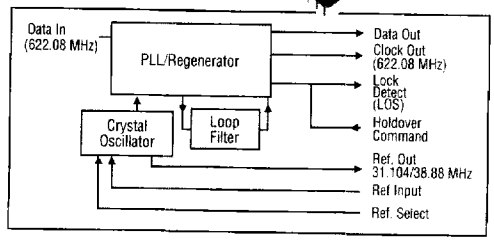
Sonet Clock Recovery Module SCRM-622



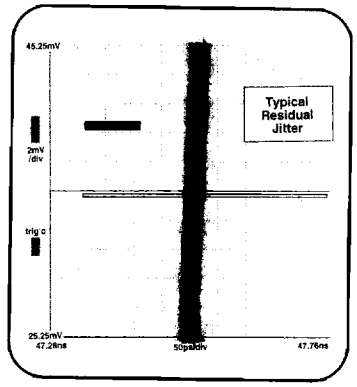
The Vectron SCRM-622 is a PLL based single package solution for clock and data recovery (CDR) at SONET OC-12/CCITT STM-4 rates. Unlike other high performance CDR modules, which require external components and crystal oscillators, the SCRM-622 is self-contained. No external loop filter or reference is required.

An onboard crystal oscillator produces a useable ±20 ppm TTL clock at 31.104 MHz (or optionally at 38.88 MHz) for holdover and system use. A LOCK indicator can be used as a Loss of Signal (LOS) detector. Jitter tolerance of the SCRM-622 is robust, meeting both CCITT STM-4A (table 2/G.958) and Bellcore TR-NWT-000253 requirements. All control lines are TTL compatible, while all high speed inputs and outputs are ECL level, making the SCRM-622 user friendly.



CHARACTERISTIC	CONDITION	SPECIFICATION
*Clock Rate		622.08 MHz
Tuning range		± 1 MHz
Acquisition Time	Input density = 50%	≤100 us
Jitter tolerance	10 Hz 30 Hz 300 Hz 25 kHz 250 kHz	≥ 15 UI ≥ 15 UI ≥ 1.5 UI ≥ 1.5 UI ≥ 0.4 UI
Residual Jitter (see plot)	2^{23}-1 PRB Sequence	≤ 7 ps rms
Output Accuracy of Internal Reference	0°C to +70°C and −40°C to +85°C	± 20 ppm and ±50 ppm

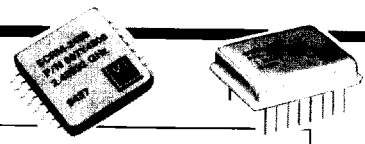
16 pin Double DIP
0.8 x 1.0 x 0.2"
(20.3 x 25.4 x 5.1mm)



*NOTE: In holdover mode (pin 9 forced low), the 622.08 MHz clock will track either the internal or external reference as determined by the user when controlling pin 2.

How to Order: 601Y3300 ☐ 4800 at 622.08 MHz ☐ = internal ref output frequency "A":31.104MHz, "B": 38.88 MHz

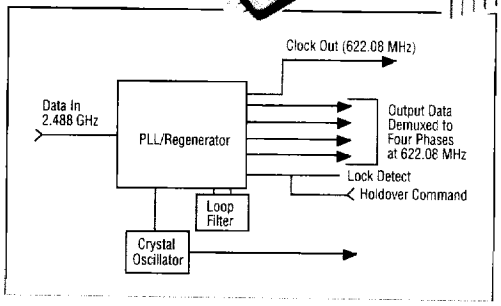
Sonet Clock Recovery Module SCRM-2488



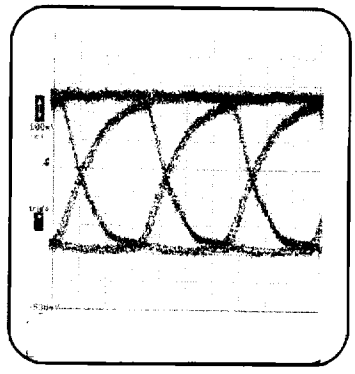
The Vectron SCRM-2488 is a PLL based single package solution for clock and data recovery (CDR) at SONET OC-48/CCITT STM-16 data rates. The SCRM-2488 is self contained, requiring no external components, simplifying design and manufacturing. An onboard 38.88 MHz crystal oscillator provides holdover and system clock capabilities.

The input to the SCRM-2488 is a complementary ECL STM-16/OC-48 NRZ datastream. The output clock is a 622.08 MHz differential clock that drives four parallel output datastreams. (REFER TO THE BLOCK DIAGRAM). The four output datastreams together represent one half byte of data (one nibble). The slower clock speed at the output greatly simplifies signal processing and board layout.

Jitter accommodation is robust. The SCRM-2488 meets both CCITT and Bellcore requirements for jitter transfer and accommodation.



CHARACTERISTIC	CONDITION	SPECIFICATION
Clock Rate		2.48832 GHz
Tuning range		±2 MHz
Acquisition Time	Input density = 50%	5 us typ
*Jitter tolerance	100 kHz 1 MHz	≥ 1.5 UI ≥ 0.15 UI
*Jitter Transfer (Peaking)	F <2 MHz	0.1 dB (max)
Residual Jitter		4 ps rms typ
†Output Accuracy of Internal Reference	0°C to +70°C and −40°C to −85°C	±20 ppm and ±50 ppm



* Meets Bellcore GR-253-CORE, Issue 1, 12/94 and ITU G.958 TYPE A
† **Note:** in Holdover Mode (PIN 3 - Forced Low) the 622.08 MHz output clock will track the internal crystal oscillator.

How to Order: 60 ☐ 4800 at 2.48832 GHz ☐ = "1" - 16 pin Double DIP; "7" - 16 pin Flatpack