September 1996
Revision 1.0

FUJITSU

DATA SHEET

EOB1UV641(1/4)-(60/70)TG-S

8MByte (1M x 64) CMOS EDO DRAM Module - 3.3V

General Description

The EOB1UV641(1/4)-(60/70)TG-S is a high performance, EDO (Extended Data Out) 8-megabyte dynamic RAM module organized as 1M words by 64 bits, in a 144-pins, small outline dual-in-line (SO DIMM) memory modules.

The module utilizes four, Fujitsu MB81V1(8/6)165A-(60/70) (FN) CMOS 1Mx16 EDO dynamic RAMs in a surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines provided are such that byte control is possible. Serial PD on the module is provided by using 128 byte serial EEPROM.

Features

- High Density: 8MByte
- Fast Access Time of 60/70 ns (max.)
- Low Power: 2.6/2.4 W (max.) - Active (60/70 ns) - 1KR
  1.3/1.1 W (max.) - Active (60/70 ns) - 4KR
  29mW (max.) - Standby (LVTTL)
  14mW (max.) - Standby (CMOS)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.00 inch

ABSOLUTE MAXIMUM RATINGS

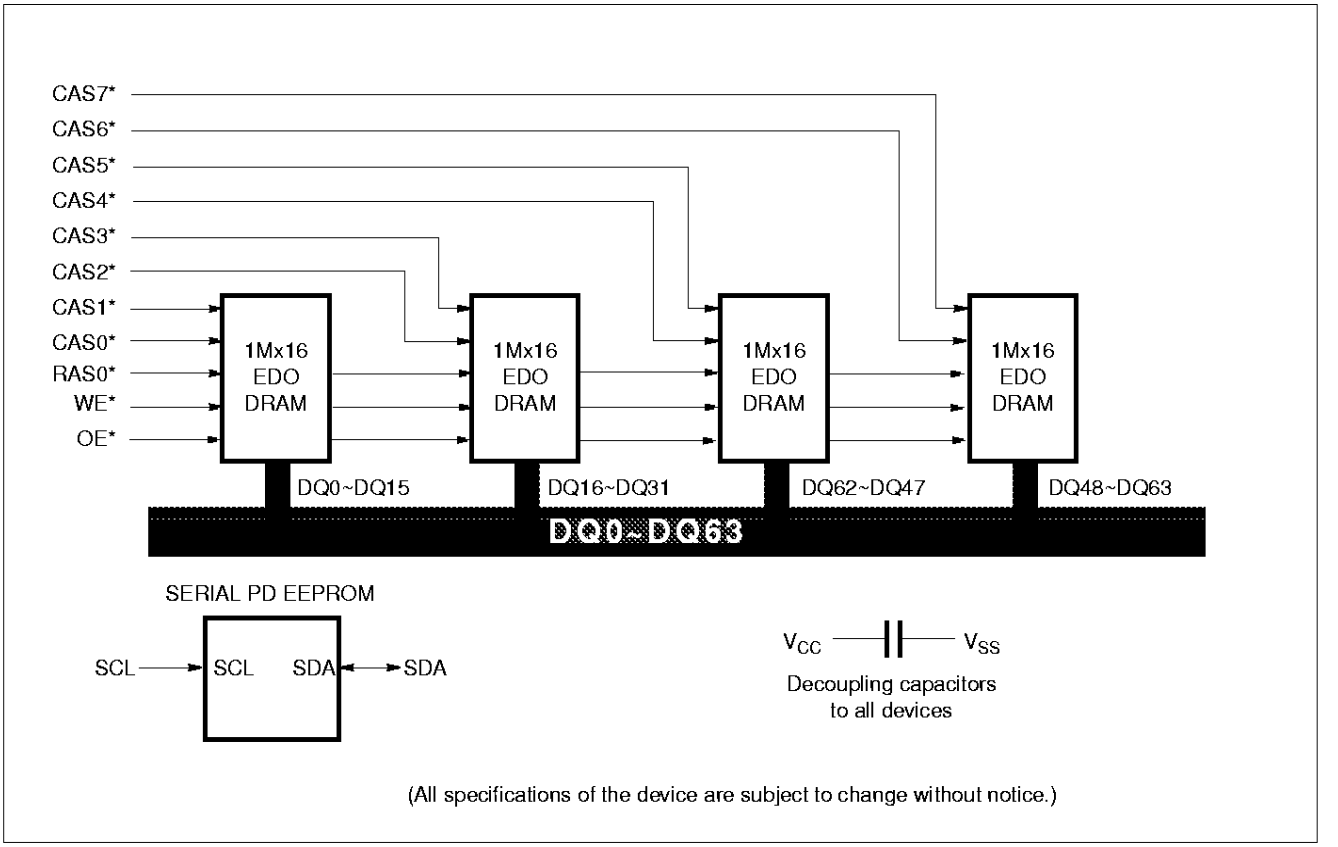
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	4	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low voltage	-0.3	-	0.8	V

Functional Diagram



(All specifications of the device are subject to change without notice.)

Notes: 1. signifies active low signal.
2. Addresses A0 ~ A11 are connected to all DRAMs. (A10 & A11 are NC for the 1K refresh module.)
3. A0~A2 of the Serial PD EEPROM device are grounded.

Pin Name

A0~A9	Row and Column Addresses for 1K Refresh	OE*	Output Enable Input
A0~A11	Row Addresses for 4K Refresh	SCL	Serial PD Clock
A0~A7	Column Addresses for 4K Refresh	SDA	Serial PD Data Input/Output
DQ0~DQ63	Data Inputs/Outputs	V_{CC}	Power Supply
RAS0*	Row Address Strobes	V_{SS}	Ground
CAS0*~CAS7*	Column Address Strobes	NC	No Connection
WE*	Write Enable Input		

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	2	V_{SS}	73	OE*	74	NC
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{CC}	82	V_{CC}
11	V_{CC}	12	V_{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	CAS0*	24	CAS4*	95	DQ21	96	DQ53
25	CAS1*	26	CAS5*	97	DQ22	98	DQ54
27	V_{CC}	28	V_{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{CC}	102	V_{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	A11 (Note)
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	A10 (Note)	112	NC
41	DQ10	42	DQ42	113	V_{CC}	114	V_{SS}
43	DQ11	44	DQ43	115	CAS2*	116	CAS6*
45	V_{CC}	46	V_{CC}	117	CAS3*	118	CAS7*
47	DQ12	48	DQ44	119	V_{SS}	120	V_{CC}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ28	132	DQ60
61	NC	62	NC	133	DQ29	134	DQ61
63	V_{CC}	64	V_{CC}	135	DQ30	136	DQ62
65	NC	66	NC	137	DQ31	138	DQ63
67	WE*	68	NC	139	V_{SS}	140	V_{SS}
69	RAS0*	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	V_{CC}	144	V_{CC}

Note: Address A10 and A11 are NC for the 1K refresh module but are used for the 4K refresh module.

DC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Condition		60		70		Unit	Note
				Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	RAS*, CAS* cycling; t_{RC} = min.	1KR	-	720	-	680	mA	1, 2
			4KR	-	360	-	320		
Standby current	I_{CC2}	LVTTL Interface RAS*, CAS* ≥ V_{IH} D_{out} = High-Z		-	8	-	8	mA	
		CMOS Interface RAS*, CAS* ≥ V_{cc} - 0.2V D_{out} = High-Z		-	4	-	4	mA	
RAS* -only Refresh Current	I_{CC3}	CAS* ≥ V_{IH}; RAS*, Address cycling @ t_{RC} = min.	1KR	-	720	-	680	mA	2
			4KR	-	360	-	320		
CAS*-before-RAS* Refresh Current	I_{CC4}	RAS*, CAS* cycling @ t_{RC} = min.	1KR	-	680	-	640	mA	
			4KR	-	360	-	320		
Hyper Page Mode Current	I_{CC5}	RAS* ≤ V_{IL}; CAS*, Address cycling @ t_{PC} = min.	1KR	-	480	-	440	mA	1, 3
			4KR	-	440	-	400		
Input Leakage Current	I_{LI}	0V ≤ V_{in} ≤ V_{CC} + 0.3V		-40	40	-40	40	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable		-10	10	-10	10	µA	
Output High Voltage	V_{OH}	High I_{out} = -2mA		2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 2 mA		0	0.4	0	0.4	V	

Notes: 1. Values depend on output load condition when the device is selected. Maximum Values are specified at the output open condition.
2. Address can be changed once or less while RAS* = V_{IL}.
3. Address can be changed once or less while CAS* = V_{IH}.

CAPACITANCE

(TA =+25°C, V_{CC} = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	25	pF	1
Input Capacitance (RAS*, OE*, WE*)	C_{I2}	33	pF	1
Input Capacitance (CAS0*~CAS7*)	C_{I3}	12	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS

(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

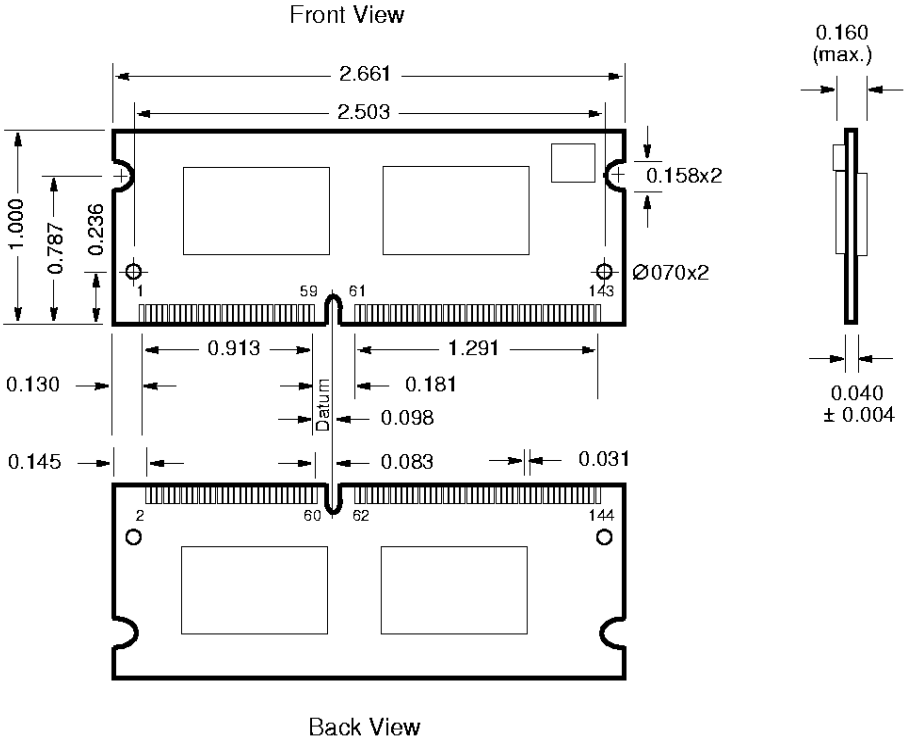
Parameter		Symbol	60		70		Unit	Notes
			Min	Max	Min	Max		
Random read/write cycle time		t_{RC}	110	-	130	-	ns	
Access time from RAS*		t_{RAC}	-	60	-	70	ns	3, 4
Access time from CAS*		t_{CAC}	-	15	-	20	ns	3, 4, 5
Access time from column address		t_{AA}	-	30	-	35	ns	3, 10
Transition time (rise and fall)		t_T	2	50	2	50	ns	2
RAS* precharge time		t_{RP}	40	-	50	-	ns	
RAS* pulse width		t_{RAS}	60	10000	70	10000	ns	
RAS* hold time		t_{RSH}	15	-	20	-	ns	
CAS* hold time		t_{CSH}	45	-	50	-	ns	
CAS* pulse width		t_{CAS}	10	10000	15	10000	ns	
RAS* to CAS* delay time		t_{RCD}	20	45	20	50	ns	4
RAS* to column address delay time		t_{RAD}	15	30	15	35	ns	10
CAS* to RAS* precharge time		t_{CRP}	5	-	5	-	ns	
Row address set-up time		t_{ASR}	0	-	0	-	ns	
Row address hold time		t_{RAH}	10	-	10	-	ns	
Column address set-up time		t_{ASC}	0	-	0	-	ns	
Column address hold time		t_{CAH}	10	-	15	-	ns	
Column address to RAS* lead time		t_{RAL}	30	-	35	-	ns	
Read command set-up time		t_{RCS}	0	-	0	-	ns	
Read command hold time to CAS*		t_{RCH}	0	-	0	-	ns	8
Read command hold time to RAS*		t_{RRH}	0	-	0	-	ns	
Write command hold time		t_{WCH}	10	-	15	-	ns	
Write command pulse width		t_{WP}	10	-	15	-	ns	
Write command to RAS* lead time		t_{RWL}	15	-	17	-	ns	
Write command to CAS* lead time		t_{CWL}	10	-	15	-	ns	
Data-in set-up time		t_{DS}	0	-	0	-	ns	9
Data-in hold time		t_{DH}	10	-	15	-	ns	9
Refresh period	1KR	t_{REF}	-	16	-	16	ms	
	4KR		-	64	-	64		
Write command set-up time		t_{WCS}	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)		t_{CSR}	10	-	10	-	ns	1
CAS* hold time (CBR refresh)		t_{CHR}	10	-	15	-	ns	1
RAS* precharge to CAS* hold time		t_{RPC}	5	-	5	-	ns	
Access time from CAS* precharge		t_{CPA}	-	35	-	40	ns	3, 11
Hyper page mode cycle time		t_{HPC}	25	-	30	-	ns	
CAS* precharge time (Hyper page)		t_{CP}	10	-	10	-	ns	
RAS* pulse width (Hyper page)		t_{RASP}	60	100000	70	100000	ns	12

Notes:

1. An initial pulse of at least 200µs is required after power-up followed by a minimum of eight RAS* cycles before device operation is achieved.
2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumed to be 5 ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) limit can be met; t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RAD}$ (max.).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS* leading edge in early write cycles.
10. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) limit can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{ACP}.
12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

144-pin 3.4V SODIMM



(All dimensions are in inches with 0.005" tolerance unless otherwise specified)

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