# PLESSEY Semiconductors

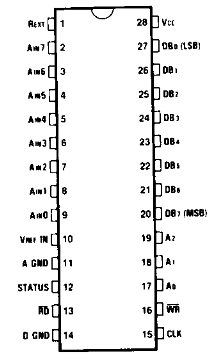
# ZN437

## MICROPROCESSOR-COMPATIBLE 8-BIT, 8 CHANNEL DATA ACQUISITION SYSTEM

The ZN437 is an 8-bit, 8 channel data acquisition system designed to easily interface to most popular microprocessors. It consists of an 8-bit successive approximation A-D converter, an 8 channel multiplexer, 8 x 8 bit RAM, clock pre-divider, control logic and double buffered latches with 3-state outputs.

The ZN437 can be programmed for any one of four possible conversion modes: 'single shot' conversion on a named channel; 'continuous conversion' on a named channel; a 'single shot' conversion on all channels; and continuous conversion on all channels.

Using the successive approximation technique, the result of each channel conversion is loaded into the correct location of the 8 x 8 bit RAM. The address bus ($A_2$→$A_0$) is used to select the channel data to be read with the double buffered output latches allowing data to be read at any time irrespective of the conversion status.




**ZN437E (DP28)**
**ZN437J (DC28)**

**Pin connections - top view**

### FEATURES

- Choice of Linearity: ±0.5, ±1 LSB
- 16 microseconds Conversion Time
- 8 Analogue Inputs
- On-Chip 8 x 8 RAM
- Four Possible Conversion Modes
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Microprocessor, TTL and CMOS Compatible
- Accepts Microprocessor Clocks up to 4MHz
- ROM Type Operation
- Commercial or Military Temperature Ranges

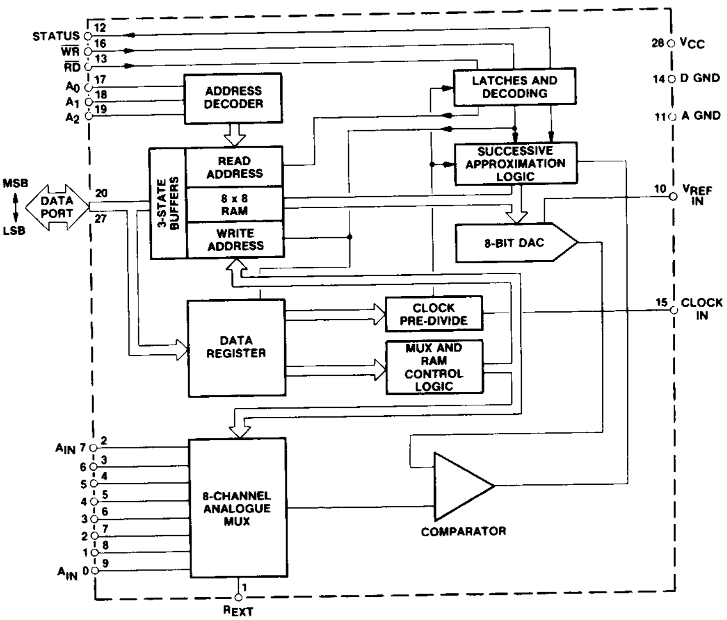



**Fig.1 System diagram**

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7V |
| Maximum voltage, logic and $V_{REF}$ inputs | $V_{CC}$ |
| Operating temperature range | 0 °C to +70 °C (ZN437E) |
| | -55 °C to +125 °C (ZN437J) |
| Storage temperature range | -55 °C to +125 °C |

**ELECTRICAL CHARACTERISTICS** (at $V_{CC}$ = 5V, $T_{amb}$ = 25°C and $f_{CLK}$ = 500KHz unless otherwise stated).

| Parameter | $T_{amb}$ = + 25°C | | | Over specified Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **ZN437-8** | | | | | | | |
| Linearity error | – | – | ±0.5 | – | ±0.5 | LSB | |
| Differential linearity error | – | – | ±0.75 | – | ±0.75 | LSB | |
| **ZN437-7** | | | | | | | |
| Linearity error | – | – | ±1 | – | ±1 | LSB | |
| Differential linearity error | – | – | ±1 | – | ±1 | LSB | |
| **ALL TYPES** | | | | | | | |
| Zero transition | – | 10 | – | – | – | mV | ZN437E } Ext. Ref. = 2.56V |
| (00000000→00000001) | – | 10 | – | – | – | mV | ZN437J |
| Full-scale transition | – | 2.550 | – | – | – | V | ZN437E |
| (11111110→11111111) | – | 2.550 | – | – | – | V | ZN437J |
| Linearity temperature coefficient | | ±3 typ. | | | | ppm/°C | } Ext. Ref. = 2.50V |
| Differential linearity temperature coefficient | | ±6 typ. | | | | ppm/°C | |
| Gain temperature coefficient | | ±10 typ. | | | | ppm/°C | |
| Offset temperature coefficient | | ±7 typ. | | | | ppm/°C | |
| Resolution | 8 | – | – | – | – | Bits | |
| Conversion time | 16 | – | – | – | – | μs | per channel |
| Supply rejection | – | 0.2 | – | – | – | %/V | |
| Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.5 | V | |
| Supply current | – | 45 | – | – | – | mA | } Outputs in high impedance state |
| Power consumption | – | 225 | – | – | – | mW | |
| Reference input range | 1.5 | – | 3.0 | – | – | V | |
| Ladder output impedance | – | 2.7 | – | – | – | KΩ | |
| **MULTIPLEXED INPUTS** | | | | | | | |
| Input current | – | 10 | – | – | – | nA | $V_{in}$ = +3V, $R_{ext}$ = 1.8KΩ |
| Input resistance | – | 10 | – | – | – | MΩ | |
| Tail current | – | 1.1 | – | – | – | mA | $R_{ext}$ = 1.8KΩ, $V_{EE}$ = −5V |
| Negative supply | −3 | −5 | −30 | −3 | −30 | V | |
| Input voltage, $V_{in}$ | −0.5 | – | +3.5 | −0.5 | +3.5 | V | |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | $T_{amb} = +25°C$ | | | Over specified temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **EXTERNAL VOLTAGE REFERENCE** | | | | | | | |
| Output voltage | 1.5 | – | 3.0 | – | – | V | |
| Slope impedance | – | 0.75 | – | – | – | Ω | |
| ZN437 current drain from $V_{REF\ IN}$ | – | – | 1.0 | – | – | mA | Note 1 |
| Output voltage temperature coefficient | – | 50 | – | – | – | ppm/°C | |
| **EXTERNAL CLOCK** | | | | | | | |
| Clock frequency | – | – | 4.0 | – | 4.0 | MHz | Pre-divide set to ÷8 |
| High level I/P voltage $V_{IH}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 200 | – | – | – | μA | $V_{CC} = 5.5V$ $V_{IN} = 4V$ |
| Low level I/P current $I_{IL}$ | – | –160 | – | – | – | μA | $V_{CC} = 5.5V$ $V_{IN} = 0.8V$ |
| **LOGIC $\overline{WR}$, $\overline{RD}$, $A_2$, $A_1$, $A_0$ INPUTS** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 220 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +5.5V$ |
| High level I/P current $I_{IH}$ | – | 35 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +2.4V$ |
| Low level I/P current $I_{IL}$ | – | –200 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +0.4V$ |
| **DATA INPUTS/OUTPUTS** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 40 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +5.5V$ |
| High level I/P current $I_{IH}$ | – | 10 | – | – | – | μA | $V_{CC} = +5\ 5V$ $V_{IN} = +2.4V$ |
| Low level I/P current $I_{IL}$ | – | –100 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +0.4V$ |
| High level output voltage $V_{OH}$ | 2.4 | – | – | 2.4 | – | V | $I_{OH\ MAX}$ |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | – | 0.4 | V | $I_{OL\ MAX}$ |
| High level output current $I_{OH}$ | – | – | –800 | – | – | μA | |
| Low level output current $I_{OL}$ | – | – | 2.0 | – | – | mA | |

Note 1: When bipolar operation is employed, the external component connections will present an additional load to the reference. See section on bipolar operation.

## ELECTRICAL CHARACTERISTICS (Cont.)

| Parameter | $T_{amb}$ = +25°C | | | Over specified temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| Enable/disable delay times | | | | | | | |
| TE1 | 90 | – | 220 | – | – | ns | see fig.9 |
| TE0 | 60 | – | 120 | – | – | ns | see fig.9 |
| TD1 | 80 | – | 160 | – | – | ns | see fig.9 |
| TD0 | 60 | – | 110 | – | – | ns | see fig.9 |
| Write pulse width | 135 | – | – | – | – | ns | |
| $\overline{WR}$ I/P to STATUS O/P high | – | 280 | 360 | – | – | ns | |
| Read pulse width | 220 | – | – | – | – | ns | |
| $\overline{RD}$ high to STATUS high | – | 240 | 400 | – | – | ns | |
| Data set up prior to $\overline{WR}$ going low | –55 | – | – | – | – | ns | |
| Data hold after $\overline{WR}$ going high | 10 | – | – | – | – | ns | |
| Address inputs stable prior to $\overline{RD}$ going low | 10 | – | – | – | – | ns | |
| Address inputs stable after $\overline{RD}$ going high | 10 | – | – | – | – | ns | |

## GENERAL CIRCUIT DESCRIPTION

The ZN437 accepts eight analogue inputs and by using an eight bit 'Control Word', can be programmed to convert in any one of four different operational modes: 'Single shot' conversion on a named channel; 'continuous conversion' on a named channel; a 'single shot' conversion on all channels; and continuous conversion on all channels. Each channel can be converted into an eight bit binary word using the successive approximation technique with the result of the conversion being loaded into the correct location of the 8×8 bit RAM. The 'Control Word' is loaded into the device on the negative edge of the $\overline{WR}$ input pulse. The conversion mode, input channel (modes 1 and 2 only) and clock pre-divide are selected. The STATUS output goes high to indicate the beginning of the conversion and the DAC input is set to the MSB. The multiplexer selects one input channel at a time (dependent on the Control Word) on which a conversion is to be performed. The output of the DAC is compared to the unknown analogue signal be means of the comparator. If the analogue input is larger, the MSB is left in the circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge the STATUS goes low indicating that the conversion is complete and the RAM is updated.

Data can be read from the ZN437 by placing the correct channel address on pins $A_0$, $A_1$, $A_2$ and by taking $\overline{RD}$ low. The negative edge of the $\overline{RD}$ pulse powers up the required channel's RAM location and enables the 3-state outputs. The RAM is kept in a low power standby mode when not being accessed. Double buffered latches on-chip allow the outputs to be enabled at any time, irrespective of the conversion status and valid data will always be presented to the data bus, this data will be the result of the most recent conversion on that channel, therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the STATUS. The data port (bi-directional input/output port) dictates that $\overline{WR}$ and $\overline{RD}$ must never be active at the same time as this will lead to conflict on the bus.

## CONTROL LOGIC

For the ZN437 to function correctly when powered up, an 'Initialisation' word must be sent to the device with START, $\overline{SQ}$ and $\overline{CY}$ set high. This will set up the device for immediate operation.

| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| Control Word | $\overline{START}$ | CLOCK PRE-DIVIDER | | $\overline{CY}$ | $\overline{SQ}$ | ANALOGUE INPUT | | |
| 'Initialisation' word | 1 | X | X | 1 | 1 | X | X | X |

X = do not care

The device is now set up for initiating the first conversion.

All operations of the ZN437 are controlled by the 'Control Word'. (See above).

ANALOGUE INPUT: 3-bit code for Analogue Input selection. Used only when doing a conversion on a named input.

SEQUENCE $\overline{SQ}$: Active low, indicates a sequencing action through all eight channels.

CYCLING $\overline{CY}$: Active low, indicates a continuous conversion of one or all channels

CLOCK PRE-DIVIDER: Two bit code enables ÷ 1, ÷ 2, ÷ 4 and ÷ 8 of the clock frequency.

$\overline{START}$: Initiates a conversion by a high to low transition.

The $\overline{WR}$ signal is used by the device to latch in the Control Word currently sat on the data bus, data being latched on the rising edge of the $\overline{WR}$ signal.

Note that a $\overline{WR}$ signal is always required to change or input a new Control Word.

| DB6 | DB5 | DIVISION RATIO |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 2 |
| 0 | 1 | 4 |
| 0 | 0 | 8 |

**CLOCK PRE-DIVIDE SELECTION**

## CONVERSION TIMING

The ZN437 will accept a low going $\overline{WR}$ pulse, which will load in the 'Control Word' and start the conversion sequence. The $\overline{WR}$ pulse can be completely asynchronous with respect to the clock and will produce valid data between 8 and 9 clock cycles later depending on the relative timing of the clock and convert signals. Timing diagrams for a conversion are shown in Fig. 2.

The $\overline{WR}$ pulse can be as short as 150ns, there is no maximum limit, but the control word should not be changed and $\overline{RD}$ should not be taken low whilst $\overline{WR}$ is low. The MSB must be allowed to settle for at least 2.0μs before the MSB decision is made. To ensure that this criterion is met even with short write pulses the converter waits for a falling clock edge before commencing with the conversion. This ensures that the MSB is allowed to settle for at least a full clock period or 2.0μs at maximum 500KHz clock frequency.

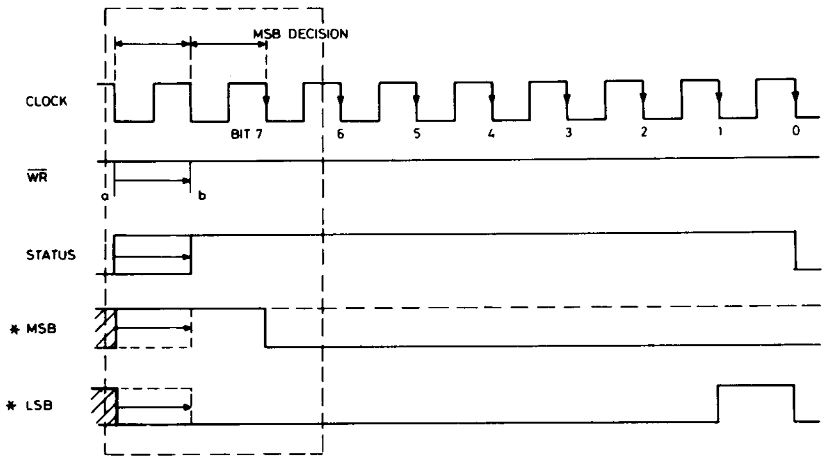



Fig. 2a

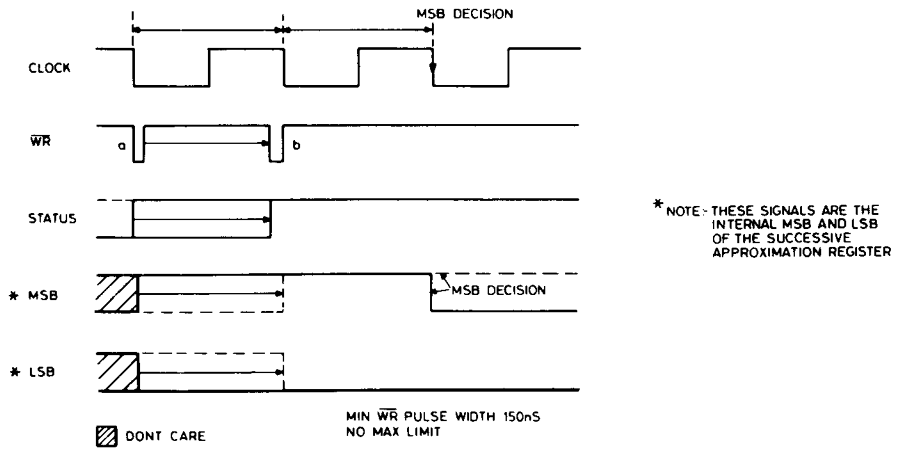



Fig. 2b

**Fig. 2 Timing diagram**

## CONVERSION MODES

The ZN437 has four possible conversion modes:

1. A single conversion on a specified analogue input.
2. A continuous conversion on a specified analogue input.
3. A single conversion of all eight channels.
4. A continuous conversion of all eight channels.

Any of the four modes can be selected by the $\overline{SQ}$ and $\overline{CY}$ bits in the control word.

**1. A single conversion on a specified analogue input.**

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 0 | CLOCK PRE-DIVIDER | | 1 | 1 | ANALOGUE INPUT | | |
| $\overline{START}$ | SELECT DIVISION RATIO | | $\overline{CY}$ | $\overline{SQ}$ | SELECT CHANNEL | | |

Control Word for Mode 1

One conversion is initiated on the specified channel by $\overline{START}$ (DB7) going low. STATUS output is forced high and the internal clock started. At the end of the conversion the STATUS output returns low, on-chip logic detects that $\overline{SQ}$ and $\overline{CY}$ are high and stops the internal clock. Note at this point the Control Word is automatically reset to all 1's (because a 1→0 transistion is required on DB7 to start the device). Hence the device is all set up waiting for a new Control Word.

A timing diagram for this mode is shown in Fig. 3.

**2. A continuous conversion on a specified analogue input.**

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 0 | CLOCK PRE-DIVIDER | | 0 | 1 | ANALOGUE INPUT | | |
| $\overline{START}$ | SELECT DIVISION RATIO | | $\overline{CY}$ | $\overline{SQ}$ | SELECT CHANNEL | | |

Control Word for Mode 2

A continuous conversion is initiated on the specified channel by $\overline{START}$ (DB7) going low. The STATUS output is forced high and the internal clock started. At the end of each conversion, internal logic checks to see if $\overline{CY}$ is still 0, if it is, it will continue with the next conversion. To stop the conversion process, a new Control Word must be written to the device which has $\overline{SQ}$ and $\overline{CY}$ both high. This can occur at any time in the conversion cycle with the device completing the current conversion before stopping.

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 1 | CLOCK PRE-DIVIDER | | 1 | 1 | ANALOGUE INPUT | | |
| $\overline{START}$ | NO CHANGE | | $\overline{CY}$ | $\overline{SQ}$ | NO CHANGE | | |

Stop Control Word for Mode 2

At the end of the conversion the control word is again automatically reset to all 1's.

A timing diagram for this mode is shown in Fig. 4.

**3. A single conversion of all eight channels.**

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 0 | CLOCK PRE-DIVIDER | | 1 | 0 | ANALOGUE INPUT | | |
| $\overline{\text{START}}$ | SELECT DIVISION RATIO | | $\overline{\text{CY}}$ | $\overline{\text{SQ}}$ | NOT USED IN THIS MODE | | |

Control Word for Mode 3

Conversions are initiated by $\overline{\text{START}}$ (DB7) going low. The STATUS output is forced high and the internal clock started. $\overline{\text{SQ}}$ being low causes the device to sequence through all eight channels starting at channel 0 going through to channel 7. After the conversion on channel 7 the device automatically stops, resetting the Control Word to all 1's ready for the next Control Word.

A timing diagram for this mode is shown in Fig. 5.

**4. Continuous conversion of all eight channels.**

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 0 | CLOCK PRE-DIVIDER | | 0 | 0 | ANALOGUE INPUT | | |
| $\overline{\text{START}}$ | SELECT DIVISION RATIO | | $\overline{\text{CY}}$ | $\overline{\text{SQ}}$ | NOT USED IN THIS MODE | | |

Start Control Word for Mode 4

Conversions are initiated by $\overline{\text{START}}$ (DB7) going low. The STATUS output is forced high. In this mode we sequence through each channel starting at channel 0. After the conversion on channel 7 the device goes back to channel 0 and starts again.

There are two ways to stop the conversion mode:

**A.** A new Control Word is written to the device with $\overline{\text{SQ}}$, $\overline{\text{START}}$ and $\overline{\text{CY}}$ high. This will force the device to stop converting at the end of the current channel conversion.

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 1 | CLOCK PRE-DIVIDER | | 1 | 1 | ANALOGUE INPUT | | |
| $\overline{\text{START}}$ | NO CHANGE | | $\overline{\text{CY}}$ | $\overline{\text{SQ}}$ | NOT USED IN THIS MODE | | |

Stop Control Word A for Mode 4

B. A new Control Word is written to the device with $\overline{SQ}=0$, $\overline{START}=1$, and $\overline{CY}=1$. In this case the device will contine until it has completed channel 7 then it will stop automatically (similar operation to mode 3) resetting the Control Word to all 1's ready for the next Control Word.

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | CLOCK PRE-DIVIDER | | 1 | 0 | ANALOGUE INPUT | | | Stop Control Word B for Mode 4 |
| $\overline{START}$ | NO CHANGE | | $\overline{CY}$ | $\overline{SQ}$ | NOT USED IN THIS MODE | | | |

A timing diagram for this mode is shown in Fig. 6.

**READ CHANNEL SELECTION**

The following table shows the truth table for the address inputs ($A_2$, $A_1$, $A_0$). The input address is used when $\overline{RD}$ goes low. When $\overline{RD}$ is high the input address is locked out.

| $A_2$ | $A_1$ | $A_0$ | CHANNEL TO BE READ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

**ANALOGUE INPUT CHANNEL SELECTION**

The following table shows how to select an Analogue Input channel using DB2,DB1 & DB0.

| DB2 | DB1 | DB0 | CHANNEL SELECTED |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 2 |
| 1 | 1 | 0 | 3 |
| 0 | 0 | 1 | 4 |
| 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 6 |
| 1 | 1 | 1 | 7 |

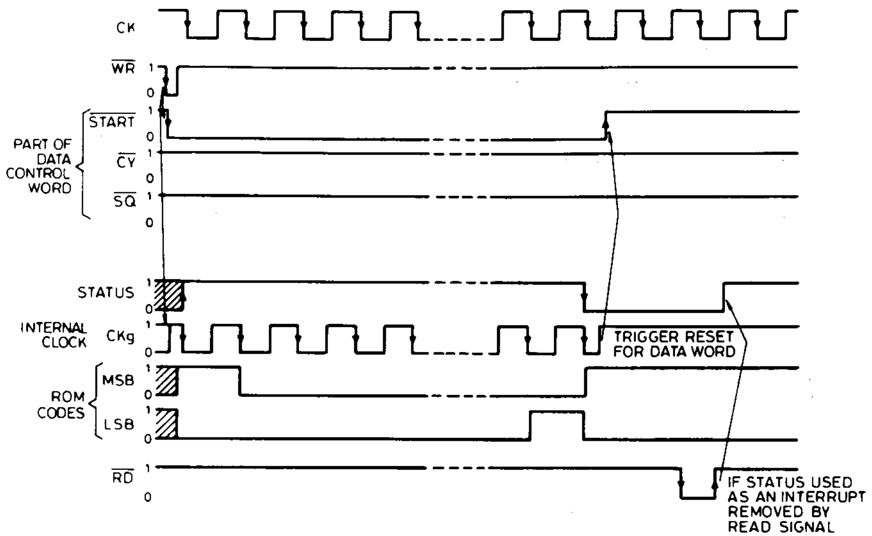



**Fig. 3 Single conversion on a named channel**

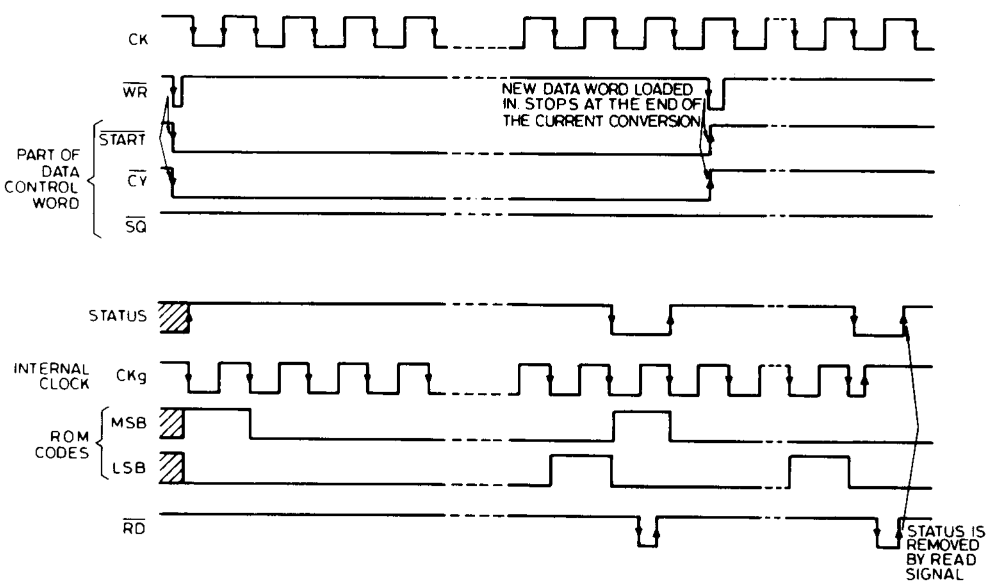



**Fig. 4 Continuous conversion on a named channel**

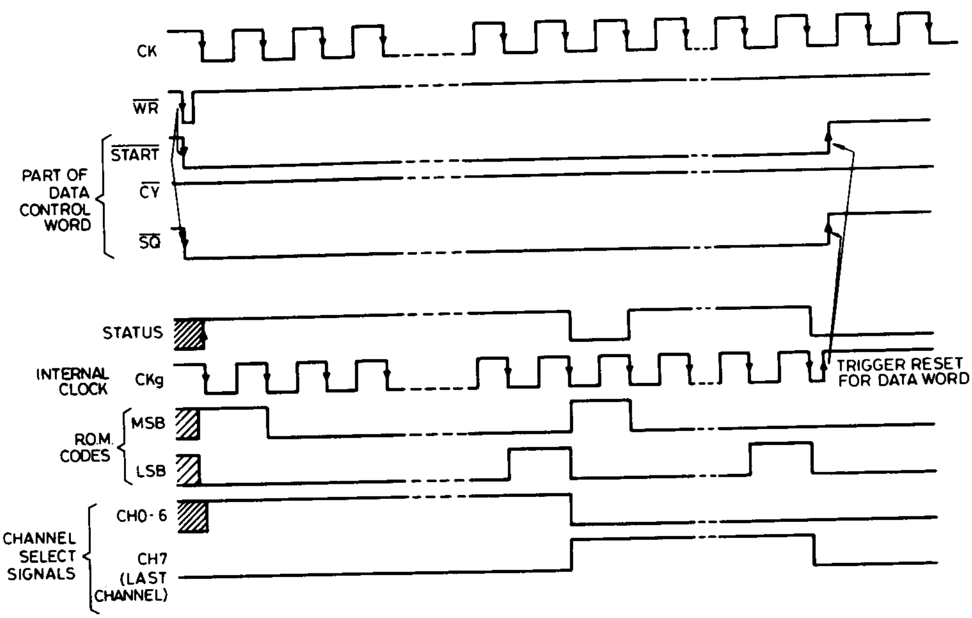



**Fig.5 A single conversion of all channels**

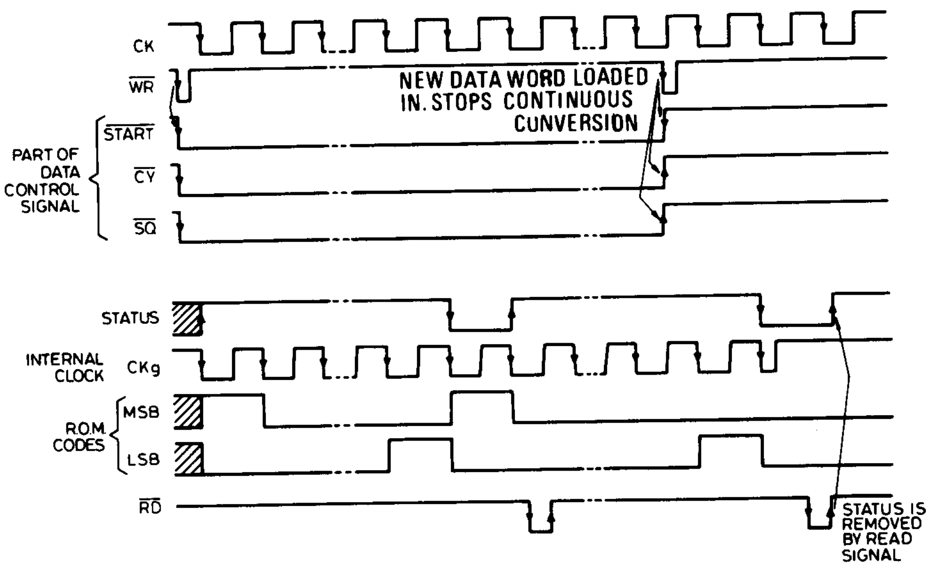



**Fig. 6 Continuous conversion of all channels**

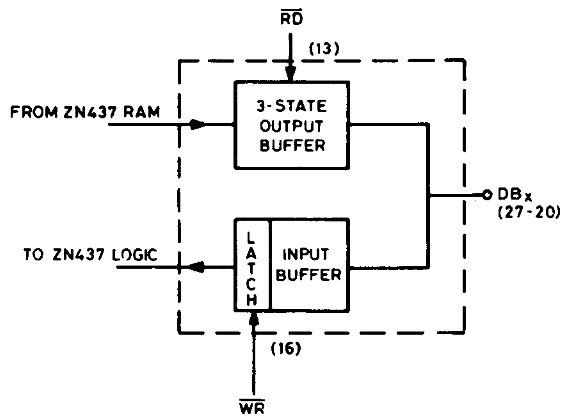



Fig. 7 ZN437 data port

## DATA PORT

The ZN437 has eight data ports. These are bi-directional input/output ports, see Fig. 7.

The data outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 8.

Whilst the $\overline{RD}$ input is high both output transistors are off.

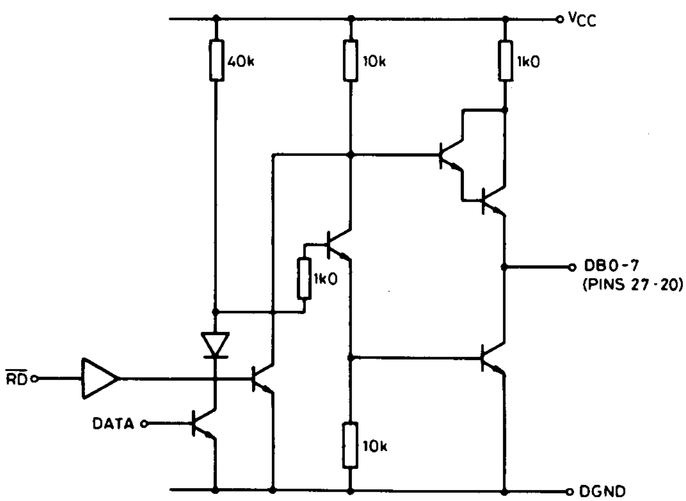
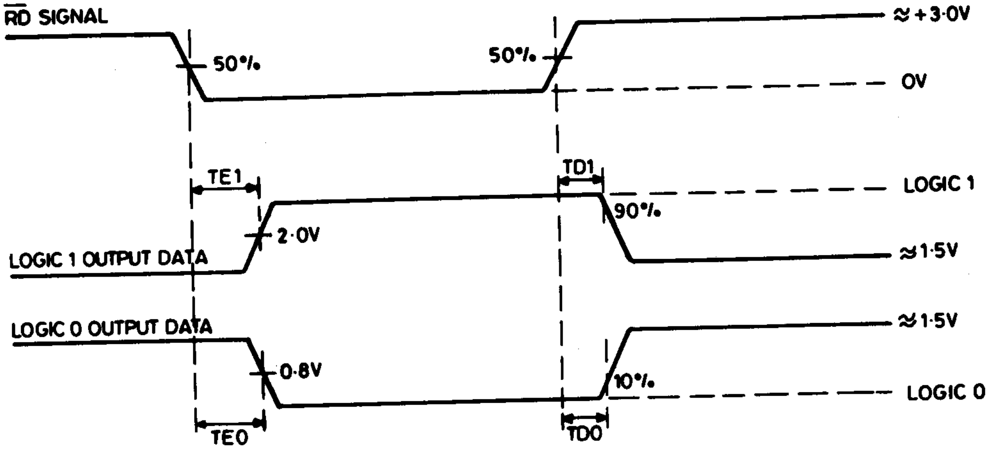



Fig. 8 Data outputs




TE = RD ENABLE DELAY TIME (CL = 50pF)
TD = RD DISABLE DELAY TIME (CL = 10pF)

**Fig. 9a Output enable/disable delays**

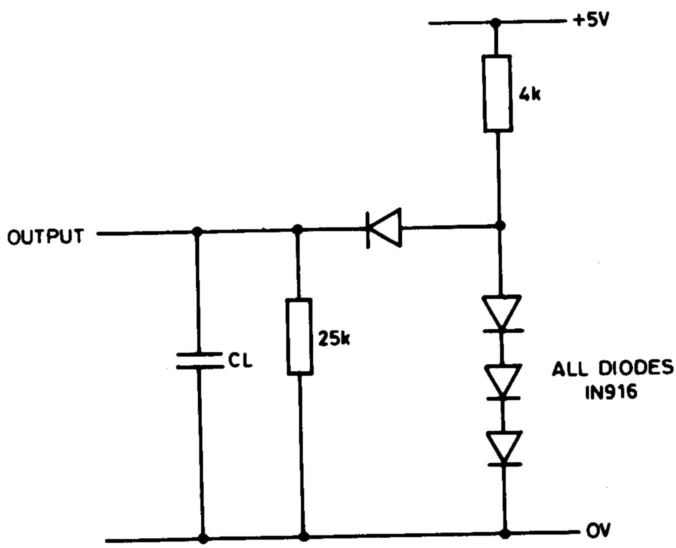



**Fig. 9b Output load circuit**

## CLOCK INPUT

The ZN437 clock input must be driven externally with TTL/CMOS compatible signals. The device will accept microprocessor clocks up to 4MHz, here the clock pre-divider will need setting to ÷8.

## ANALOGUE CIRCUITS

### Reference

The ZN437 requires an external reference in the range +1.5 to +3.0V which is connected between $V_{REF\ IN}$ (pin 10) and analogue GND (pin 11). The slope resistance of such a reference source should be less than 2.5Ω or 2.5Ω/n where n is the number of converters supplied.

Suggested reference sources are the REF25Z for commercial applications and the ZNREF025A1 for military temperature range operation.

### Ratiometric operation

If the output from a transducer varies with its supply then an external reference for the ZN437 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN437 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

## D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 10. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be 0 to $V_{REFIN}$ − 1LSB through an output resistance R(2K7).

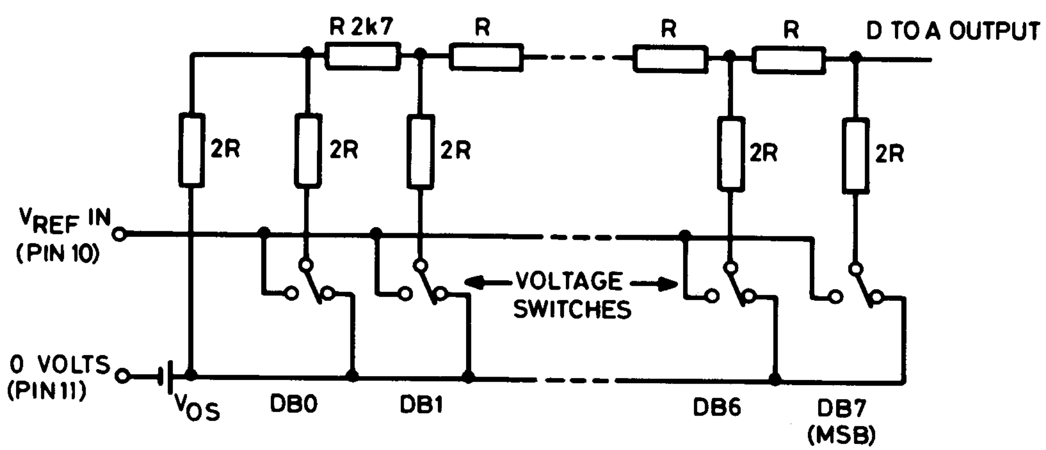



Fig. 10 R-2R Ladder Network

## MULTIPLEXED INPUTS AND COMPARATOR

The ZN437 contains eight analogue inputs which are fed into a multiplexer. The required channel is then selected and fed into the comparator. The multiplexer is digitally controlled by the information contained in the 'Control Word' (bits DB0 – DB4). This allows the multiplexer to behave in any one of the four system operating modes as previously described.

The ZN437 contains a fast comparator. The equivalent input circuit for one channel is shown in Fig. 11. A negative supply voltage is required to supply the tail current of the input stages which is a nominal 1.1mA with $V_{EE} = -5V$ and $R_{EXT} = 1.8K\Omega$.

A list of suitable resistors for different supply voltages is given in the adjacent table.

| $V_{EE}$ (volts) | $R_{EXT}$ (KΩ) |
|---|---|
| −3 | — |
| −5 | 1.8 |
| −10 | 6.2 |
| −12 | 7.5 |
| −15 | 11 |
| −20 | 15 |
| −25 | 20 |
| −30 | 24 |

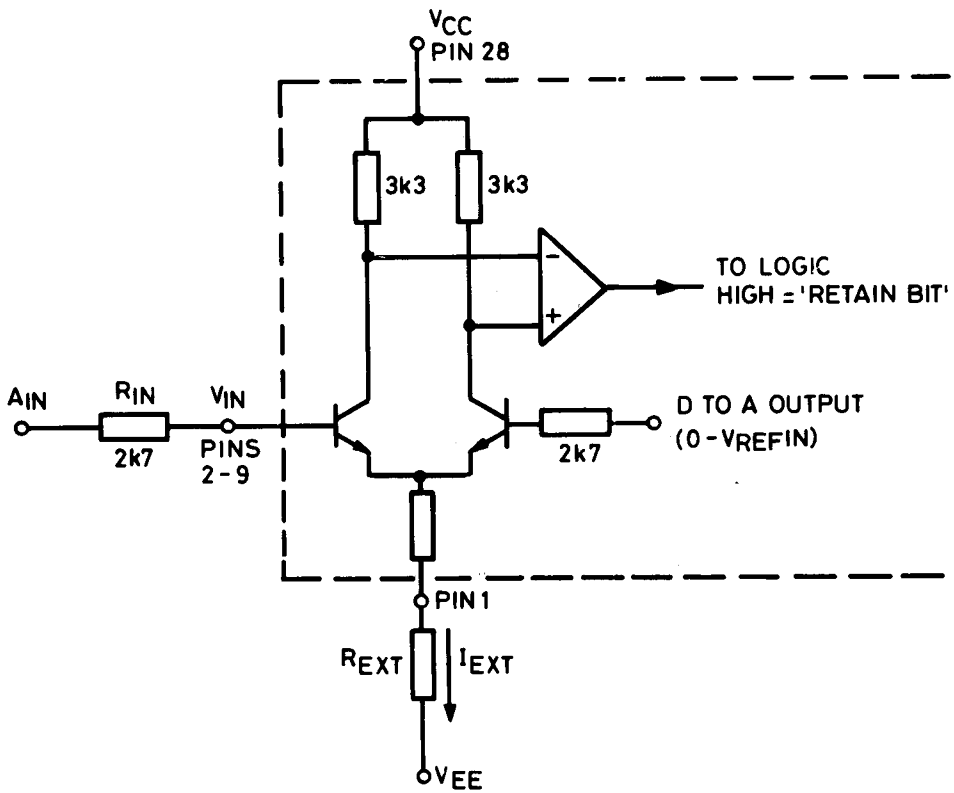



Fig. 11 Analogue input equivalent circuit for a channel

## ANALOGUE INPUT RANGES

The basic connection of the ZN437, shown in Fig. 12, has an analogue input range 0 to $V_{REF}$ which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input ranges so that the input stage always sees a positive input voltage.

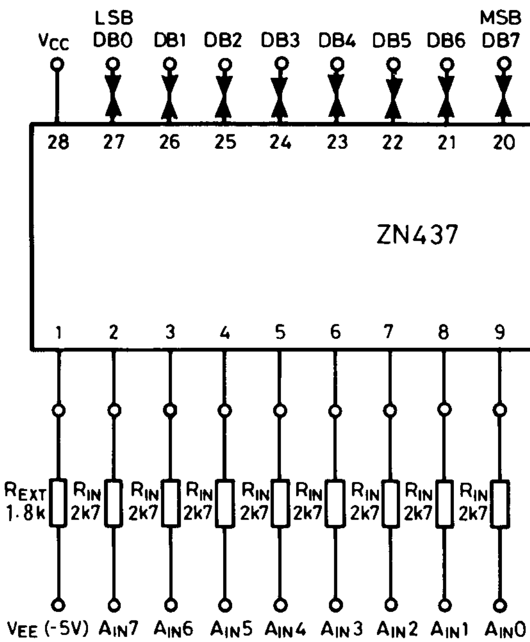



Fig. 12 External components for basic operation

## UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 13.

The values of $R_1$ and $R_2$ are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input ($A_{IN}$) is at full-scale.

The resulting full-scale range is given by: $A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right)$. $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance $R_1 // R_2$ ($R_{IN}$) = 2.7KΩ.

The required nominal values of $R_1$ and $R_2$ are given by $R_1 = 2.7GKΩ$, $R_2 = \frac{2.7G}{G-1}$ KΩ

Using these relationships a table of nominal values of $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5V$.

| Input range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| +5V | 2 | 5.4KΩ | 5.4KΩ |
| +10V | 4 | 10.8KΩ | 3.6KΩ |

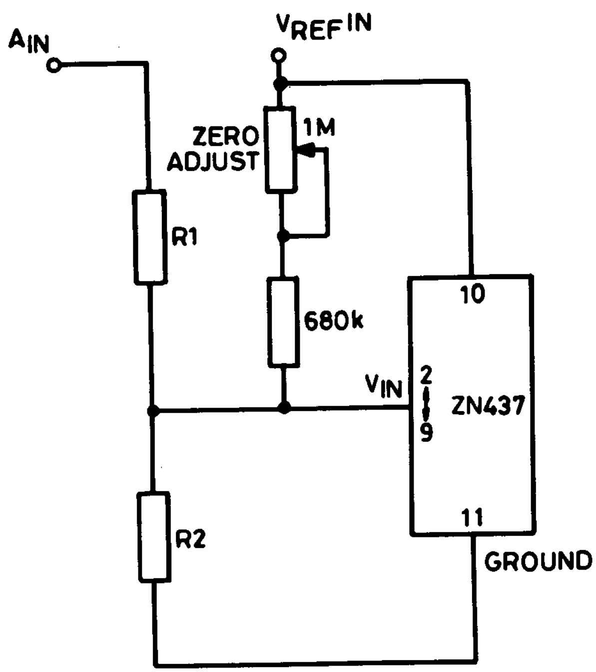



Fig. 13 General unipolar input connections

## GAIN ADJUSTMENT

Due to tolerances in $R_1$ and $R_2$, tolerances in $V_{REF}$ and the gain (full-scale) error of the DAC, some adjustment should be incorporated into $R_1$ to calibrate the full-scale of the converter. When used with 2% resistors a preset capable of adjusting $R_1$ by at least ±5% of its nominal value is suggested.

## ZERO ADJUSTMENT

Zero adjustment needs providing to set the zero transition to the value of +0.5LSB. This is achieved by applying an adjustable positive offset to the comparator input via P2 and $R_3$.

Practical circuits values for +5V and +10V input ranges are given in Fig. 14 which incorporates both zero and gain adjustments.

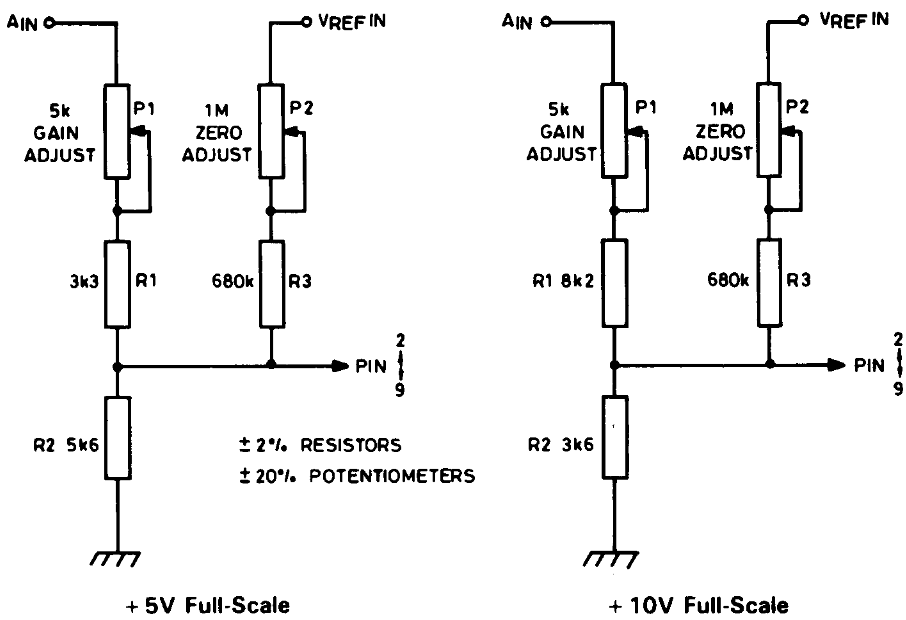



Fig. 14 Unipolar operation component values

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Select the required channel for continuous conversion as described earlier and monitor the digital outputs ($\overline{RD}$ will need to be pulsed appropriately with the address inputs selecting the correct channel).

### OFFSET SETTING

(ii) Apply 0.5LSB to $A_{IN}$ and adjust zero until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.

i.e. transition 00000000 to 00000001.

### GAIN SETTING

(iii) Apply full-scale minus 1.5LSB to $A_{IN}$ and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. transition 11111111 to 11111110.

### UNIPOLAR SETTING-UP POINTS

| Input range, +FS | 0.5LSB | FS - 1.5LSB |
|---|---|---|
| +5V | 9.8mV | 4.9707V |
| +10V | 19.5mV | 9.9414V |

$$1LSB = \frac{FS}{256}$$

### UNIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Binary) |
|---|---|
| FS - 1LSB | 11111111 |
| FS - 2LSB | 11111110 |
| 0.75FS | 11000000 |
| 0.5FS + 1LSB | 10000001 |
| 0.5FS | 10000000 |
| 0.5FS - 1LSB | 01111111 |
| 0.25FS | 01000000 |
| 1LSB | 00000001 |
| 0 | 00000000 |

## BIPOLAR OPERATION

For bipolar operation the input to the ZN437 is offset by half full-scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and $V_{IN}$ (Fig. 15).

When $A_{IN} = -FS$, $V_{IN}$ needs to be equal to zero.

When $A_{IN} = +FS$, $V_{IN}$ needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm G.\ V_{REF\ IN}$ then $R_1 = (G - 1).\ R_2$ and $R_1 = G.\ R_3$ fulfil the required conditions.

To match the ladder resistance, $R_1//R_2//R_3$ $(= R_{IN}) = 2.7K\Omega$.

Thus the nominal values of $R_1$, $R_2$, $R_3$ are given by $R_1 = 5.4GK\Omega$, $R_2 = 5.4G/(G - 1)K\Omega$, $R_3 = 5.4K\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 5.4K\Omega$ and $R_2 = \infty$.

Assuming $V_{REF\ IN} = 2.5V$, the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

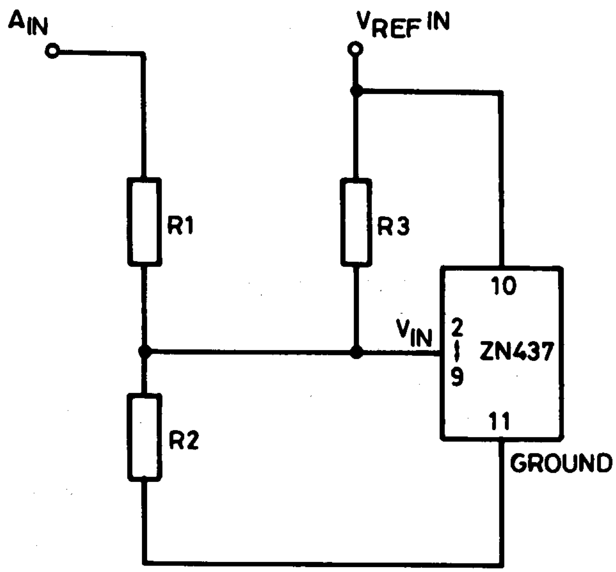



Fig. 15 Basic bipolar input connection

| Input range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| ±5V | 2 | 10.8KΩ | 10.8KΩ | 5.4KΩ |
| ±10V | 4 | 21.6KΩ | 7.2KΩ | 5.4KΩ |

Minus full-scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full-scale (gain) is set by adjusting $R_2$ relative to $R_1$. Practical circuit realisations are given in Fig. 16.

Note that $R_3$ will sink additional current from the reference to that required by $V_{REFIN}$ and this should be taken into consideration when selecting the reference components.

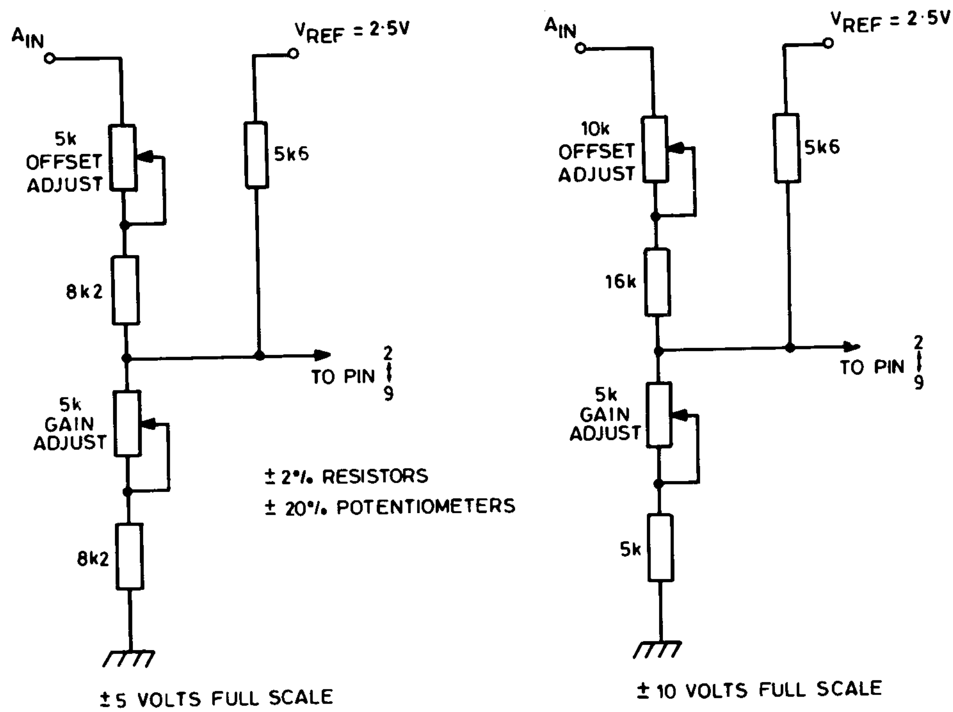



Fig. 16 Bipolar operation - component values

## BIPOLAR ADJUSTMENT PROCEDURE

(i) Select the required channel for continuous conversion as described earlier and monitor the digital outputs ($\overline{RD}$ will need to be pulsed appropriately with the address inputs selecting the correct channel).

### OFFSET SETTING

(ii) Apply − (FS - 0.5LSB) to $A_{IN}$ and adjust offset until the DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.

i.e. transition 00000000 to 00000001.

### GAIN SETTING

(iii) Apply + (FS - 1.5LSB) to $A_{IN}$ and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. transition 11111111 to 11111110.

### BIPOLAR SETTING-UP POINTS

| Input range, ± FS | − (FS − 0.5LSB) | + (FS − 1.5LSB) |
|---|---|---|
| ± 5V | − 4.9805V | + 4.9414V |
| ± 10V | − 9.9609V | + 9.8828V |

$$1\text{LSB} = \frac{2\text{FS}}{256}$$

### BIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Digital output code MSB LSB |
|---|---|
| + (FS - 1LSB) | 11111111 |
| + (FS - 2LSB) | 11111110 |
| + 0.5FS | 11000000 |
| + 1LSB | 10000001 |
| 0 | 10000000 |
| − 1LSB | 01111111 |
| − 0.5FS | 01000000 |
| − (FS - 1LSB) | 00000001 |
| − FS | 00000000 |

## MICROPROCESSOR INTERFACING TO THE 8086

The typical circuitry required to interface the ZN437 to the 8086 microprocessor is shown in Fig. 17. The ZN437 has been located within the IO memory map using standard address decoding techniques. The decoded address is used to gate either the microprocessor RD or WR through to the ZN437 depending on which cycle is being executed.

The clock is derived from the PCLK output of the 8284 clock generator which is half the frequency of the microprocessor clock. The A-D converter of the ZN437 can run at a maximum clock frequency of 500KHz. The clock pre-divider bits in the control register should therefore be set to ÷8. This will give a converter clock frequency of 312KHz for the 5MHz 8086 and 500KHz for the 8MHz 8086-2. For the 10MHz 8086-1 the PCLK output of the 8284 clock generator should be further divided by 2 using a flip flop divider. This ensures that the converter clock rate is not exceeded and corresponds to a converter clock frequency of 312KHz.

The ZN437 is an 8-bit device and is shown connected to the lower 8 bits (AD0-AD7) of the 16-bit bus. Each ZN437 RAM location must therefore be located on an even address boundary. This is because the 8086 reads data from bits AD8-AD15 when reading from odd addresses. Similarly to write a Control Word to the ZN437 an IO write is performed to an even address in the 16 byte block enabled by the address decoding logic. Writing to any of the 8 even addresses will result in the word being written to the control register. This is because the state of the ZN437 address inputs is irrelevant during a ZN437 write cycle.

As an example assume the address decoding gives an active low output for an IO address of 100X hex, (where 'X' is any hex number). The addresses of the ZN437 RAM locations are shown below.

Therefore reading from IO address 1004 reads the converted data from analogue input 2.

It should be noted that as the ZN437 is an 8-bit device it is not necessary to decode the AD0 and BHE signals of the 8086.

## HIGH SPEED INTERFACING

The high speed 8086-2 and 8086-1 have minimum access times of 130 and 125ns respectively. To interface these microprocessors to the ZN437 the wait state should be inserted in the ZN437 read cycle. This is shown by the dotted box in the circuit diagram of Fig. 17.

| IO address | ZN437 RAM address | Corresponding input channel |
|---|---|---|
| 1000 | 0 | $A_{IN}$ 0 |
| 1002 | 1 | $A_{IN}$ 1 |
| 1004 | 2 | $A_{IN}$ 2 |
| 1006 | 3 | $A_{IN}$ 3 |
| 1008 | 4 | $A_{IN}$ 4 |
| 100A | 5 | $A_{IN}$ 5 |
| 100C | 6 | $A_{IN}$ 6 |
| 100E | 7 | $A_{IN}$ 7 |

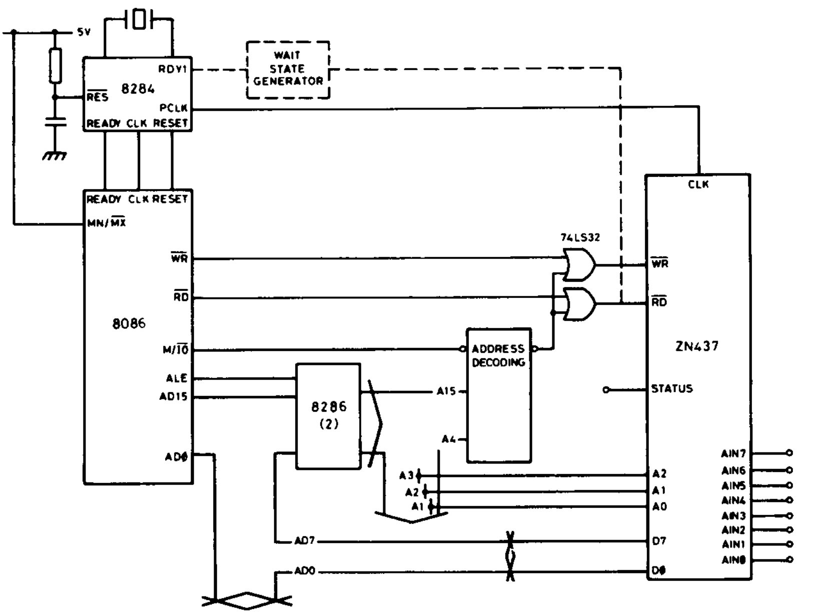



Fig. 17 ZN437 - 8086 interface

## 8088 INTERFACING

Fig. 18 shows the typical circuitry required to interface the ZN437 to the 8088. As can be seen from the diagram the circuitry is very similar to that required for the 8086. The main difference is the addressing of the ZN437 RAM. As the data bus is now only 8-bits wide every microprocessor read whether from odd or even addresses reads data from AD0-AD7. Therefore each ZN437 RAM location no longer has to lie on an even address boundary and so they can now occupy consecutive addresses.

To illustrate this consider the example used with the 8086. Here the address decoding gives an active low output pulse for an IO address of 100X hex, (where 'X' is any hex number). However in this case as AD3 is also decoded we will assume it has to be low. The addresses of the ZN437 RAM locations are shown below.

| IO address | ZN437 RAM address | Corresponding input channel |
|---|---|---|
| 1000 | 0 | $A_{IN}$ 0 |
| 1001 | 1 | $A_{IN}$ 1 |
| 1002 | 2 | $A_{IN}$ 2 |
| 1003 | 3 | $A_{IN}$ 3 |
| 1004 | 4 | $A_{IN}$ 4 |
| 1005 | 5 | $A_{IN}$ 5 |
| 1006 | 6 | $A_{IN}$ 6 |
| 1007 | 7 | $A_{IN}$ 7 |

As with the 8086 when using the higher speed version, the 8MHz 8088-2, the wait state should be inserted into the ZN437 read cycle.

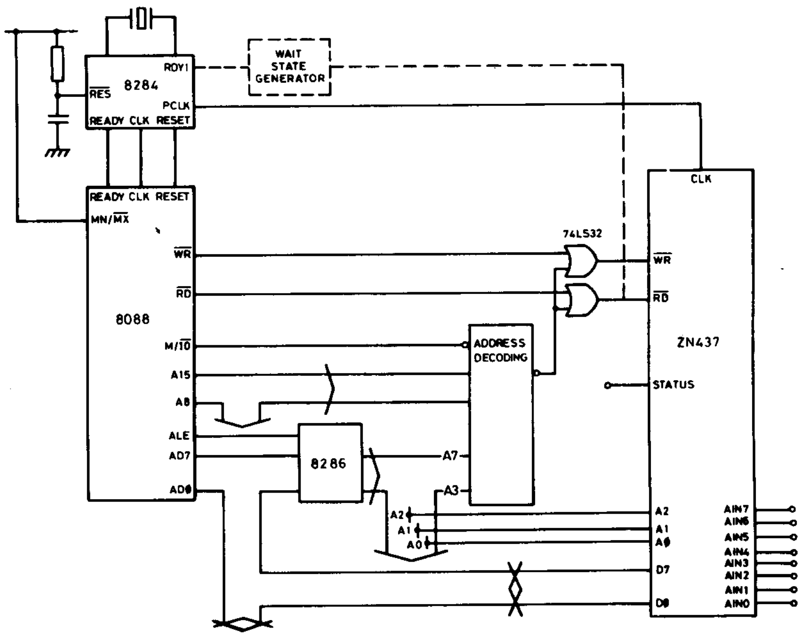



Fig. 18

## INTERFACING TO THE Z80 MICROPROCESSOR

The ZN437 can easily be interfaced to the Z80, Z80A or Z80B microprocessors, as shown in Fig. 19.

The data lines from the microprocessor are connected directly to DB0-DB7 on the ZN437 for bi-directional data transfer. Some of the lower 8 address lines are decoded along with the I/O RQ line to gate through the RD and WR signals to the ZN437 as required. The decoded WR signal is used by the ZN437 to latch in the Control Word. The decoded RD signal is used to enable data onto the data bus from the location in the 8 × 8 bit RAM selected by the ZN437 address inputs $A_0$, $A_1$ and $A_2$.

The microprocessor clock can be connected directly to the ZN437 clock input when using the Z80 or Z80A. The Z80B will require an external ÷ 2 circuit. The ZN437 clock input is then divided down, as governed by the Control Word and should be set to give an internal clock of 500KHz or less.

The STATUS output goes low when a conversion is complete. This can be used to generate an interrupt or to set a flag for polling. Alternatively STATUS can be left open circuit and a software delay used to ensure the conversion is complete.

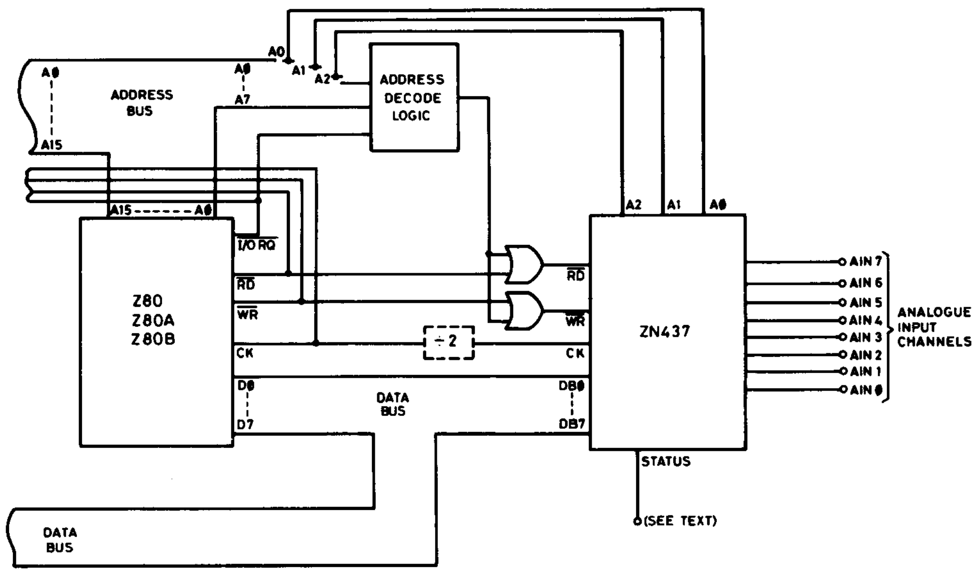



Fig. 19 Interfacing the ZN437 to the Z80 (schematic)