PYRAMID
SEMICONDUCTOR CORPORATION

P54FCT240T/74FCT240T

INVERTING OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

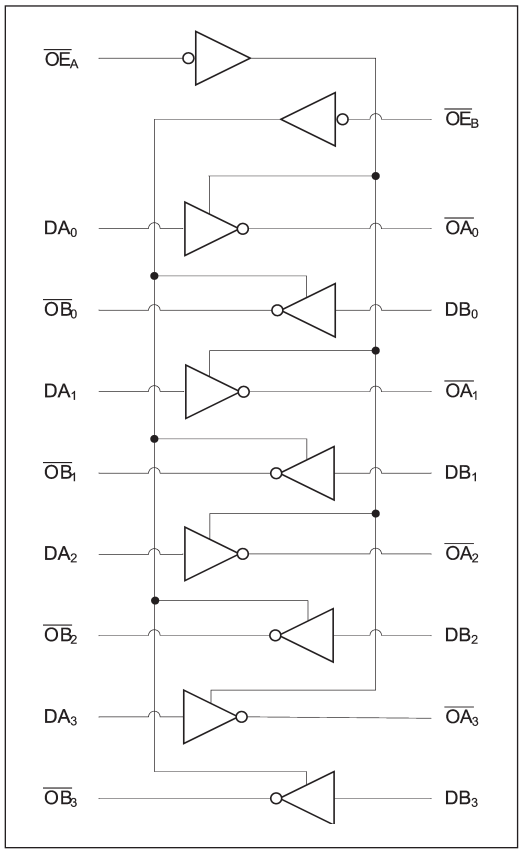
FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-A speed at 5.1ns max (MIL)**
- **Reduced VOH (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **48 mA sink current, 12 mA source current (MIL)**

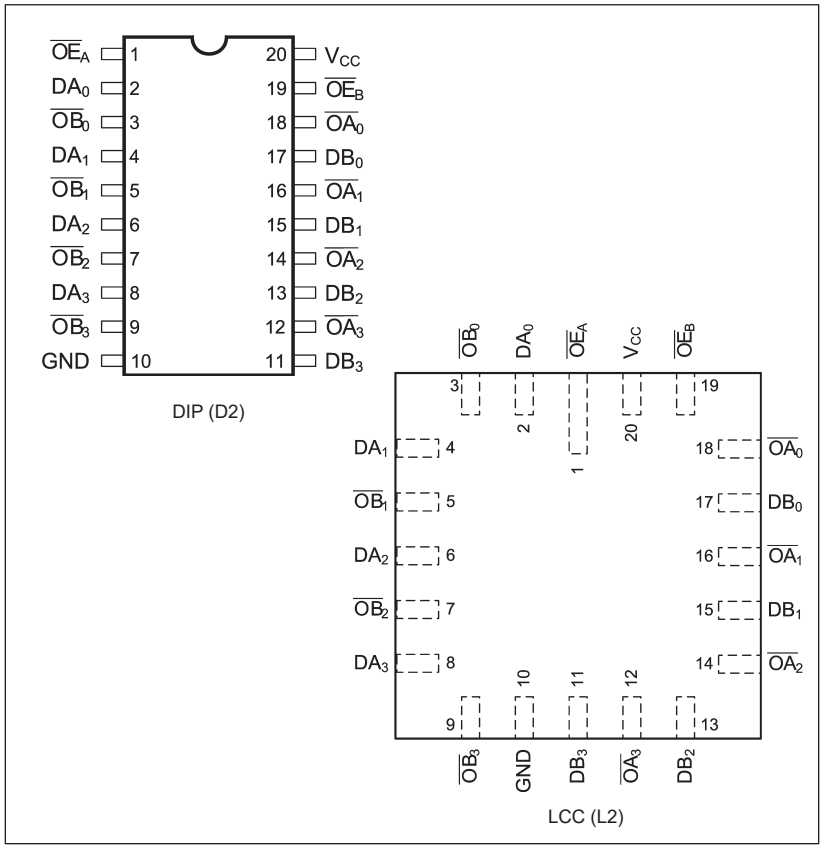
DESCRIPTION

The P54/74FCT240T is an inverting octal buffer and line driver designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. The device provides speed and drive capabilities equivalent to the fastest bipolar logic counterparts while reducing power dissipation by using advanced CMOS technoloy. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without external components.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1,2]

Sym	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-65 to +135	°C
V_{CC}	V_{CC} Potentional to Ground	-0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	-0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Grade	Ambient Temp	GND	V_{cc}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 5%

CAPACITANCES

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	Test Conditions	Min	Max	Unit
V_{OH1}	High Level Output Voltage	For all inputs affecting output under test V_{IN} = 2.0V or 0.8V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -300 µA, V_{CC} = V_{CC} (Min)	3.0	V_{CC} - 0.5	V
V_{OH2}		For all inputs affecting output under test V_{IN} = 2.0V or 0.8V For all other inputs V_{IN} = V_{CC} or GND I_{OH} = -12 mA, V_{CC} = V_{CC} (Min)	2.4	V_{CC} - 0.5	V
V_{OL1}	Low Level Output Voltage	For all inputs affecting output under test V_{IN} = 2.0V or 0.8V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 300 µA, V_{CC} = V_{CC} (Min)		0.20	V
V_{OL2}		For all inputs affecting output under test V_{IN} = 2.0V or 0.8V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 48 mA, V_{CC} = V_{CC} (Min)		0.55	V
I_{OZH}	Three-State Output Leakage Current High	$\overline{OE}_n$ = V_{IH} or V_{IL} V_{IH} = 2.0V, V_{IL} = 0.8V For all other inputs, V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}, V_{CC} = V_{CC} (Max)		1.0	µA
I_{OZL}	Three-State Output Leakage Current Low	$\overline{OE}_n$ = V_{IH} or V_{IL} V_{IH} = 2.0V, V_{IL} = 0.8V For all other inputs, V_{IN} = V_{CC} or GND V_{OUT} = GND, V_{CC} = V_{CC} (Max)		1.0	µA
V_{IC-}	Negative Input Clamp Voltage	For input under test, I_{IN} = -18 mA, V_{CC} = V_{CC} (Min)		-1.2	V
I_{IH}	Input Current High	For input under test, V_{IN} = V_{CC} For all other inputs, V_{IN} = V_{CC} or GND, V_{CC} = V_{CC} (Max)		+1.0	µA
I_{IL}	Input Current Low	For input under test, V_{IN} = GND For all other inputs, V_{IN} = V_{CC} or GND, V_{CC} = V_{CC} (Max)		-1.0	µA
C_{IN}	Input Capacitance	T_C = +25°C, V_{CC} = GND, F = 1 MHz		10	pF
C_{OUT}	Output Capacitance	T_C = +25°C, V_{CC} = GND, F = 1 MHz		12	pF

Notes:

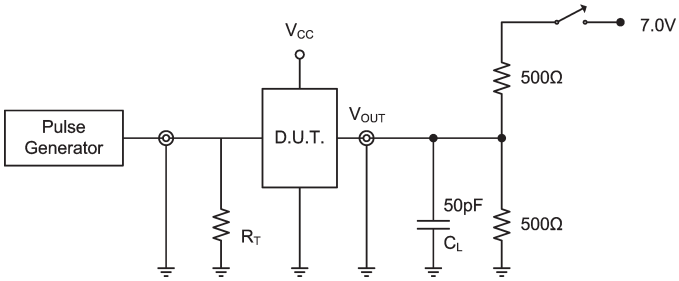
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

Sym	Parameter	Test Conditions			Min	Max	Unit
I_{OS}	Output Short Circuit Current	For all inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = GND, $V_{CC} = V_{CC}$ (Max)			-60	-225	mA
I_{CCD}	Dynamic Power Supply Current	Outputs open, $V_{CC} = V_{CC}$ (Max)				0.25	mA/MHz
ΔI_{CC}	Quiescent Supply Current Delta, TTL Input Level	For input under test, $V_{IN} = V_{CC}$ - 2.1 V For all other inputs, $V_{IN} = V_{CC}$ or GND, $V_{CC} = V_{CC}$ (Max)				2.0	mA
I_{CCH}	Quiescent Supply Current, Outputs High	$\overline{OE_n}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND, $V_{CC} = V_{CC}$ (Max)				1.5	mA
I_{CCL}	Quiescent Supply Current, Outputs Low					1.5	mA
I_{CCZ}	Quiescent Supply Current, Outputs Three-State	$\overline{OE_n} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND, $V_{CC} = V_{CC}$ (Max)				1.5	mA
I_{CCT1}	Total Supply Current	Outputs open $\overline{OE_A}$ + $\overline{OE_B}$ = GND 50% duty cycle For nonswitching input, $V_{IN} = V_{CC}$ or GND, $V_{CC} = V_{CC}$ (Max)	f_i = 10 MHz One bit toggling	For switching inputs, $V_{IN} = V_{CC}$ or GND		4.0	mA
				For switching inputs, V_{IN} = 3.4 V or GND		5.0	
			f_i = 2.5 MHz Eight bits toggling	For switching inputs, $V_{IN} = V_{CC}$ or GND		6.5	
				For switching inputs, V_{IN} = 3.4 V or GND		14.5	
V_{OLP}	Low Level Ground Bounce Noise	V_{IH} = 3.0 V, V_{IL} = 0.0 V, T_A = +25°C, V_{CC} = 5.0 V				1160	mV
V_{OLV}						-1020	
V_{OHP}	High Level V_{CC} Bounce Noise					460	
V_{OHV}						-400	

AC CHARACTERISTICS

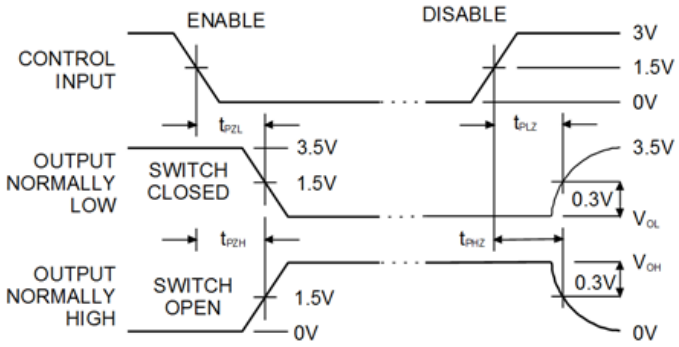
(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	Condition	54/74FCT240T				54/74FCT240AT				Unit
			Ind		Mil		Ind		Mil		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_X to $\overline{O}_{\overline{XX}}$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	9.5	1.5	10.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.0	1.5	10.0	1.5	5.6	1.5	5.9	ns

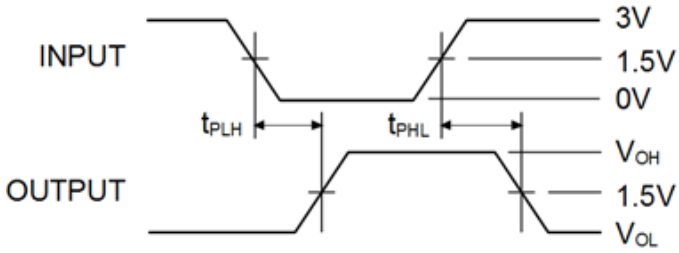


Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

ENABLE/DISABLE TIMES



PROPAGATION DELAY



PIN DESCRIPTION

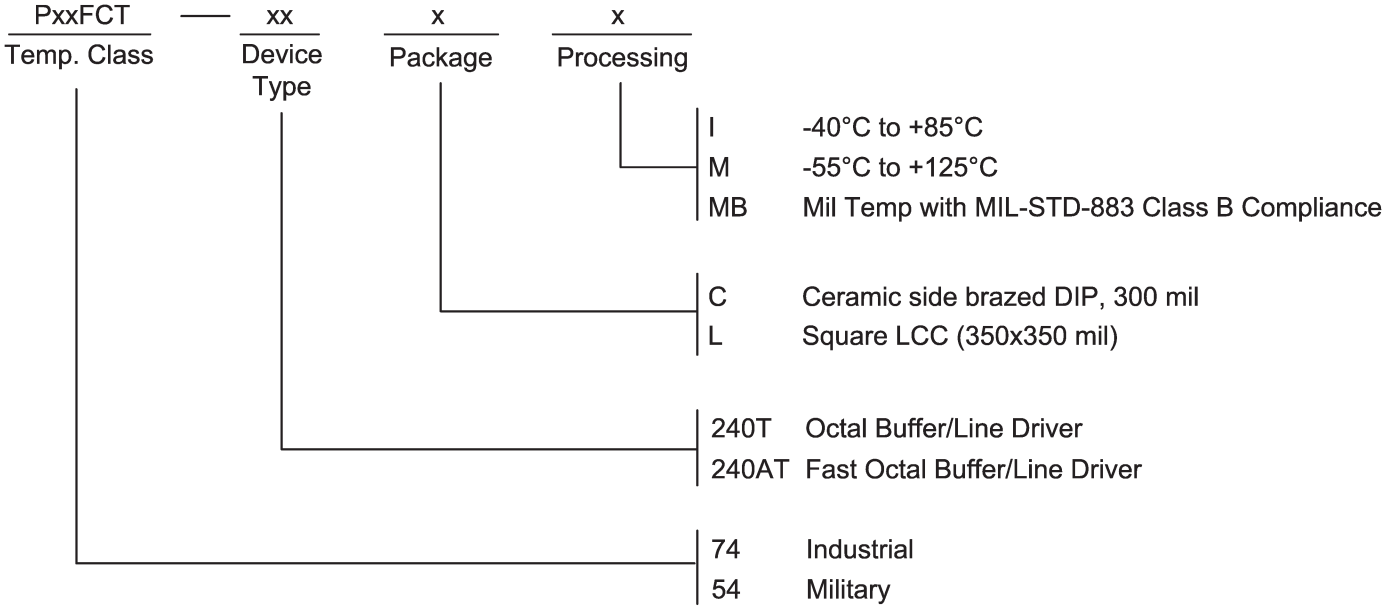
Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	Output Enable Inputs (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

FUNCTION TABLE

Inputs			Outputs
$\overline{OE}_A$	$\overline{OE}_B$	D	$\overline{O}_{\overline{XX}}$
L	L	L	H
L	L	H	L
H	H	X	Z

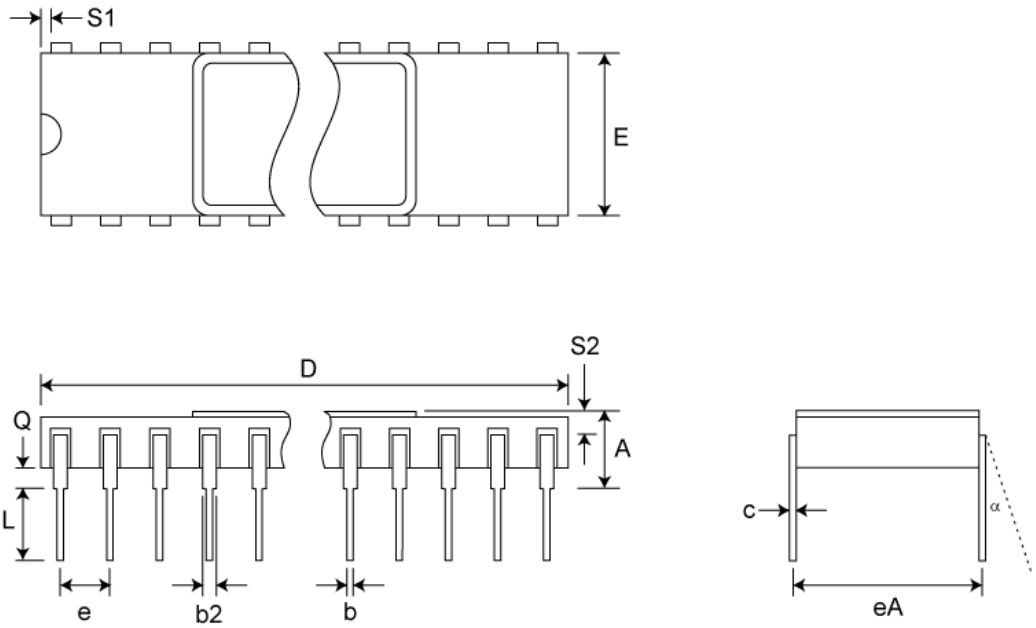
H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High Impedance

ORDERING INFORMATION



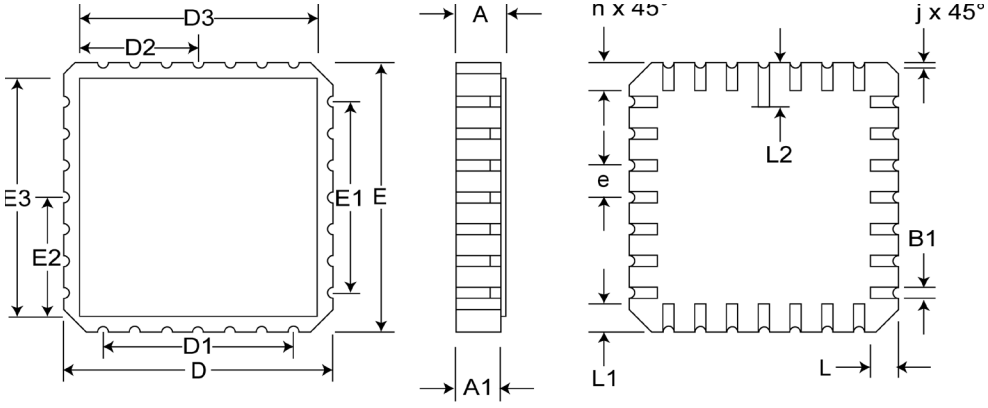
Pkg #	D2	
# Pins	20 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	-	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-
α	0°	15°

SIDEBRAZED DUAL INLINE PACKAGE



Pkg #	L2	
# Pins	20	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.342	0.358
D1/E1	0.200 BSC	
D2/E2	0.100 BSC	
D3/E3	-	0.358
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	5	

SQUARE LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	LOGIC104
DOCUMENT TITLE	P54FCT240T - OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Dec 2015	JDB	New Data Sheet
01	Feb 2016	JDB	Updated DC Electrical Characteristics
02	Mar 2016	JDB	DC Electrical Characteristics
03	Mar 2016	JDB	DC Electrical Characteristics