KS54HCTLS/KS74HCTLS 195

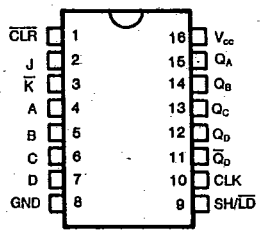
4-Bit Bidirectional Universal Shift Registers

T-46-09-05

FEATURES

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and K Inputs to First Stage**
- **Right-shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74HCTLS: −40°C to +85°C KS54HCTLS: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction A_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associate flip-flops and appears at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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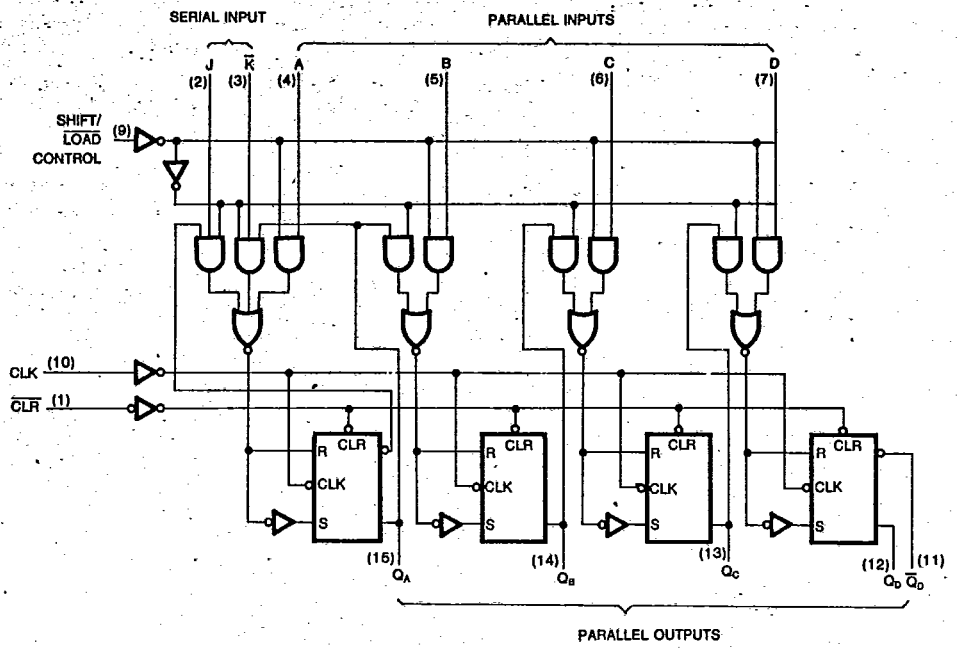
FUNCTION TABLE

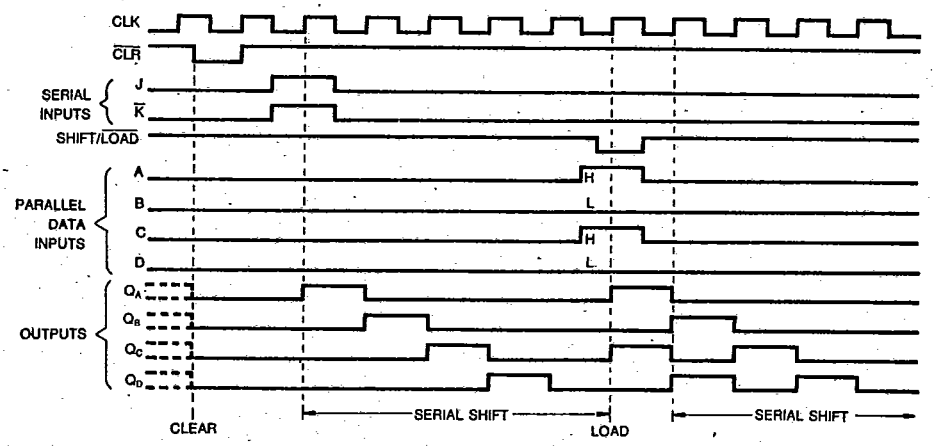
INPUTS									OUTPOUTS				
$\overline{CLR}$	SHIFT/$\overline{LOAD}$	CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}=the level of Q_A, Q_B or Q_C, respectively, before the mostrecent transition of the clock.

LOGIC DIAGRAM



typical clear, shift, and load sequences



Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS195

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$		Unit
				Typ	Guaranteed Limits				
Maximum Clock Frequency		f_{max}	$C_L = 50pF$	50	30		25	20	MHz
Maximum Propagation Delay, CLK to Q_H		t_{PLH}		18	24		30	36	ns
		t_{PHL}		18	24		30	36	ns
Maximum Propagation Delay, $\overline{CLR}$ to Q_H		t_{PHL}		21	28		35	42	ns
Maximum Pulse Width	$\overline{CLR}$ Low	t_w		10	12		15	20	ns
	CLK High or Low			12	16		20	24	
Minimum Setup Time before CLK†	SH/$\overline{LD}$ High	t_{su}		15	20		25	25	ns
	Serial or Parallel			12	15		20	24	
	$\overline{CLR}$ inactive			15	20		25	25	
Minimum Hold Time after CLK†	SH/$\overline{LD}$ High	t_h		−3	0			0	ns
	Serial or Parallel Data			−3	0			0	
Maximum Input Capacitance		C_{IN}		5					pF
Power Dissipation Capacitance*		C_{PD}							pF

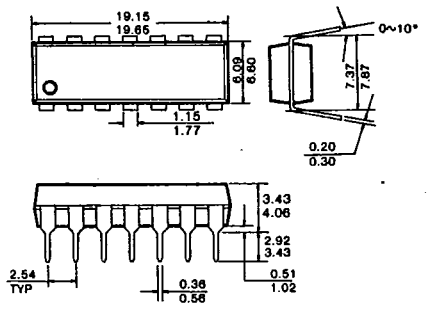
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

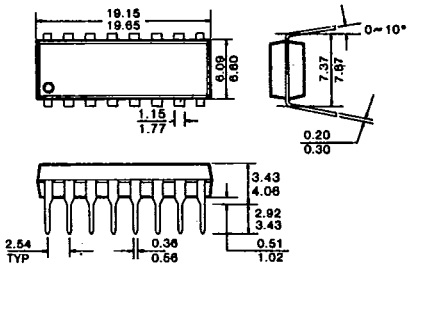
T-90-20

1. PLASTIC PACKAGES

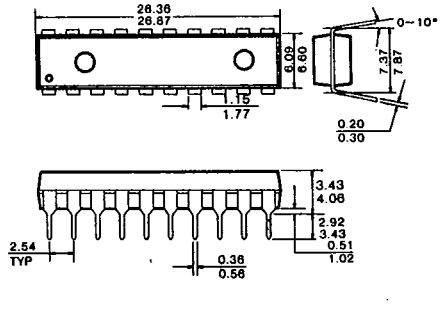
14-Pin Plastic DIP **Units: mm**



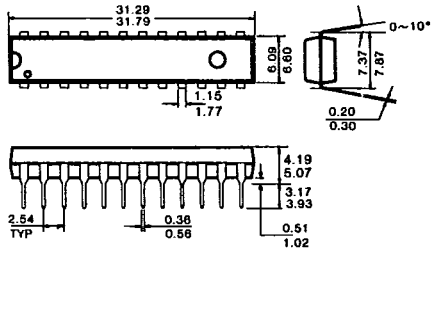
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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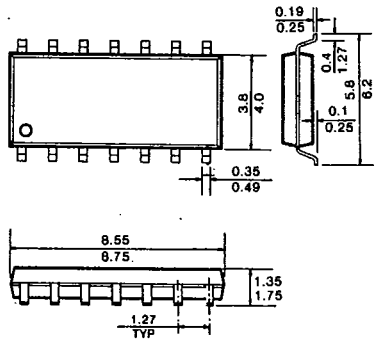
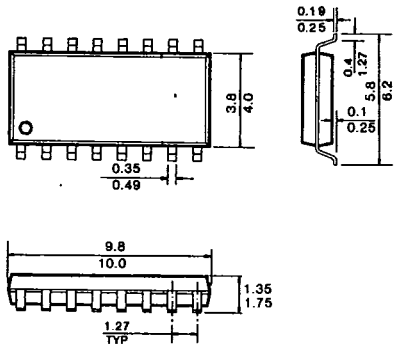
14-Pin SOP

Unit: mm



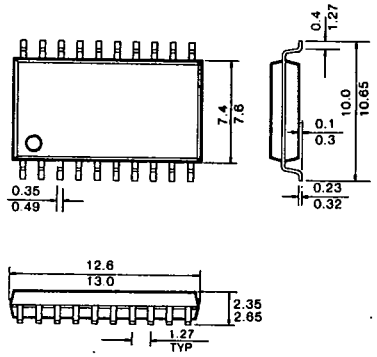
16-Pin SOP

Unit: mm



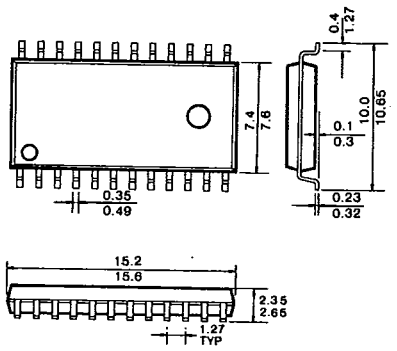
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm



PACKAGE DIMENSIONS

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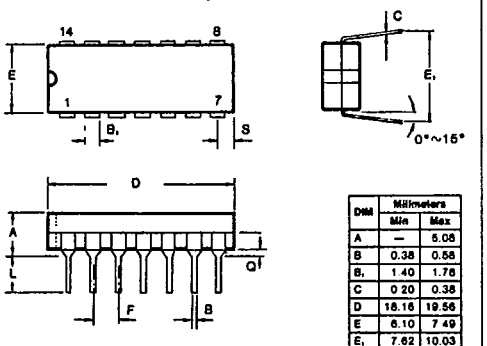
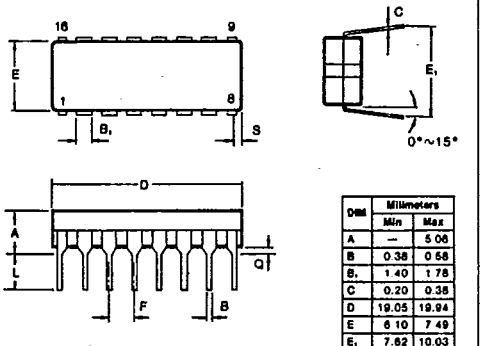
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



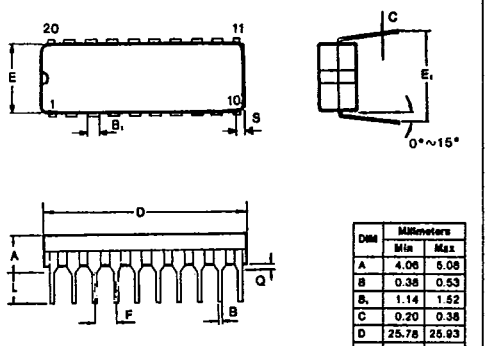
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



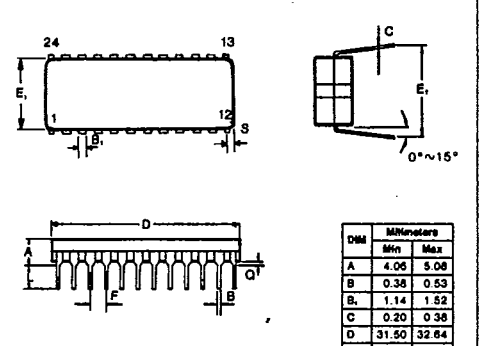
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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