4M × 4Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C4002-6	60ns	15ns	110ns
KM44C4002-7	70ns	20ns	130ns
KM44C4002-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Double +5V±10% power supply**
- **4096 cycles/64ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

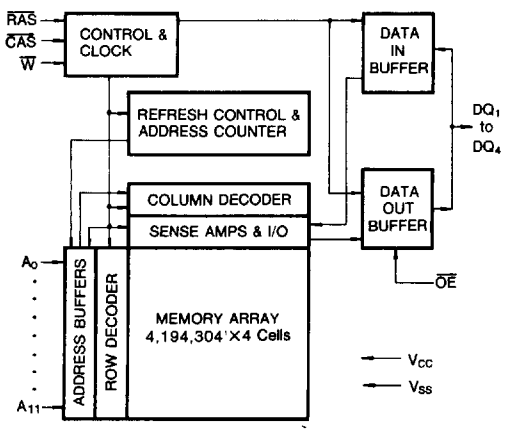
The Samsung KM44C4002 is a high speed CMOS 4,194,304×4 Dynamic Random Access Memory. Its Design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C4002 features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

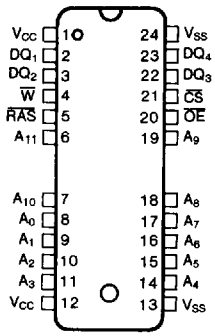
The KM44C4002 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

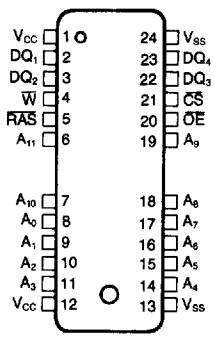


PIN CONFIGURATION (Top Views)

• KM44C4002J

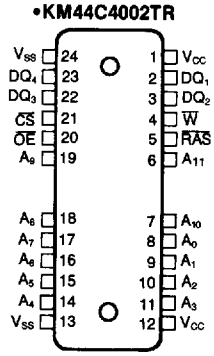


•KM44C4002T



(TSOP(II)-Forward)

•KM44C4002TR



(TSOP (II)-Reverse)

Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_1-DQ_4	Data In / Data out
$\overline{W}$	Read / Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power(+5V)
V_{SS}	Ground
$\overline{OE}$	Data Out Enable

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM44C4002-6	I_{CC1}	—	90	mA
	KM44C4002-7		—	80	mA
	KM44C4002-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM44C4002-6	I_{CC3}	—	90	mA
	KM44C4002-7		—	80	mA
	KM44C4002-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM44C4002-6	I_{CC4}	—	80	mA
	KM44C4002-7		—	70	mA
	KM44C4002-8		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM44C4002-6	I_{CC6}	—	90	mA
	KM44C4002-7		—	80	mA
	KM44C4002-8		—	70	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, address should be changed only once while $\overline{RAS}$ = V_{IL}. In I_{CC4}, address should be changed only once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance(DQ_1-DQ_4)	C_{IN3}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C4002-6		KM44C4002-7		KM44C4002-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C4002-6		KM44C4002-7		KM44C4002-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4,096 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Static column mode cycle time	t_{SC}	35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	85		100		110		ns	
Access time from last write	t_{ALW}		55		65		75	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		45		55	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	15	200,000	20	200,000	20	200,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	50		55		60		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	25	20	30	20	35	ns	
Last write to column address hold time	t_{AHLW}	55		65		75		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (test in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
W to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
W to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output butter turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	

TEST MODE CYCLE

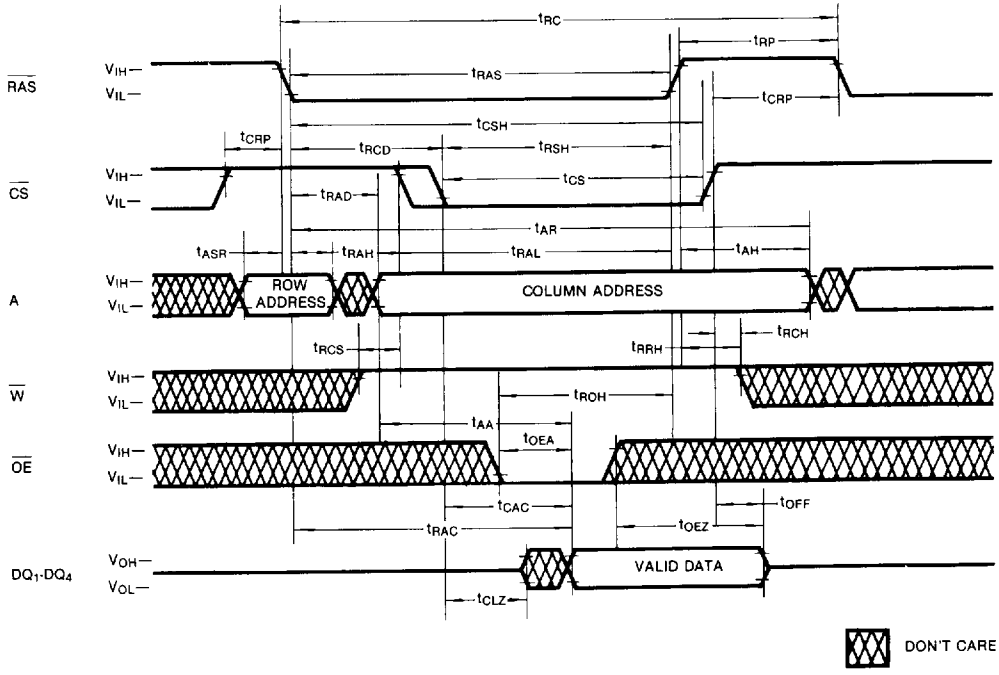
Parameter	Symbol	KM44C4002-6		KM44C4002-7		KM44C4002-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	45		55		55		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	7
Static column mode cycle time	t_{SC}	40		45		50		ns	
Static column mode read-modify-write	t_{SRWC}	90		105		115		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	t_{ALW}		60		70		80	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	200,000	25	200,000	25	200,000	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

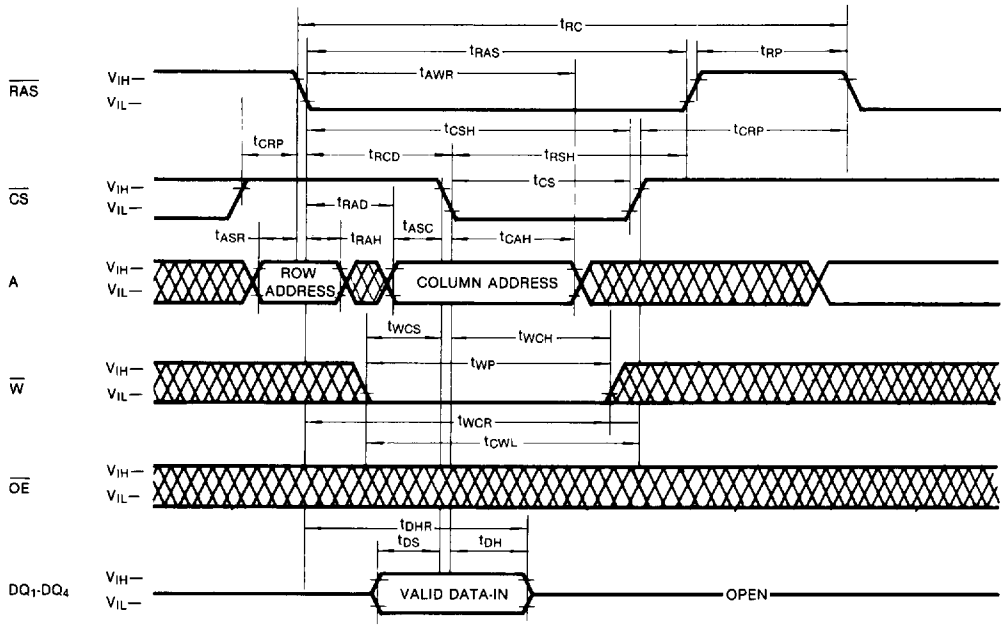
TIMING DIAGRAMS

READ CYCLE

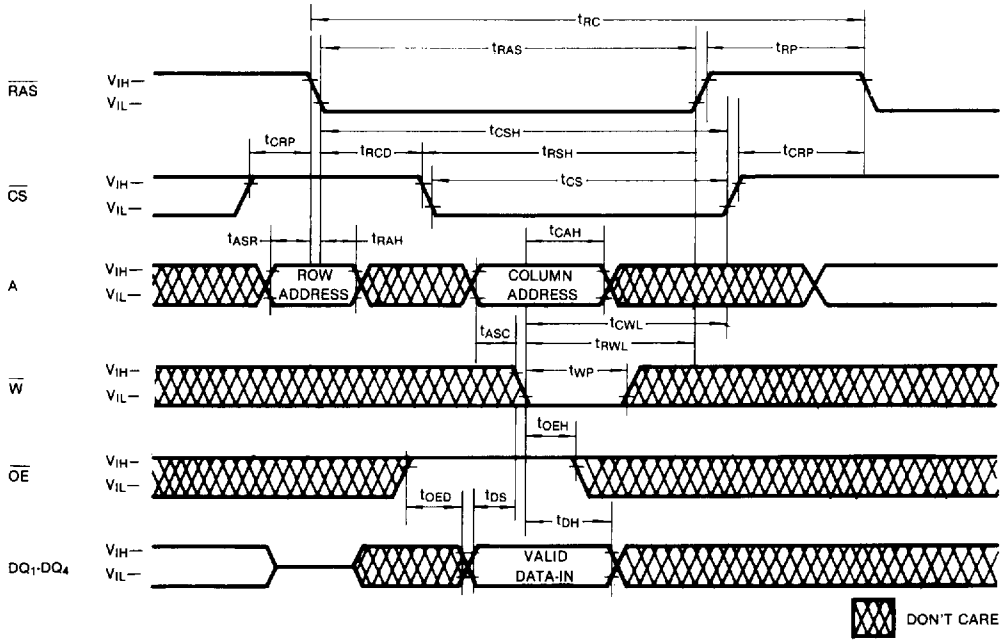


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



WRITE CYCLE (OE CONTROLLED WRITE)



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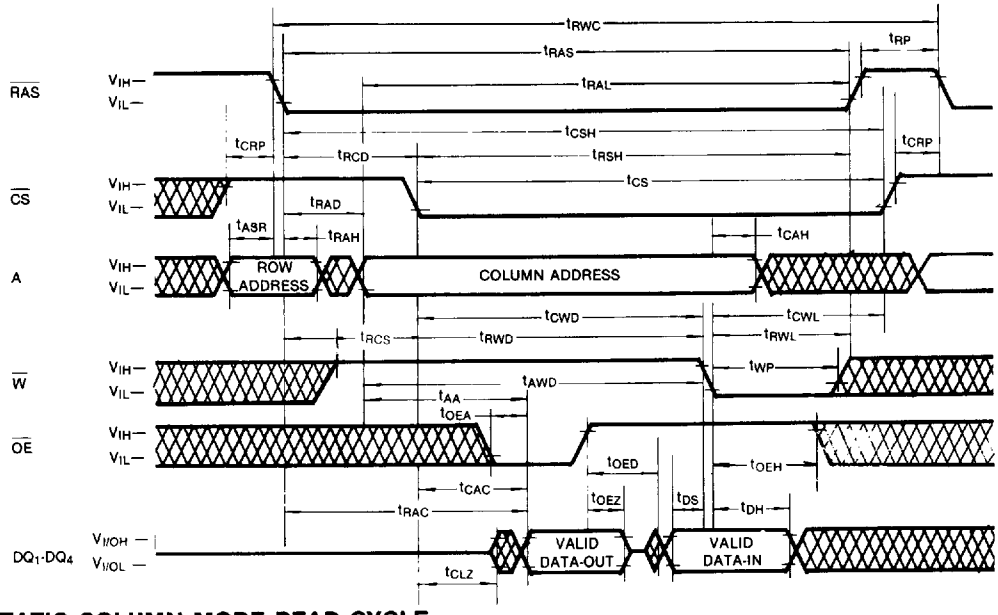
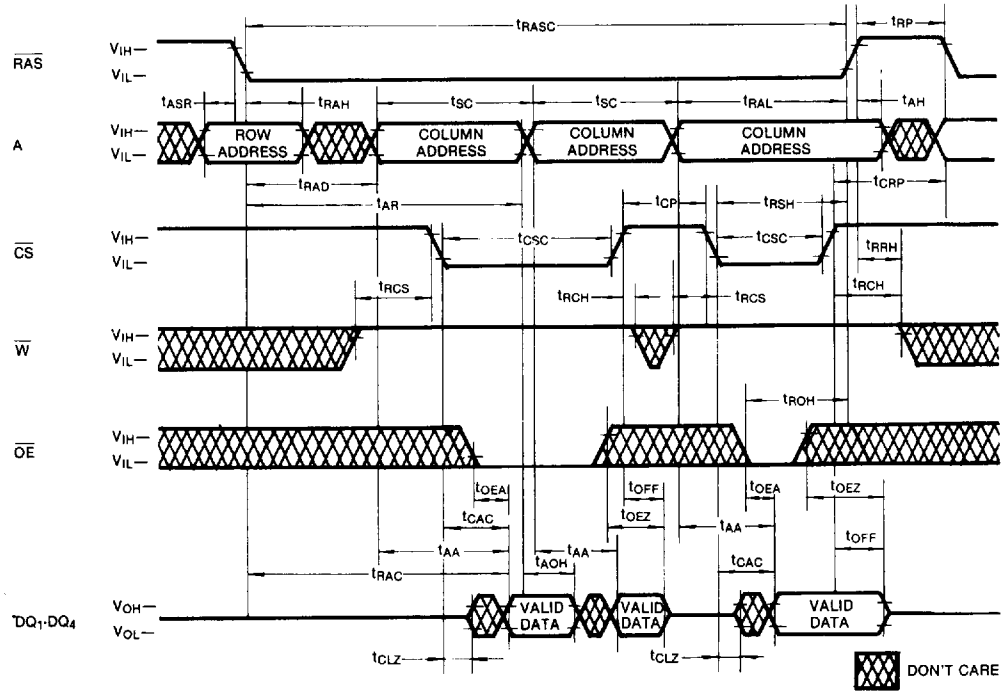
TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

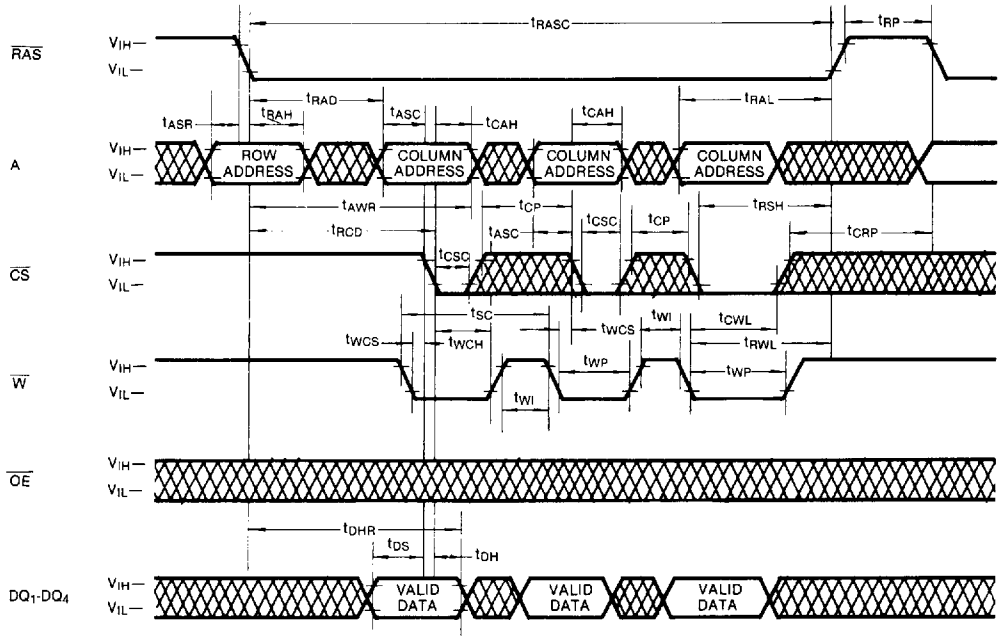


STATIC COLUMN MODE READ CYCLE

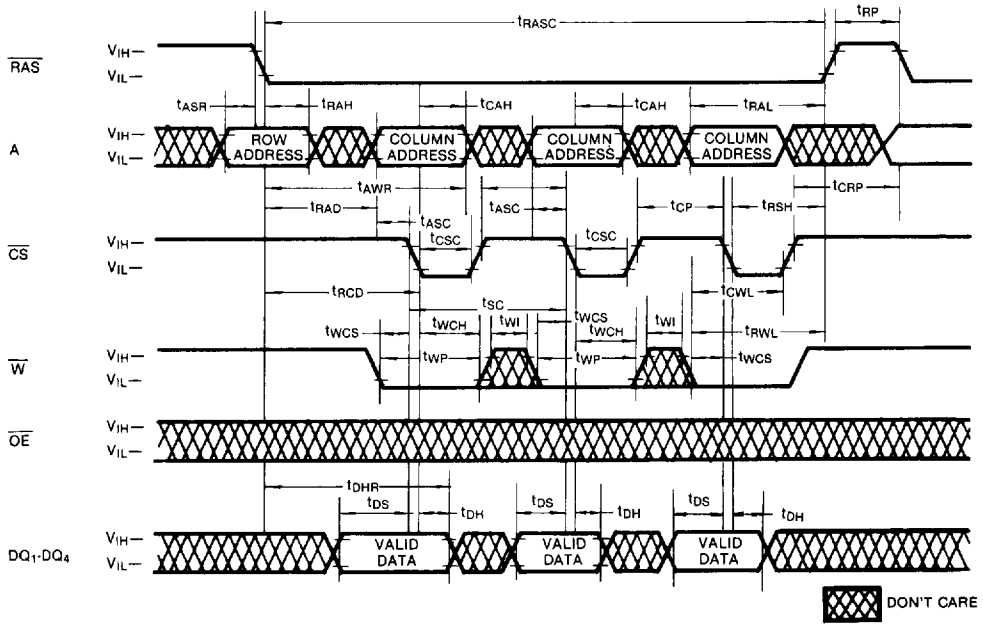


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)



STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



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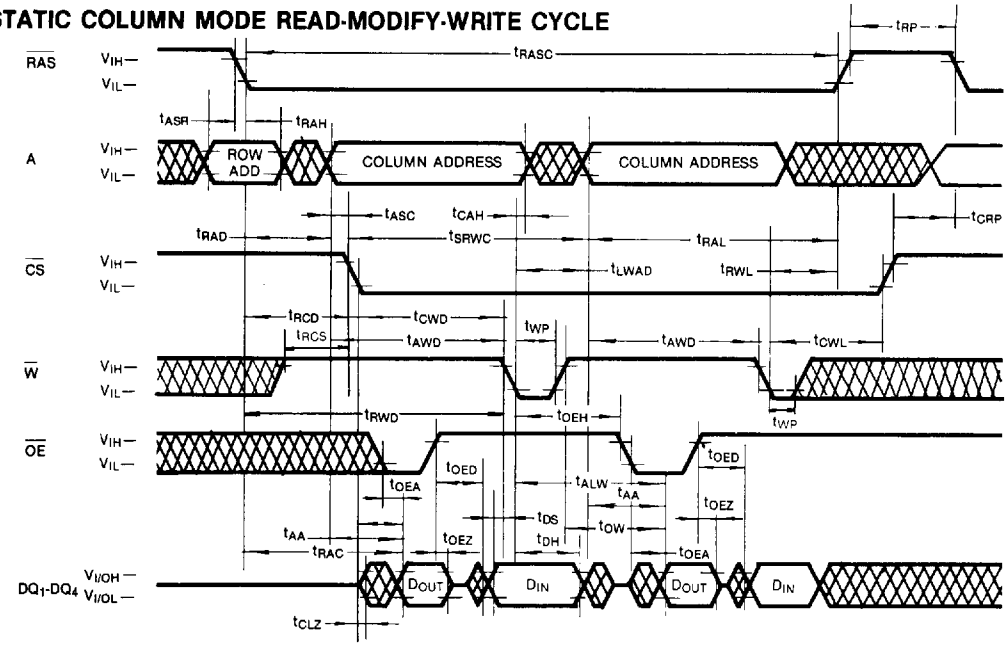
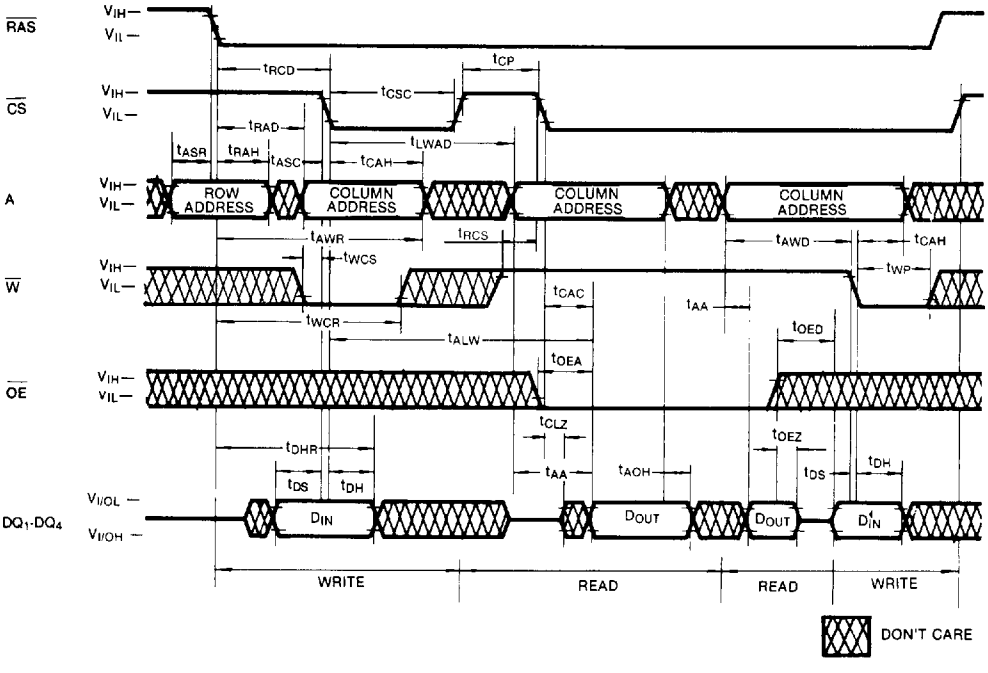
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



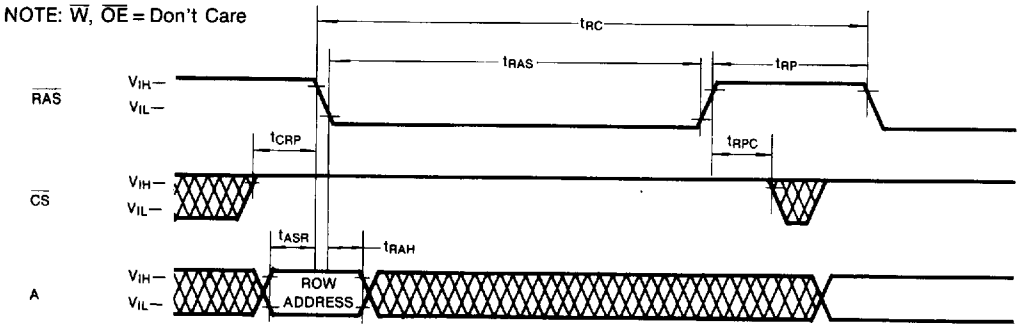
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

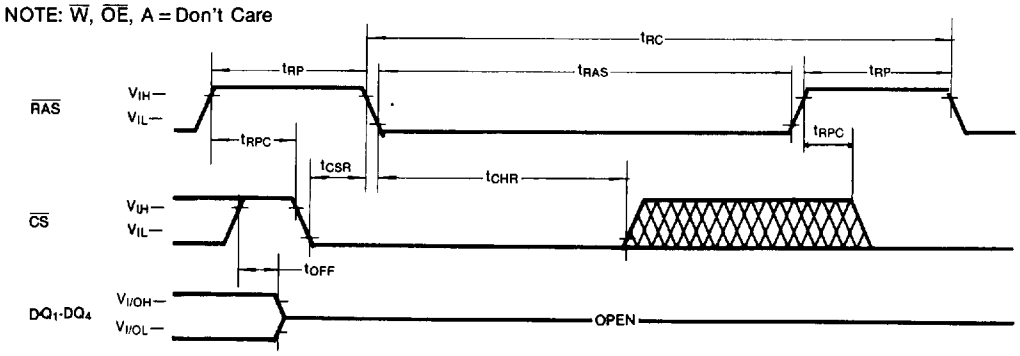
RAS-ONLY REFRESH CYCLE

NOTE: W, OE = Don't Care



CS-BEFORE-RAS REFRESH CYCLE

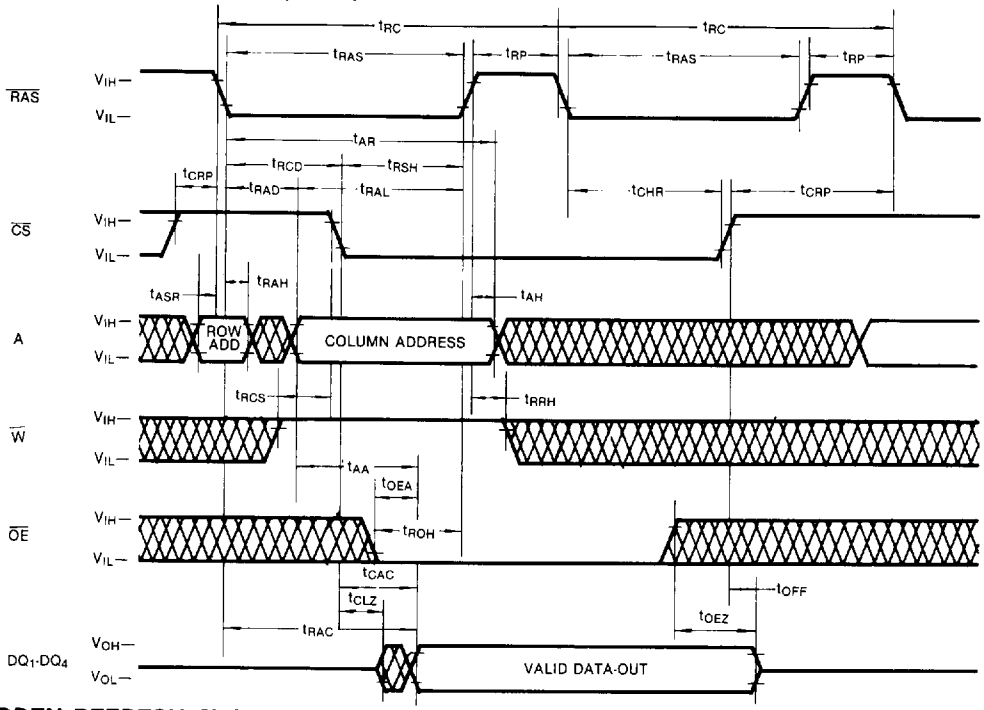
NOTE: W, OE, A = Don't Care



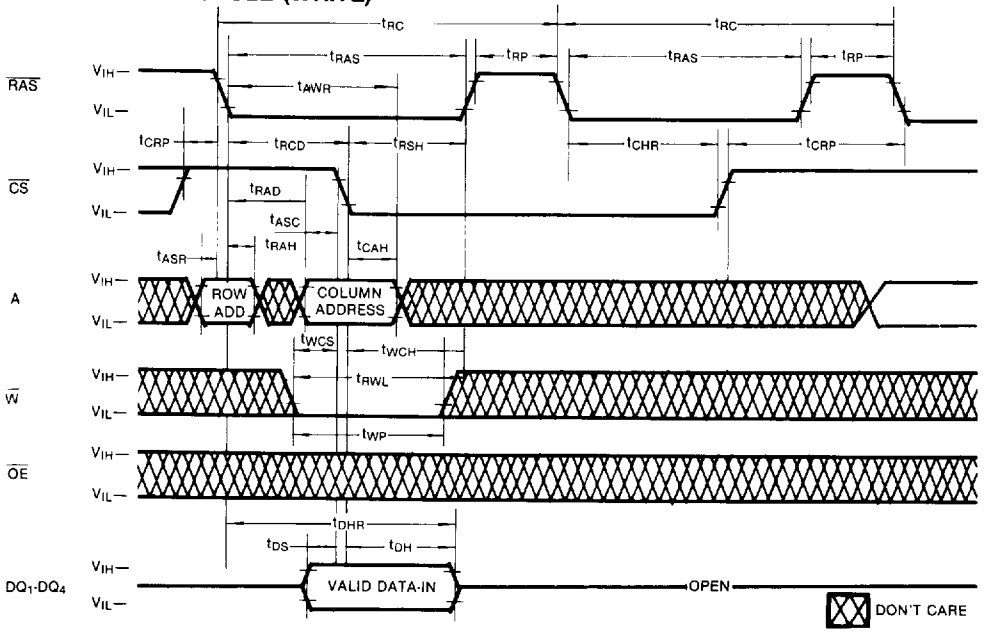
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

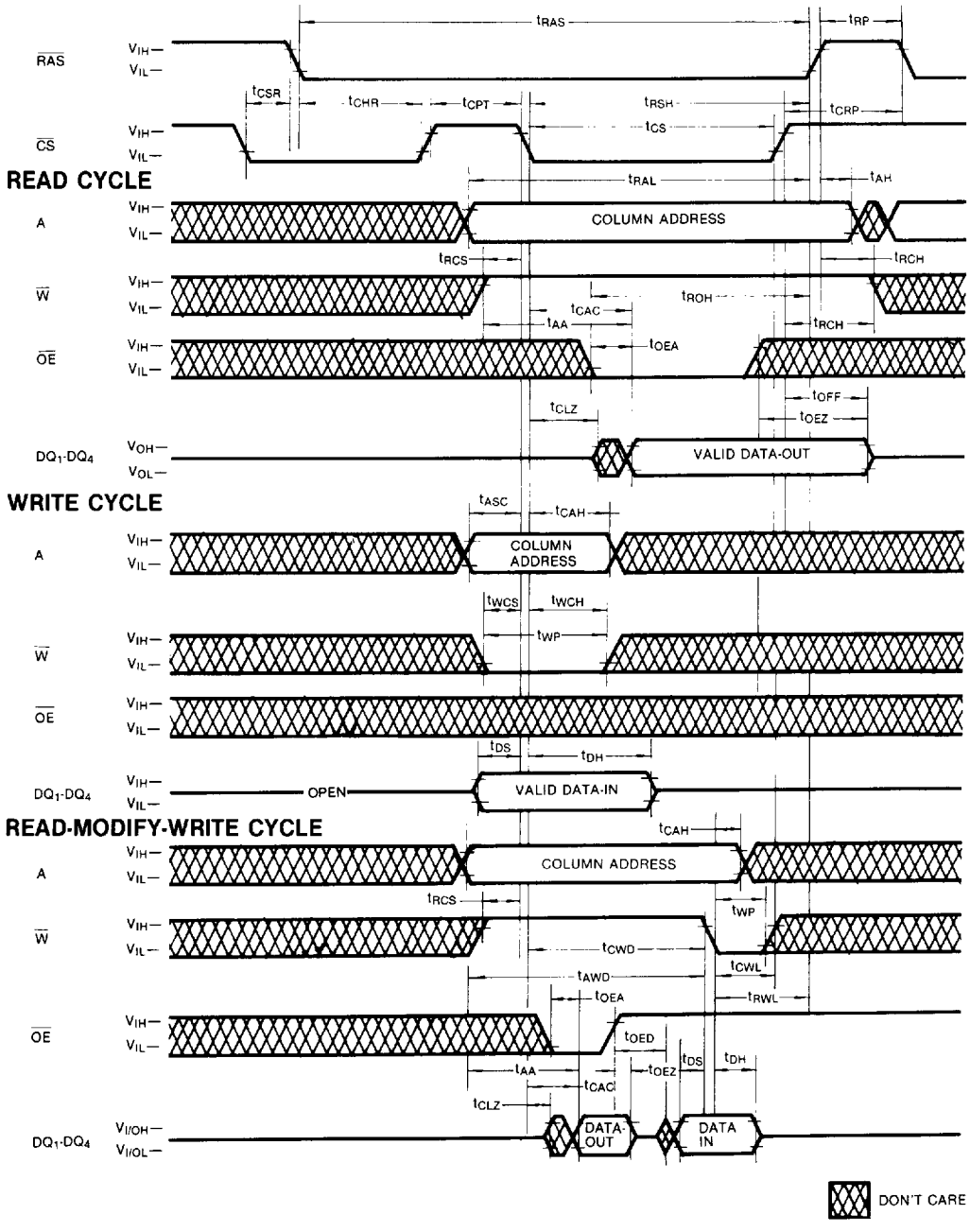


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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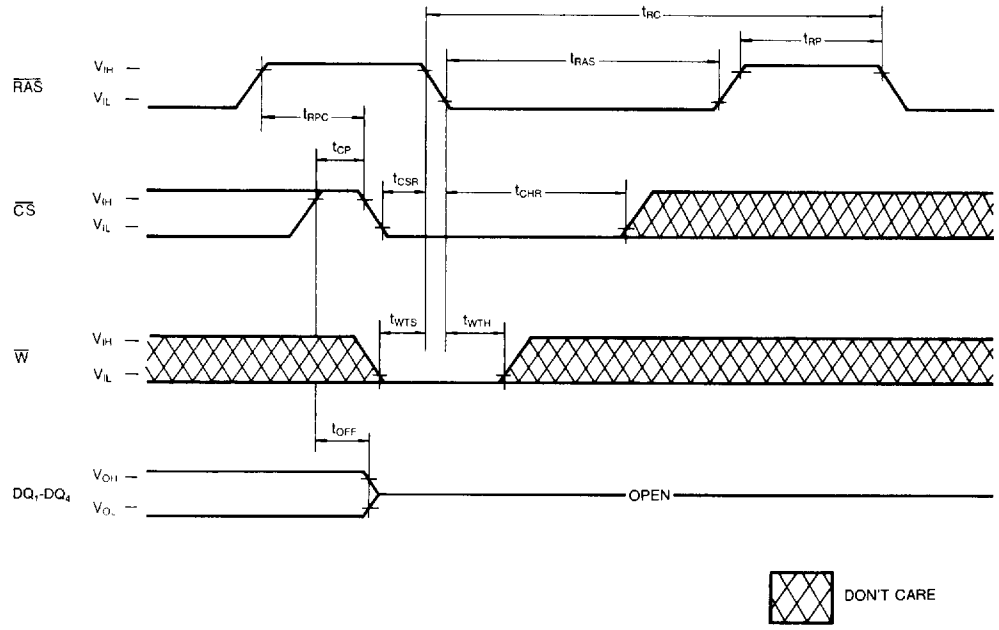
TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$ Address: Don't Care



TEST MODE DESCRIPTION

The KM44C4002 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a 1M x 4 DRAM. $\overline{W}$, $\overline{CS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And $\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" $\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C4002 contains 4,194,304 × 4 memory locations. Twenty-two address bits are required to address a particular 4 bit word in the memory Array. Since the KM44C4002 has only 12 address input pins, time multiplexed addressing is used to input 12 row and 10 column addresses. The The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM44C4002 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C4002 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C4002 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM44C4002 can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between W and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of W or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If W is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD} are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C4002 has a tri-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C4002 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C4002 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C4002 has $\overline{CS}$-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C4002 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C4002 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected to are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

CS-before-RAS Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_{11} are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle. The status of A_{10}, A_{11} is don't care.

Suggested CS-before-RAS Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

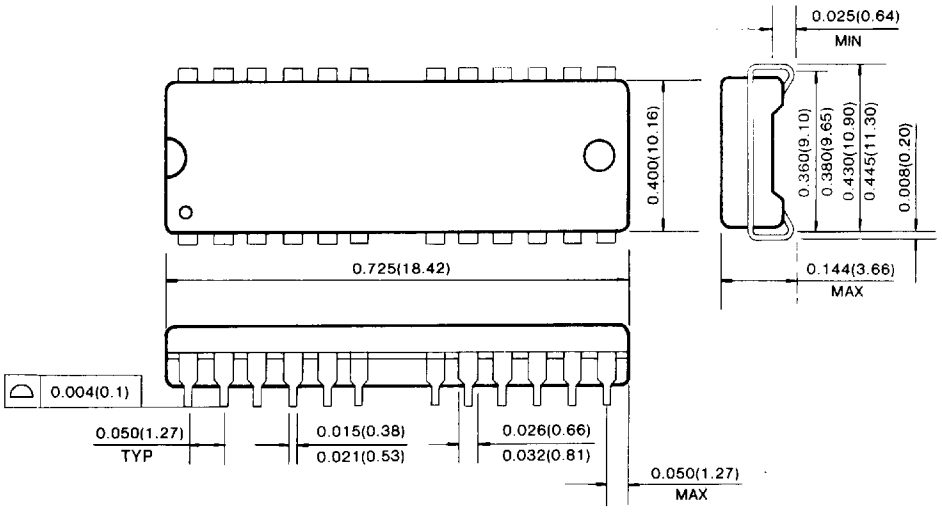
If $\overline{RAS} = V_{SS}$ during power-up, the KM44C4002 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured.

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)