HARRIS

HD-15530/883

T-75-57

June 1989

CMOS Manchester Encoder-Decoder

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Support of MIL-STD-1553
- 1.25 Megabit/Sec Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power .....50mW @ 5 Volts

Description

The Harris HD-15530/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

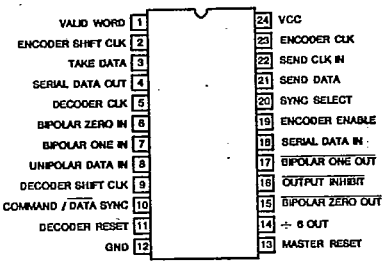
This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

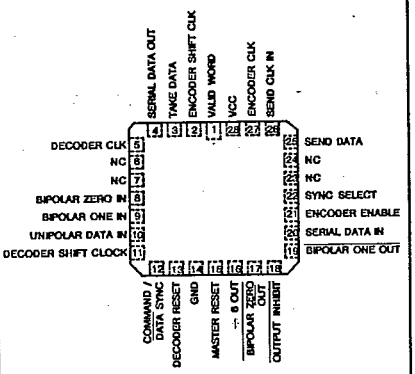
The HD-15530/883 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

Pinouts

HD1-15530/883 (CERAMIC DIP)
TOP VIEW

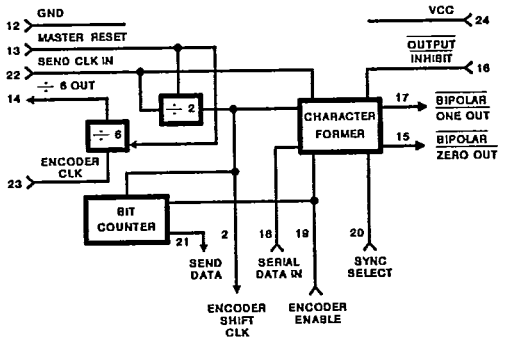


HD4-15530/883 (CERAMIC LCC)
TOP VIEW

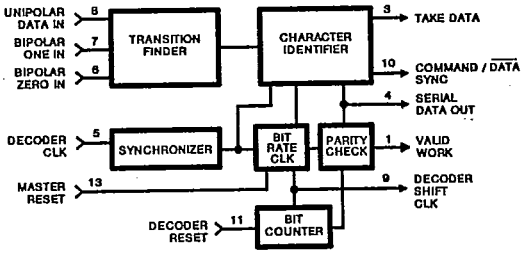


Block Diagrams

ENCODER



DECODER



6 CMOS DATA COMMUNICATIONS

Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transtition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	VCC	Both	VCC is the +5V power supply pin. A 0.1 µF decoupling capacitor from VCC (pin 24) to GROUND (pin 12) is recommended.

I = Input O = Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC+0.3
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	50.4°C/W	11.7°C/W
Ceramic LCC Package	71.1°C/W	16.8°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 992mW
Ceramic LCC Package 703mW
Gate Count ..... 456 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Ambient Operating Temperature Range (T_A) ... -55°C to +125°C
Encoder/Decoder Clock Rise Time ..... 8ns Max
Encoder/Decoder Clock Fall Time ..... 8ns Max
Sync Transition Span (TD2) ..... 18 TDC Typical (Note1)
Short Data Transition Span (TD4) ..... 6 TDC Typical (Note1)
Long Data Transition Span (TD5) ..... 12 TDC Typical (Note1)

TABLE 1. HD-15530/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	GND+0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	VCC-0.5	-	V
Output LOW Voltage	VOL	IOL = 1.8mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3mA (Note 2) VCC = 4.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Input Leakage Current	II	VI = GND or VCC VCC = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V Output Open	1, 2, 3	$-55°C \le T_A \le +125°C$	-	2	mA
Function Test	FT	(Note 3)	7, 8	$-55°C \le T_A \le +125°C$	-	-	-

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. Interchanging of force and sense conditions is permitted.

3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH $\ge$ 1.5V and VOL $\le$ 1.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. HD-15530/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Send Clock Frequency	FESC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	2.5	MHz
Encoder Data Rate	FED	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Master Reset Pulse Width	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	125	ns
Serial Data Setup	TE2	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Serial Data Hold	TE3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Enable Setup	TE4	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	100	-	ns
Sync Setup	TE6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Send Data Delay	TE8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	130	ns
Enable Hold	TE10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Sync Hold	TE11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
DECODER TIMING							
Decoder Clock Frequency	FDC	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	MHz
Decoder Data Rate	FDD	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	1.25	MHz
Decoder Reset Pulse Width	TDR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Decoder Reset Setup Time	TDRS	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Decoder Reset Hold Time	TDRH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	75	-	ns
Master Reset Pulse	TMR	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TDC+10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-20	110	ns
Take Data Delay (ON)	TD7	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns
Valid Word Delay	TD11	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	110	ns

NOTES: 1. TDC = Decoder clock period = 1/FDC

2. A.C. Testing as follows: Input levels: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: 1.5V; Output load: CL = 50pF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HD-15530/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	15	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND	1	$T_A = +25^oC$	-	15	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \leq T_A \leq +25^oC$	-	10	mA

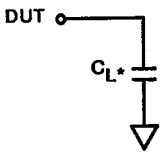
NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit

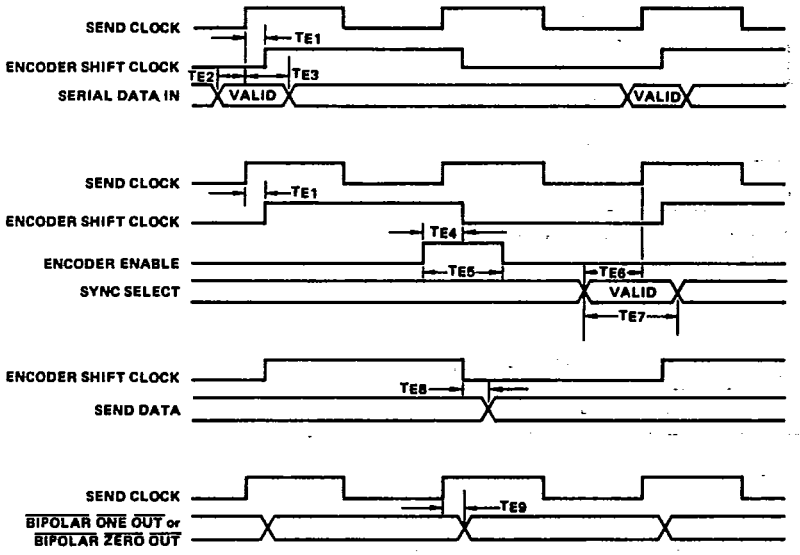


*Includes Stray and Jig Capacitance

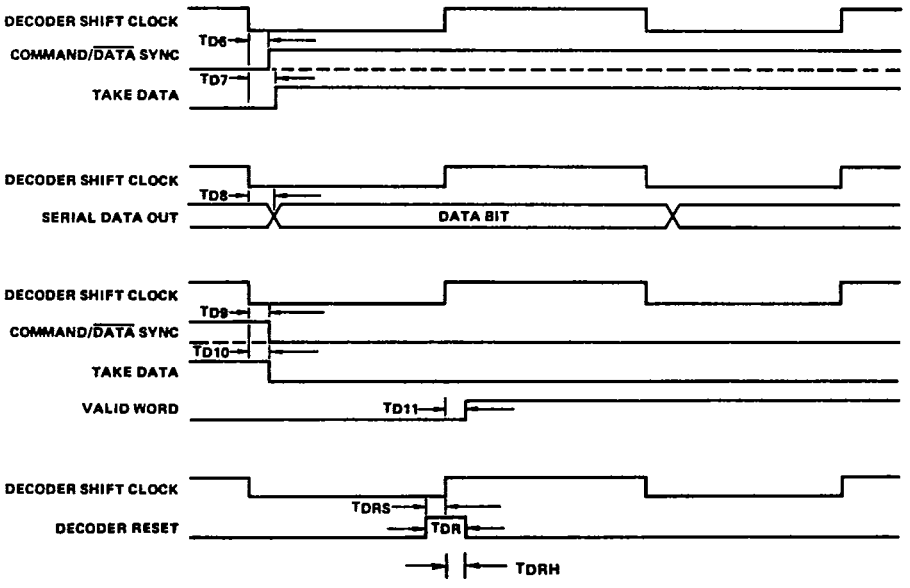
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Timing Waveforms

ENCODER TIMING

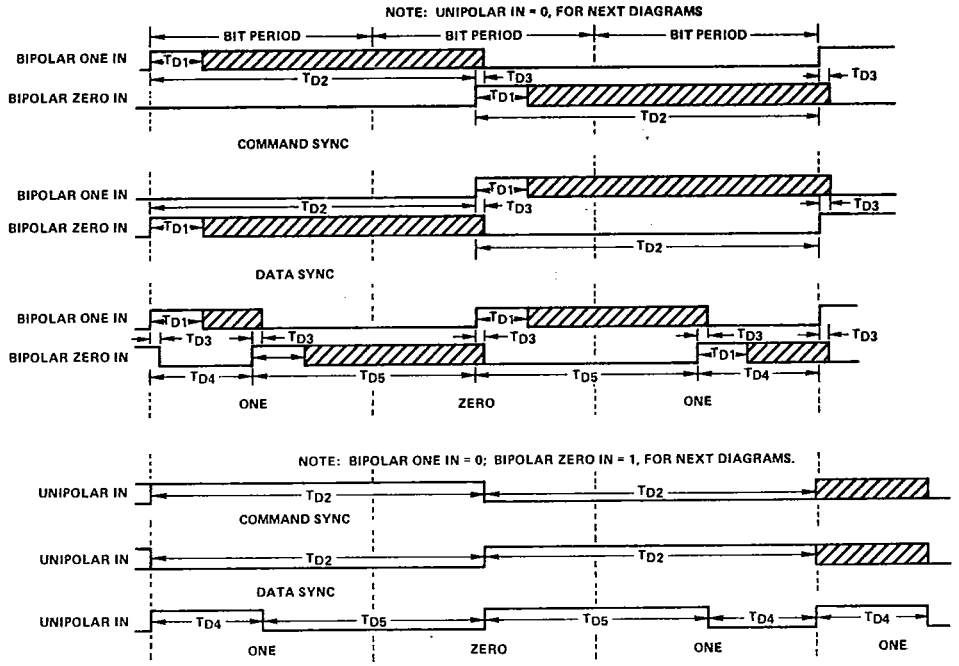


DECODER TIMING



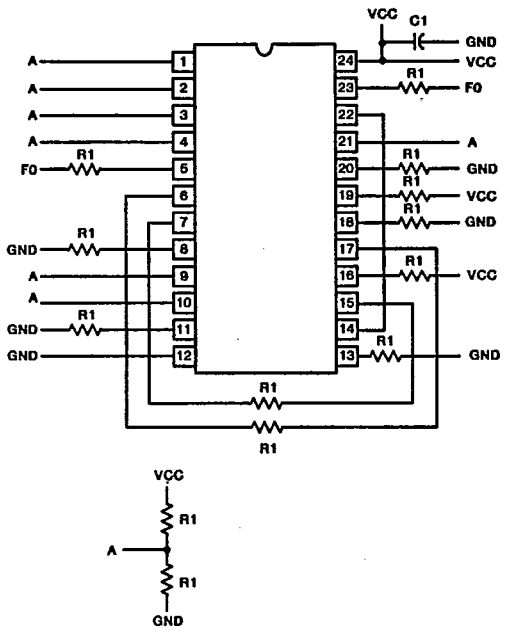
Timing Waveforms (Continued)

DECODER TIMING (Continued)



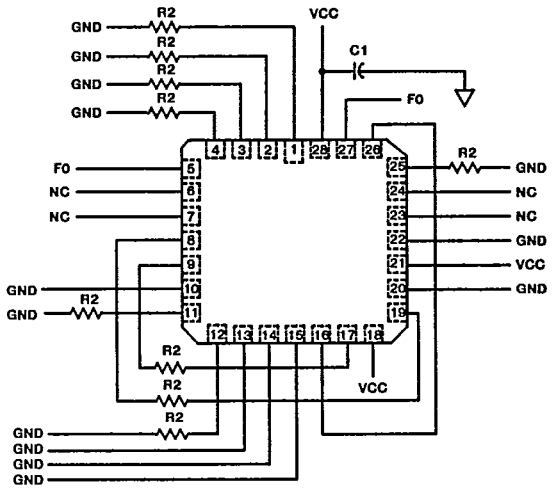
Burn-In Circuits

HD1-15530/883 CERAMIC DIP



NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R1 = 47KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.01μF Min.

HD4-15530/883 CERAMIC LCC



NOTES:
VCC = 5.5V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.4V
R2 = 1.8KΩ ± 5%
F0 = 100KHz ± 10%
C1 = 0.0μF Min.

Metallization Topology

DIE DIMENSIONS:
155 x 195 x 19 ± 1 mils

METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

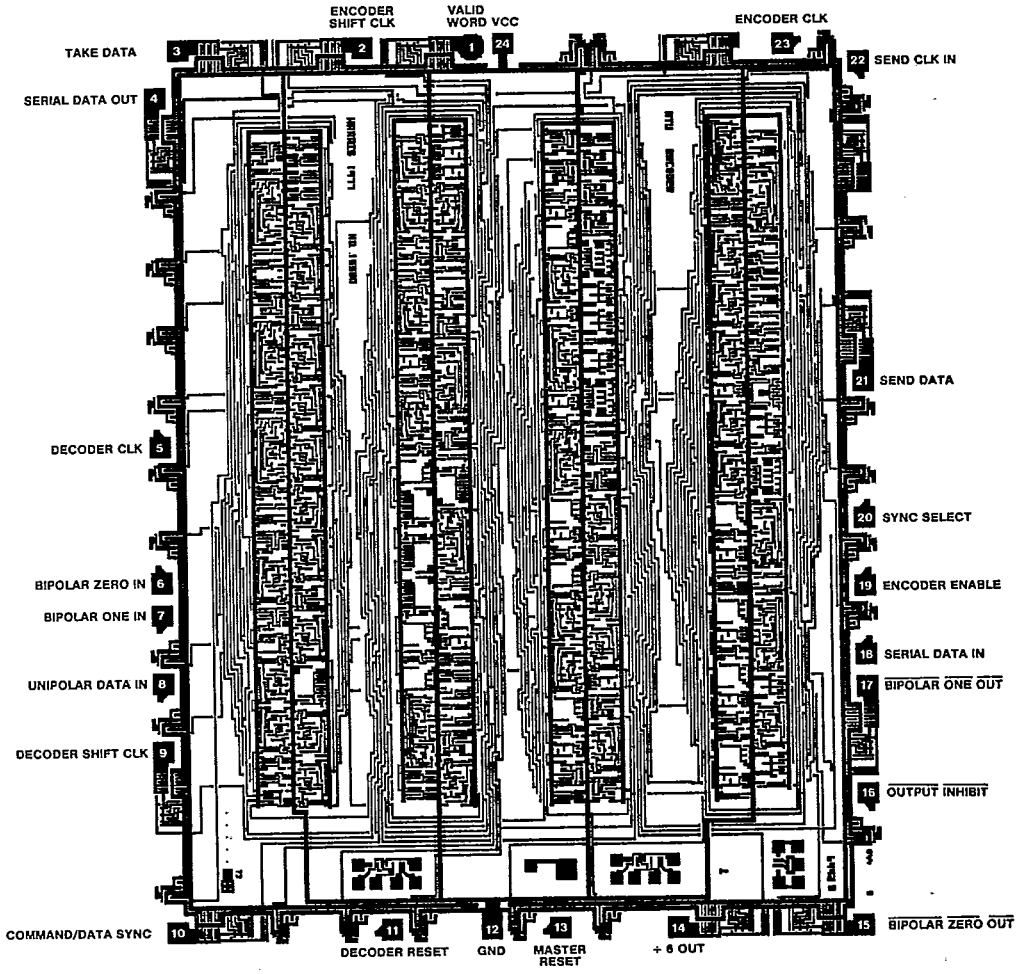
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
$1.8 \times 10^5 A/cm^2$

LEAD TEMPERATURE (10 seconds soldering):
≤275°C

Metallization Mask Layout

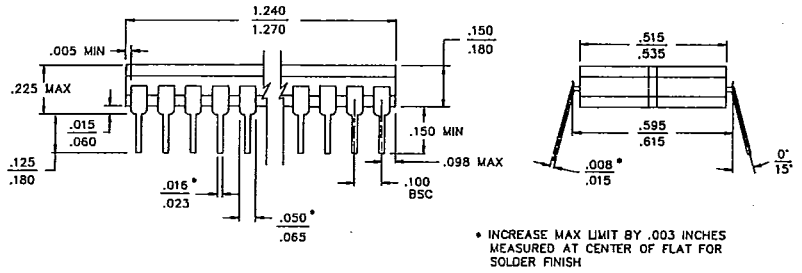
HD-15530/883



6 CMOS DATA COMMUNICATIONS

Packaging†

24 PIN (.600) CERAMIC DIP

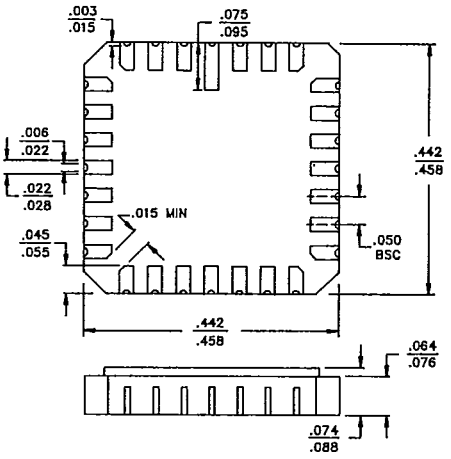


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

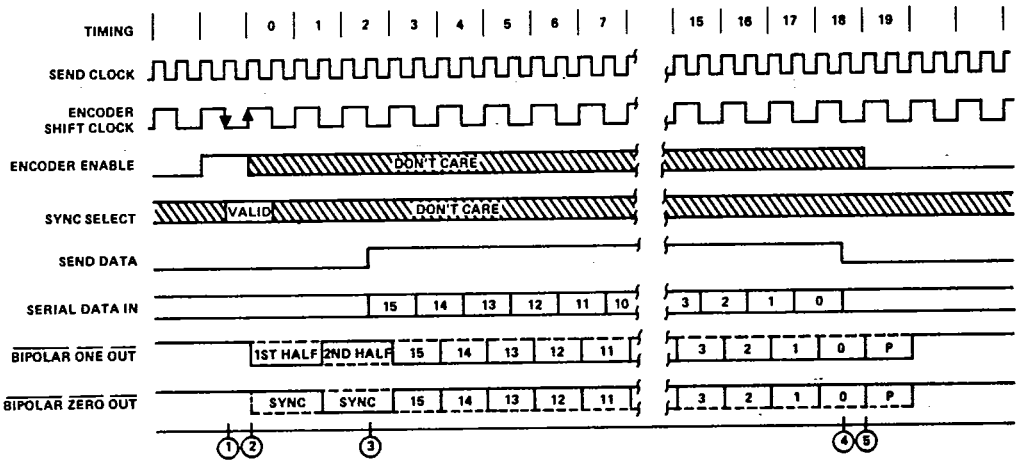
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

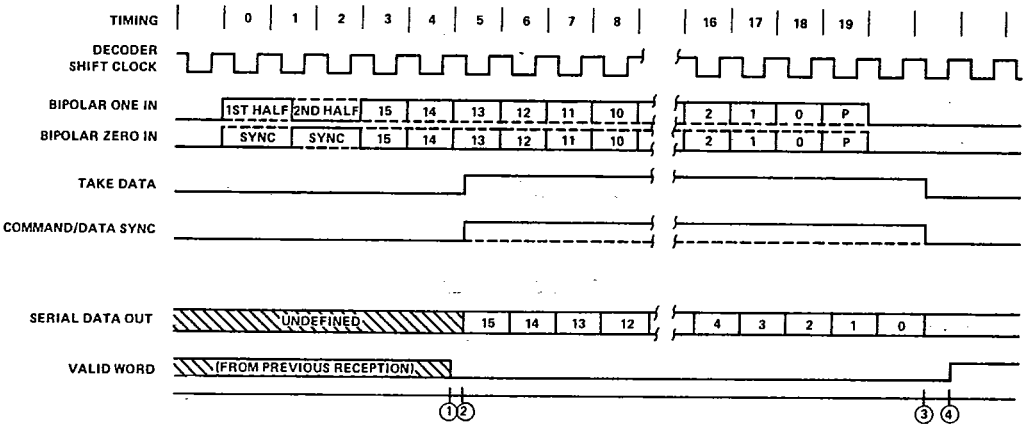
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixten DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

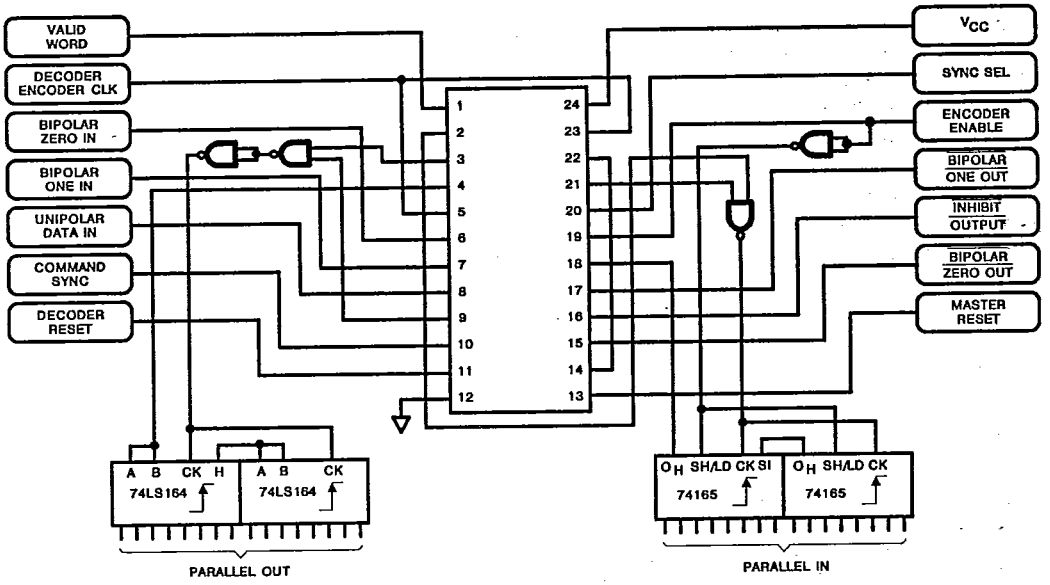
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



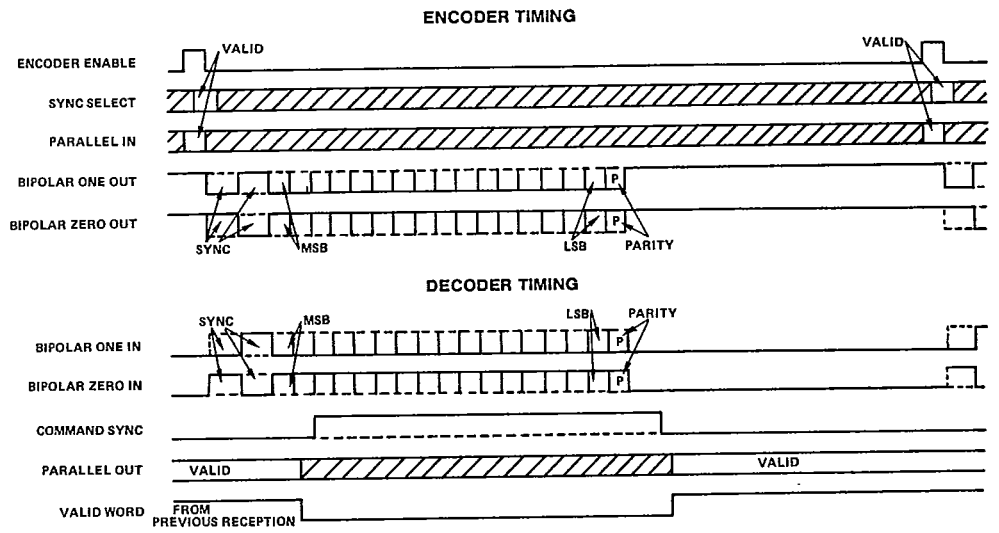
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



6 CMOS DATA COMMUNICATIONS

Packaging Techniques

T-90-20

Harris Semiconductor offers Leadless Chip Carriers (LCC) as a packaging option on various Digital integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is comprised of the cavity and seal ring section of a standard DIP and offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC Packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

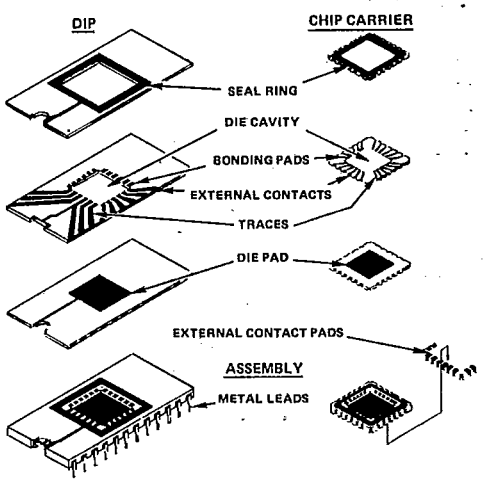


FIGURE 1. EXPLODED VIEW OF CHIP CARRIER AND DIP

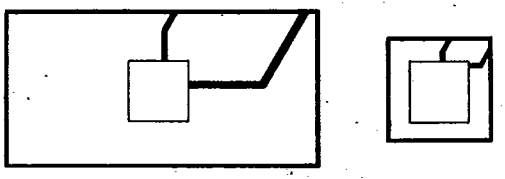
The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

TABLE 1.

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA vs. LCC AREA
18	0.10	0.22	220%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All Units in Square Inches)

The chart indicates a 220% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is a significantly smaller determinant of system performance.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE LCC	LONGEST TRACE SHORTEST TRACE	
		LCC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. ELECTRICAL PERFORMANCE (RESISTANCE AND SPEED)

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal vapor content can be carefully controlled during production.

Harris Semiconductor Leadless Chip Carriers in both Ceramic and Epoxy provide reliable, high density, high performance packaging options for today's systems.

Consult the factory or your Harris sales representative for pricing and availability.