Am8163/Am8167

Dynamic Memory Timing, Refresh and EDC Controllers

DISTINCTIVE CHARACTERISTICS

- Complete CPU to dynamic RAM control interface
- RAS/MSEL/CAS Sequencer to eliminate delay lines
- Complete EDC/data path controls for Word/Byte read or write
- Automatic write-back of corrected data and check bits when single errors are detected on any read cycle
- EDC error flag latches for error logging under software control
- Two timing configurations support a broad range of processors (Z80, Z8000, 8086, 8088, MC68000)

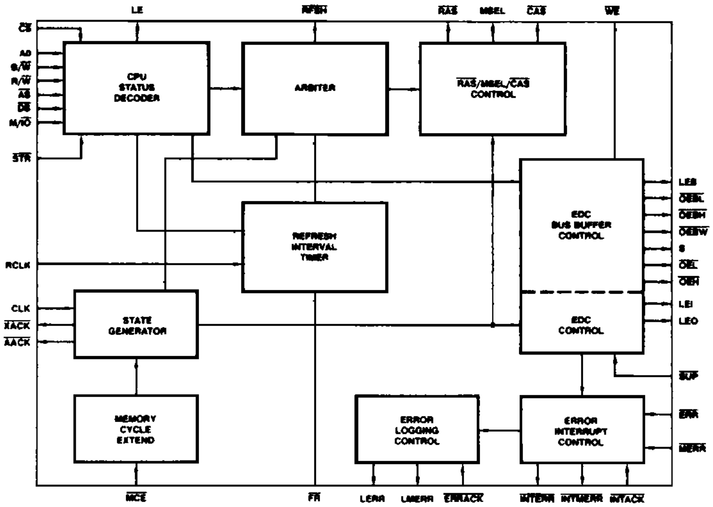
GENERAL DESCRIPTION

The Am8163 and Am8167 are high speed bus interface controllers forming an integral part of the 8086 and AmZ8000* memory support chip set using dynamic MOS RAMs with Error Detection and Correction (EDC). The complete chip set includes the Am8284A and AmZ8127 Clock Generators, the Am2964B Dynamic Memory Controller, the Am2961/62 EDC Bus Buffers, the Am2960 EDC Unit and Am2965/66 RAM Drivers.

The Am8163 and Am8167 provide all of the control interface functions including RAS/Address-MUX/CAS timing (without delay lines), refresh timing, memory request/refresh arbitration and all EDC enables and controls. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction. The Am8163/7 generates bus and operating mode controls for the Am8160 EDC Unit.

The Am8163/7 uses the AmZ8127 oscillator output to generate RAS/Address MUX/CAS timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA memory requests.

BLOCK DIAGRAM



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RELATED PRODUCTS

Part No.	Description	Part No.	Description
Am2960	16-Bit Error Detection and Correction Unit	Am2964B	Dynamic Memory Controller
Am2968	Dynamic Memory Controller	Am2961/62	Error Correction Bus Buffers
Am2969/70	Memory Timing Controllers	Am2965/66	Octal Dynamic Memory Drivers
Am2971	Memory Timing Controller		

*Z8000 is a trademark of Zilog.

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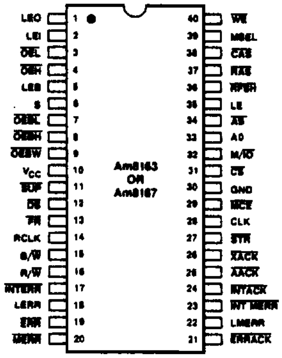
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View



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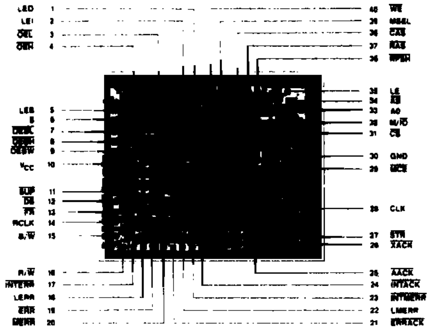
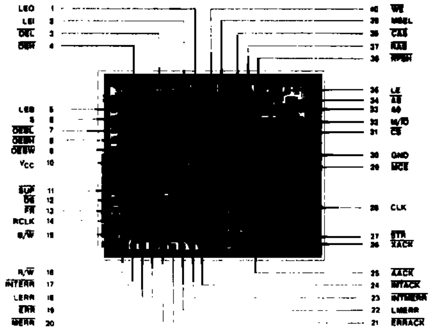
Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT

Am8163



Am8167



DIE SIZE 0.185" x 0.156"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am8163
Am8167 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (−55°C to +125°C)
- **D** — Package
  - D – 40-pin CERDIP (D-40-1)
  - X – Dice
- **Am8163/Am8167** — Device type
  - Dynamic Memory Timing, Refresh, and EDC Controller

Valid Combinations	
Am8163	DC, DCB, DM, DMB XC, XM
Am8167	DC, DCB XC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Bus Control			
28	CLK	I	Clock. The CLK input determines memory cycle timing via the internal state machine from which the control outputs are derived. It is normally 16MHz for the Am8163 and 22MHz for the Am8167. The clock can run at lower frequencies, but not higher, because of other memory timing constraints.
14	RCLK	I	Refresh Clock. This input determines the period of the internal refresh interval ÷ 16 timer and is normally 1MHz. This results in a refresh cycle every 16 microseconds. This provides an internal refresh request to guarantee valid memory data independent of other system operating modes, (memory request, DMA, etc.).
13	FR	I	Force Refresh. FR is used to force a refresh cycle at user-designated times. One example is transparent refresh during I/O operations. The refresh interval timer is reset so the next refresh occurs 16 RCLK cycles later if no other FR pulses occur. FR can be used to minimize collisions with memory requests, thereby reducing the amount of time the CPU waits for refresh.
26	XACK	O	Transfer Acknowledge (open collector). This active LOW output indicates that corrected data has been latched in the Am8160 EDC output latch (as opposed to indicating data is valid on the system bus).
25	AACK	O	Advanced Acknowledge (open collector). This active LOW output indicates that a memory access has started. It can be used to run without wait states when the memory system timing is synchronous with the CPU clock. Multibus or asynchronous configuration should use XACK to control the CPU Ready input.
11	SUP	I	Suppress. This active LOW input inhibits access to the RAM in memory access protected systems. It must be valid before the HIGH-to-LOW transition of DS to suppress a read cycle. It must remain valid until after the cycle (RAS). This is required because SUP simply inhibits WE on a write and inhibits OEBH, OEBL, and OEBW on a read, without halting the internal state generator.
12	DS	I	Data Strobe. This active LOW input is used during read cycles to generate OEBL, OEBH and OEBW. These signals control when data is enabled onto the system data bus.
33	A0	I	Address Bit 0. A0 data input is latched internally on the LOW-to-HIGH transition of AS. It is used during byte operations to designate whether high byte or low byte data is being accessed. A0 = LOW for high byte operations and A0 = HIGH for low byte operations with the AmZ8000 Family CPU's. A0 phasing is opposite for 8086 and inversion can be avoided by interchanging the roles of OEL and OEH (and OEBL and OEBH).
34	AS	I	Address Strobe. The AS input is used to control the A0 latch. When HIGH, A0 data is latched. For non-multiplexed buses, the AS input is tied LOW to make the latch transparent.
15	B/W	I	Byte/Word. This input designates a byte operation if HIGH and a word operation if LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine OEH and OEL.
16	R/W	I	Read/Write. This input indicates a read operation when HIGH and a write operation when LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine the outputs OEH, OEL, OEBH, OEBL, and OEBW.
32	M/IO	I	Memory/Input-Output. This signal serves as an active HIGH chip select for memory operations. It is used in conjunction with CS to determine if STR is valid. It must be HIGH before the LOW-to-HIGH transition of STR if the STR input command is a pulse (AmZ8000). When using a level input (multibus) to start the cycle, M/IO must become valid no later than one clock period after the HIGH-to-LOW transition of STR.
31	CS	I	Chip Select. This active LOW input is one of the enables for the Am8163/7. It must be LOW before the LOW-to-HIGH transition of STR when using a pulse to start a memory access. When using a level input to start the cycle, CS must become valid no later than one clock period after the HIGH-to-LOW transition of STR.
27	STR	I	Start. This active LOW input can be a pulse or a level. It is used to indicate when memory access is requested. It must not extend past the LOW-to-HIGH transition of DS.
Address Control			
35	LE	O	Latch Enable. This output controls the LATCH ENABLE input of the Dynamic Memory Controller. When LE is HIGH, the DMC address input latch is transparent. When LE is LOW, the address is latched. This signal is AS inverted.
36	RFSH	O	Refresh. This active LOW output indicates a refresh operation is to be done. The Dynamic Memory Controller uses this signal to select the refresh address output.
37	RAS	O	Row Address Strobe. This active LOW output strobes the row address into memory. The RAS HIGH-to-LOW transition occurs during t_0 if STR, M/IO and CS have selected a memory cycle. Additionally, RAS will be active one t-state after the RFSH HIGH-to-LOW transition occurs during refresh. The RAS LOW-to-HIGH transition at the end of each cycle starts an internally timed RAS precharge time consisting of three t-states.
39	MSEL	O	Multiplexer Select. This output controls the row and column address selection in the DMC. When MSEL is HIGH, the row address is selected and when LOW, the column address is selected. MSEL is normally HIGH and goes LOW only during memory accesses.
38	CAS	O	Column Address Strobe. This active LOW output strobes the column address into memory. It is generated only during memory accesses.
Error Logging and Control			
19	ERR	I	Error. This active LOW signal from the Am8160 EDC indicates when an error has occurred. The Am8163 samples this input just before the HIGH-to-LOW transition of LEO. Single errors cause an automatic write-back of corrected data.
20	MERR	I	Multiple Error. This active LOW signal from the EDC indicates when a multiple error has occurred. Write back to memory is inhibited if a MULTIPLE ERROR occurs on a read cycle.
18	LERR	O	Latched Error. This active HIGH output is set HIGH as a result of the ERR input becoming active. LERR HIGH indicates an error has occurred. LERR is normally used to control error logging. It is reset when ERRACK goes LOW.
22	LMERR	O	Latched Multiple Error. This active HIGH output is set HIGH as a result of the MERR input. When HIGH, it indicates a multiple error has occurred. It is reset when ERRACK goes low.
17	INTERR	O	Interrupt Error (open collector). This active LOW output is used to interrupt the CPU when an error occurs. This can be used for diagnostics or error logging. INTERR has high output drive capability in order to drive system buses.

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Refer to Page 13-1 for Essential Information on Military Devices

Pin No.	Name	I/O	Description
Error Logging and Control (Cont.)			
23	$\overline{INTMERR}$	O	Interrupt Multiple Error (open collector). This active LOW output is used to interrupt the CPU when a multiple error occurs. This can be used for diagnostics or error logging. $\overline{INTMERR}$ has high output drive capability in order to drive system buses.
24	$\overline{INTACK}$	I	Interrupt Acknowledge. This active LOW input resets both the $\overline{INTERR}$ and $\overline{INTMERR}$ signals.
21	$\overline{ERRACK}$	I	Error Acknowledge. This active LOW input resets the error logging flags, LERR and LMERR. It is only effective when $\overline{INTACK}$ has previously cleared the interrupt flags, $\overline{INTERR}$ and $\overline{INTMERR}$.
EDC Control			
5	LEB	O	Latch Enable Bus. LEB is used to latch corrected data in the external Am8161/2 EDC Data Bus Buffers. By latching data output to the system data bus, the CPU can be operated in a single-step mode. The data latch is required to capture data so the memory can be released for refresh immediately after a read (or write) cycle.
1	LEO	O	Latch Enable Output. LEO is used to latch corrected data in the Am8160 EDC data output latch. Correct data is then available to regenerate correct check bits for the write portion of the read-modify-write cycle. LEO can also control LEY of the Am8161/2 EDC Data Bus Buffers (the input latch from the system data bus). This is required in systems where the CPU removes data from the system data bus before the Am8163/7 has completed a write cycle.
2	LEI	O	Latch Enable Input. LEI is used to control the Am8160 EDC's input latch. It is normally LOW when a memory cycle is not in progress. This prevents transitions on the bus from toggling the EDC logic, thereby reducing power dissipation and system noise. LEI latches the input data so the EDC data bus (Y bus) can be TURNED AROUND WHILE the EDC is correcting the data. Cycle time is reduced by doing these functions in parallel.
6	S	O	Select. This output controls the multiplexer that selects EDC input data. It is normally HIGH to select data from the system bus. When LOW, it selects data from memory. Since all cycles are a read-modify-writes, S switches every cycle. All memory operations take the same number of internal t-states. There is no difference in the length of a cycle on read or write, error or no error.
8	$\overline{OEBH}$	O	Output Enable Bus High. $\overline{OEBH}$ output enables the high byte data onto the system data bus during byte read operations. It is used when interfacing to 8-bit data buses or the Multibus.*
7	$\overline{OEBL}$	O	Output Enable Bus Low. $\overline{OEBL}$ output enables the low byte of data onto the system data bus during Byte Read operations. It is used when interfacing to 8-bit data buses or the Multibus.
9	$\overline{OEBW}$	O	Output Enable Bus Word. $\overline{OEBW}$ output enables data onto the system data bus. It occurs on every read cycle independent of B/$\overline{W}$. It is used for 16-bit systems or Multibus systems.
4	$\overline{OEH}$	O	Output Enable High. $\overline{OEH}$ controls the high byte of the EDC data bus (Y bus). When $\overline{OEH}$ is HIGH, the Am2961/62 are driving the bus. When $\overline{OEH}$ is LOW, the Am8160 EDC is driving the bus. $\overline{OEH}$ is HIGH during word writes and goes low on reads and byte writes.
3	$\overline{OEL}$	O	Output Enable Low. $\overline{OEL}$ controls the low byte of the EDC data bus (Y bus). When HIGH, the Am2961/62's are driving the bus. When LOW, the Am2960 is driving the bus. $\overline{OEL}$ is HIGH during word writes and goes LOW on reads and byte writes.
Other Controls			
40	$\overline{WE}$	O	Write Enable. $\overline{WE}$ controls the memory during a write operation. It is generated during a byte or word write and also during a read if a single error has occurred. $\overline{WE}$ always occurs at the end of the memory cycle. Thus, the RAM is always doing a late write.
29	$\overline{MCE}$	I	Memory Cycle Extend. This input is normally not used and is pulled up internally to produce "normal" timing. When tied LOW it extends the memory cycle (adds 5 t_2 states for Am8163 and adds 4 t_3 states for Am8167). This allows use of slower RAMs. Note that $\overline{MCE}$ affects the refresh cycle as well as the normal cycle. By adding external logic, the user may extend the cycle by 1, 2 or 3 t-states instead. This is done by keeping MCE low until 2, 3, or 4 clocks after MS for the 8163 or 2, 3, or 4 clocks after $\overline{CAS}$ for the 8167.

*Multibus is a registered trademark of Intel Corporation.

FUNCTION TABLES

Am8163/8167

R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEH}$	$\overline{OEL}$
L	L	L	H	H
L	L	H	H	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	L
H	L	H	L	L
H	H	L	L	L
H	H	H	L	L

OEH and OEL are enabled by appropriate sequencer "T" states. (See Timing Diagram)

$\overline{DS}$	R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEBH}$	$\overline{OEBL}$	$\overline{OEBW}$
X	L	L	L	H	H	H
X	L	L	H	H	H	H
X	L	H	L	H	H	H
X	L	H	H	H	H	H
L	H	L	L	L	H	L
L	H	L	H	H	L	L
L	H	H	L	L	H	L
L	H	H	H	H	L	L
H	X	X	X	H	H	H

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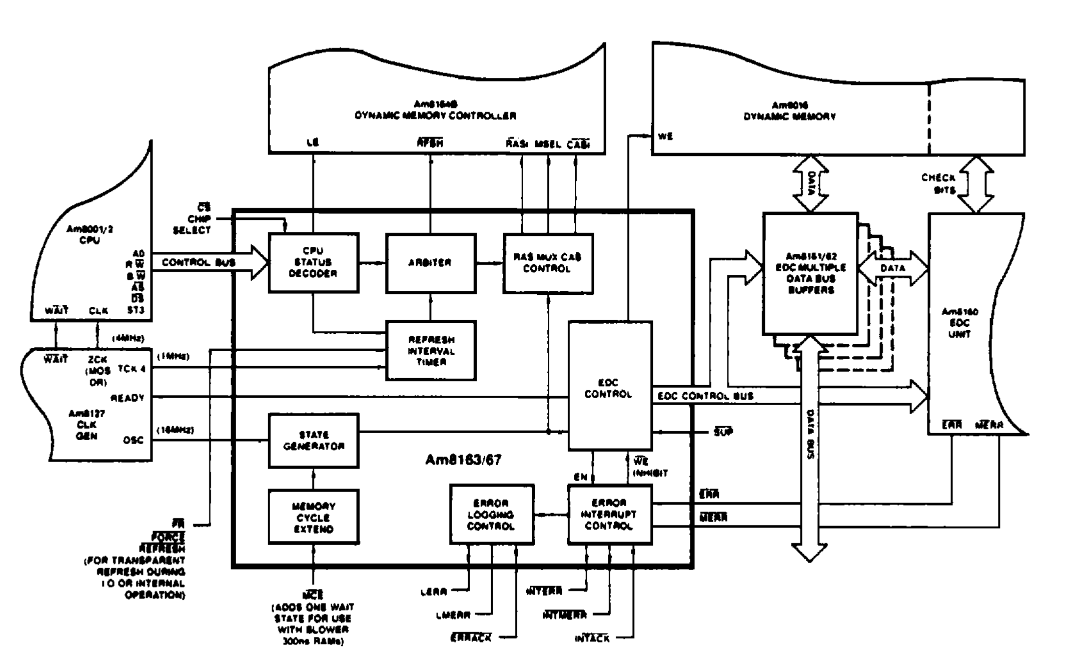
SYSTEM DIAGRAM



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Am8163/67 DETAILED DESCRIPTION

The Am8163/67 provides timing and control for Error Detection and Correction (EDC) using dynamic Random Access Memories (RAM) together with the Am2960 family of EDC devices. See Table 1 to determine which device (Am8163/67) is best suited to which processor.

The Am2960 family provides an optimized, but also flexible solution to the interface between MOS microprocessors and dynamic MOS RAMs.

The Am2960 performs the function of error detection and correction, using a modification of the well-known Hamming Code algorithm.

The Am2961 and Am2962 are bus buffers optimized for operation with the Am2960.

TABLE 1.

Processor		Am8163	Am8167
Z80A		X	
Z80B		X	
Z8000	– 4MHz	X	
	– 6MHz		X
	– 8MHz	X	X
8086	– 5MHz	X	
	– 10MHz		X
8088	– 5MHz	X	
	– 10MHz		X
68000	– 4MHz	X	
	– 6MHz		X
	– 8MHz	X	X
	– 10MHz	X	X
	– 12MHz	X	X

Note: Where X's appear in both columns, either device may be used.

The Am2964B performs address latching and multiplexing for the RAS/CAS sequence. It also contains a refresh counter that can be multiplexed onto the address outputs.

The Am2965 and Am2966 are octal memory address bus drivers, similar and pin-compatible to the popular 74LS240 and 74LS244, but with on-chip resistors that reduce the problem of undershoot on unterminated address lines.

None of the above-mentioned circuits contain timing elements. To achieve the greatest versatility, this function is concentrated in the Am8163.

The Am8163/67 performs two independent functions:

1. It provides timing and control to the Am2964B Dynamic Memory Controller, i.e., the RAS/CAS Refresh address multiplexer.
2. It provides timing and control for the 2960, 2961, or 2962 EDC circuits and interfaces with the microprocessor's interrupt lines and WAIT input.

RAS/CAS and Refresh

The Am8163/67 accepts several control signals from the microprocessor (BYTE/$\overline{\text{WORD}}$, READ/$\overline{\text{WRITE}}$, Address Strobe, Data Strobe, Memory/IO) and a Refresh clock signal from the clock generator.

From these inputs, the Am8163/67 generates control signals for the 2964B RAS/CAS and Refresh multiplexer.

The LE output, when HIGH, makes the 2964B input latches transparent. The HIGH-to-LOW transition of LE latches address information into the 2964B.

The $\overline{\text{RAS}}$ output is activated when the appropriate combination of $\overline{\text{STR}}$, M/$\overline{\text{IO}}$, and $\overline{\text{CS}}$ occur or when a refresh operation is to be performed. MSEL goes LOW one clock period after $\overline{RAS}$ goes LOW.

$\overline{CAS}$ goes LOW a short specified delay after MSEL goes LOW. $\overline{RAS}$, MSEL and $\overline{CAS}$ go HIGH together, eight clock periods after RAS goes LOW. The RAS/CAS timing is thus derived from a high frequency (16MHz clock) without any monostables or delay lines.

The Am8163 and Am8167 are comparable except for the CAS timing sequence.

The Am8163 timing is optimized for operation with a 4MHz microprocessor clock, derived from a 16MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (62ns) and the MS to $\overline{CAS}$ delay is combinatorial, 16ns minimum.

The Am8167 timing is optimized for operation with a 5.5MHz microprocessor clock, derived from a 22MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (47ns) and the MS to $\overline{CAS}$ delay is also one oscillator period (47ns).

Dynamic Memory Refresh

The proper sequencing of refresh operations can be performed either by the CPU (transparent refresh) or by the memory controller (stand-alone refresh).

Transparent refresh, as implemented in the Z80 and Z8000 microprocessors is simple and avoids all memory contention, but it wastes processor time and is not fully compatible with DMA operation.

"Stand-alone" refresh puts the responsibility of refresh address generation and timing on the memory controller. The Am8163/67 performs the necessary timing and access arbitration. The internal refresh interval timer generates a refresh request after every 16 clock pulses on the RCLK refresh clock input (typically 1MHz). When FR (force refresh) goes LOW, the ÷ 16 counter is cleared and the internal refresh request is generated.

Refresh requests and memory requests are synchronized inside the Am8163/67 where the arbiter circuit resolves potential conflicts. If a refresh request occurs after a memory request or during a memory operation, this refresh request will be honored after the memory transaction is complete and the necessary additional precharge time has elapsed.

Similarly, if a memory request occurs after a refresh request or during a refresh operation, this memory request will not be acknowledged until the refresh operation is completed and the necessary precharge time has elapsed. When memory and refresh requests occur simultaneously, the arbiter favors the memory request.

Error Detection/Correction

The other function of the Am8163/67 is timing and control for Error Detection and Correction using the 2960, 2961 or 2962 circuits.

The Am8163/67 drives the ECC Control Bus and receives ERROR or MULTIPLE ERROR inputs from the 2960 Error Detection and Correction Unit. The Am8163/67 also interfaces with the microcomputer interrupt structure and with the error-logging circuitry.

The 2960 can support two methods of error correction: "Correct Only On Error" and "Correct Always".

"Correct Only On Error" relies on the fact that error detection is faster than correction. Data read from the memory is fed directly to the processor. A read error will insert a wait state while the error is being corrected and data is also being written back into the memory. At reasonably low error rates, this scheme achieves the highest possible throughput, but it is incompatible with all present microprocessors, since they sample their WAIT input too early in the cycle.

The Am8163/67 implements the other scheme— "Correct Always"—which is compatible with all modern microprocessors.

This scheme allocates time to insure that corrected data is sent to the CPU. Additionally, the Am8163/67 allows time after each memory read operation, to write the corrected result back into the memory. This write operation, however, is executed only if there was a single error; there is no need to write correct data back, and it is undesirable to write the wrong result of a double error.

the Am8163/67 also provides the proper control signals to allow byte write operation in 16-bit memory systems with Error Correction. The Am8163/67 automatically first performs a word read operation, retains the corrected unused byte in the 2960, and then writes the composite word and check bits into the memory. Outputs LEO, LEI, $\overline{OEH}$, $\overline{OEL}$ and S are responsible for this.

- **$\overline{OEL}$** is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 0 (even address)
- **$\overline{OEH}$** is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 1 (odd address)
- **$\overline{OEBW}$** is pulsed LOW during every read operation
- **$\overline{OEBL}$** is pulsed LOW during every read operation with A0 = 1 (odd address)
- **$\overline{OEBH}$** is pulsed LOW during every read operation with A0 = 0 (even address)

Note: The $\overline{OE}$ and $\overline{OEB}$ outputs interpret A0 in opposite ways. This is consistent with 2960/61 operation.

R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEH}$	$\overline{OEL}$	$\overline{OEBW}$	$\overline{OEBH}$	$\overline{OEBL}$
L	L	L	H	H	H	H	H
L	L	H	H	H	H	H	H
L	H	L	H	L	H	H	H
L	H	H	L	H	H	H	H
H	L	L	L	L	L	L	H
H	L	H	L	L	L	H	L
H	H	L	L	L	L	L	H
H	H	H	L	L	L	H	L

$\overline{OEBW}$, $\overline{OEBH}$, and $\overline{OEBL}$ can be active (LOW) only if: $\overline{DS}$ = $\overline{CS}$ = L AND $\overline{SUP}$ = H

Note that 16-bit memory with EDC must always be initialized with word write operations in order to allow a later byte write operation. (An uninitialized memory would most likely read multiple errors and would then not allow byte write operation.)

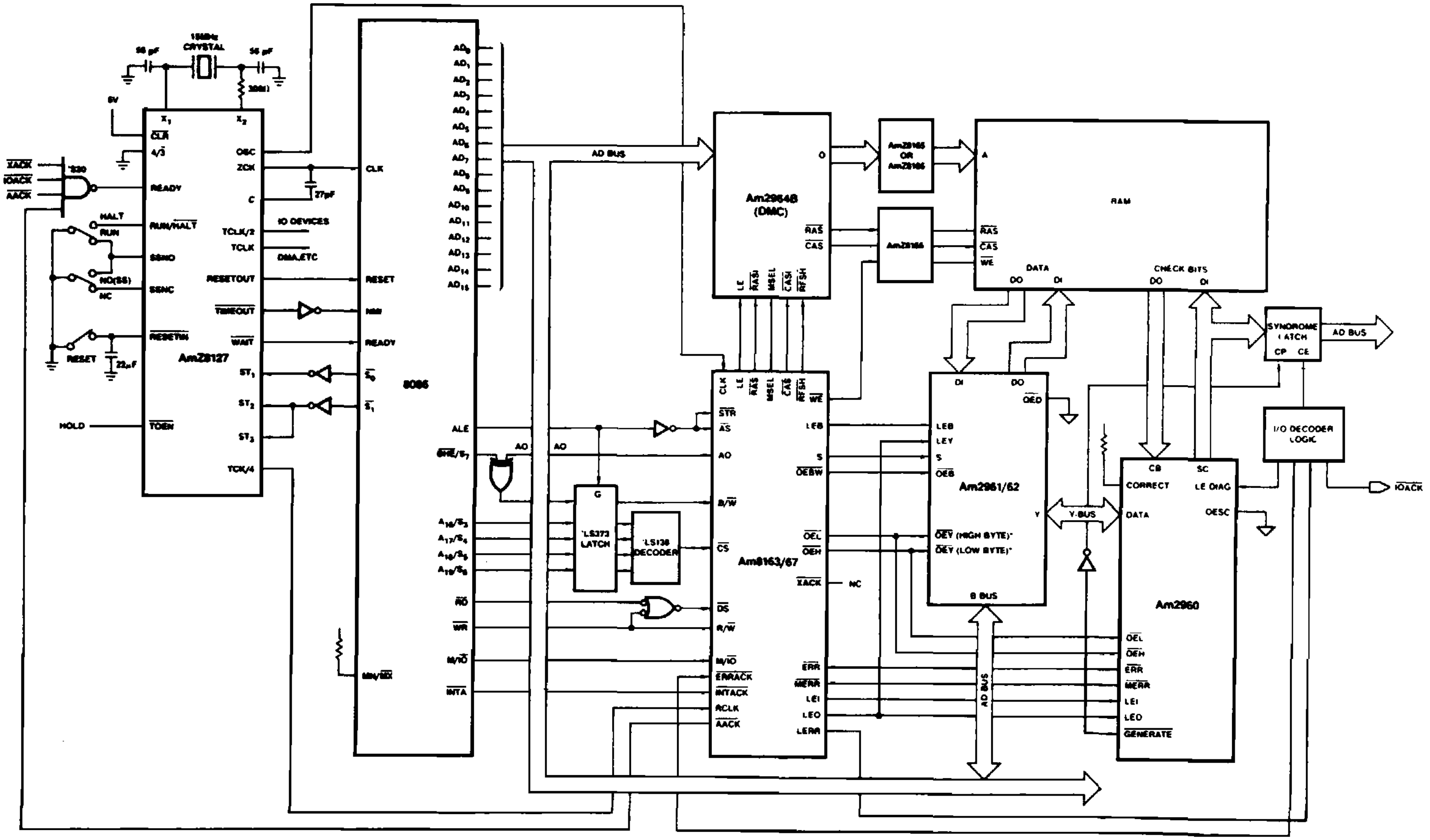
Error Interrupt Control

The Am8163/67 clocks in the $\overline{ERROR}$ and $\overline{MULTIPLE\ ERROR}$ signals coming from the 2960 and stores them in both the Interrupt Logic and in the Error Control Logic.

Interrupt Acknowledge clears both $\overline{INTERR}$ and $\overline{INTMERR}$. The latter must therefore always be the higher priority interrupt.

The Error Logic Control circuit latches up the two bits in the Error Interrupt Control circuit. The LERR and LMERR outputs are cleared by $\overline{ERRACK}$, provided that the interrupts have been cleared first. These signals are normally used to control updating of the syndrome latch or other diagnostic circuitry.

Am8163/67 APPLICATION WITH Am8086 CPU AND Am8127 CLOCK GENERATOR



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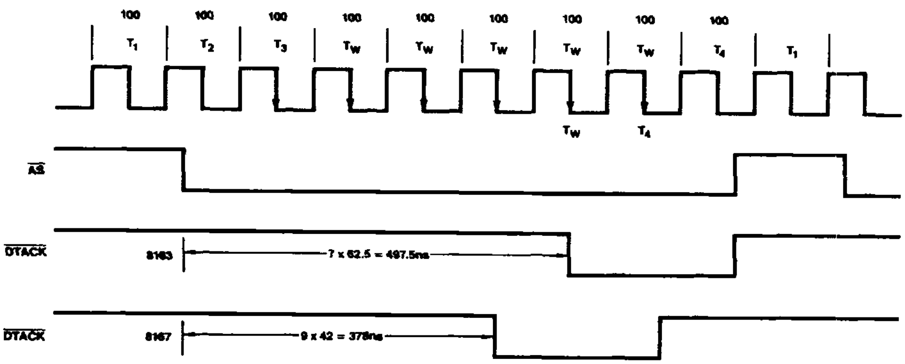
Am8163/67 APPLICATION WITH MC68000



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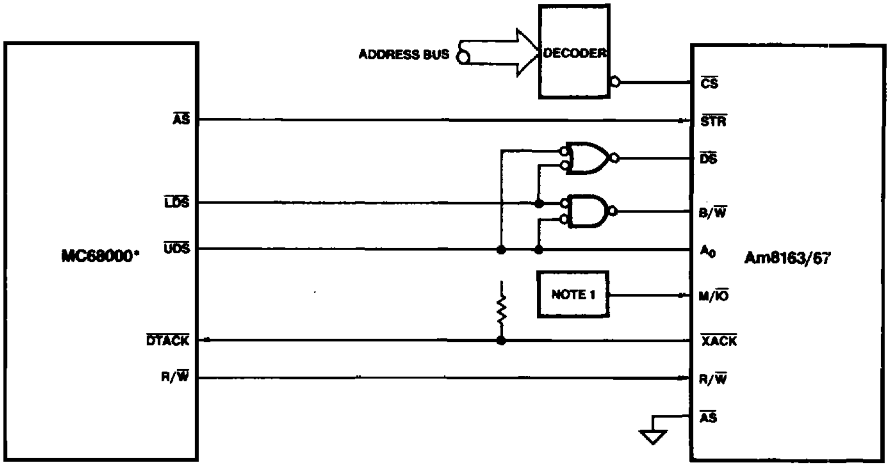

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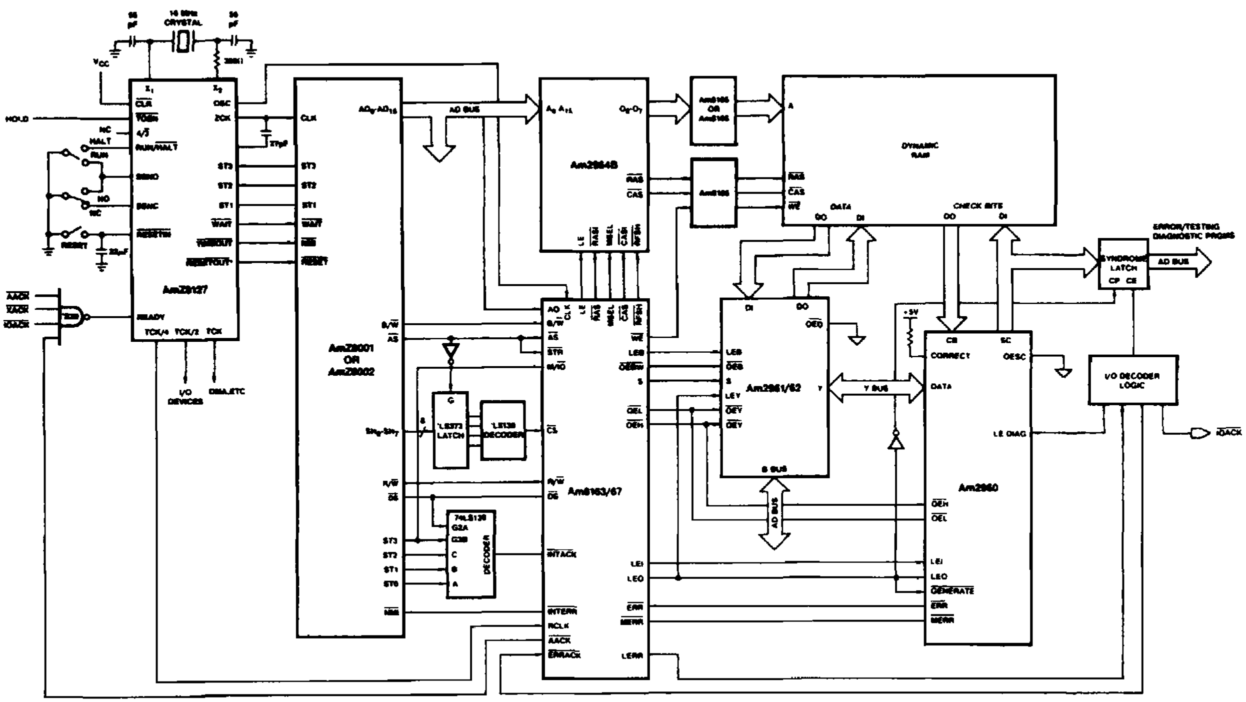
*Timing refers to 10MHz MC68000.

Note 1: M/$\overline{IO}$ may be tied HIGH or connected to an address pin. It may also be connected to an I/O port. The main consideration is not to start the 8163/67 when communicating with the 2960 Diagnostic Latch.

Am8163/67 APPLICATION WITH Am8001/2 AND Am8127 CLOCK GENERATOR



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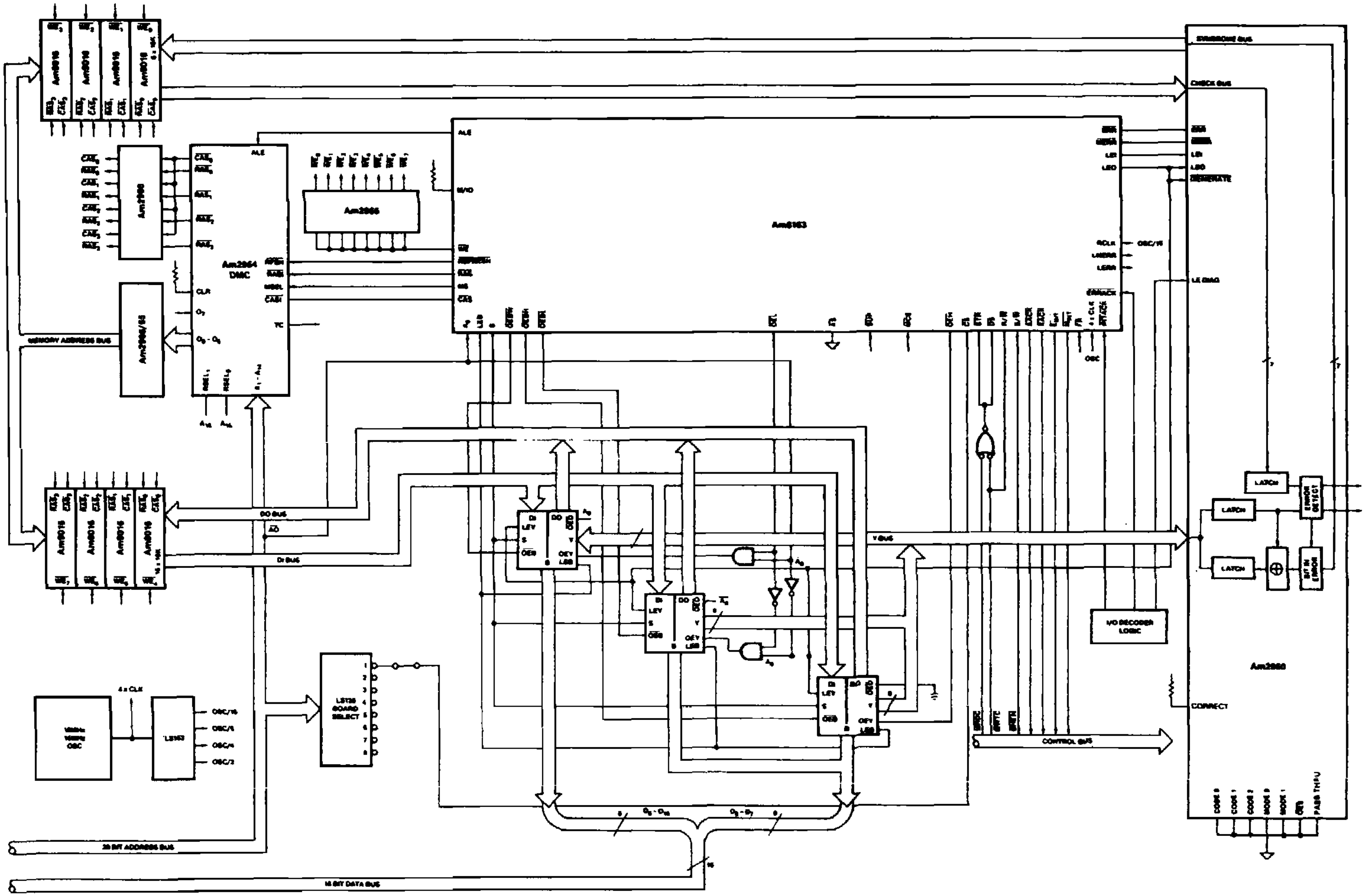
Am8163/67 APPLICATION WITH MULTIBUS*



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*MULTIBUS is a trademark of Intel.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential
  Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs For
  High Output State .... −0.5V to V_{CC} Max
DC Input Voltage .... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current .... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature .... 0°C to +70°C
  Supply Voltage .... +4.75V to +5.25V
Military (M) Devices
  Temperature .... −55°C to +125°C
  Supply Voltage .... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

(Group A, Subgroups 1, 2 and 3)

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Output(s): All except open collectors	MIL, I_{OH} = −1.0mA	2.4			Volts
				COM'L, I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Output(s): LERR, LMERR	I_{OL} = 8mA			0.50	Volts
			$\overline{CAS}$, $\overline{RAS}$, $\overline{OEBH}$, $\overline{OEBL}$	I_{OL} = 12mA			0.50	
			$\overline{OEH}$, $\overline{OEL}$, $\overline{OEBW}$, $\overline{RFSH}$	I_{OL} = 12mA			0.50	
			LEO, LEI, $\overline{WE}$	I_{OL} = 12mA			0.50	
			LEB, LE, S, MSEL	I_{OL} = 12mA			0.50	
			$\overline{INTMERR}$, $\overline{INTERR}$	I_{OL} = 16mA			0.50	
			$\overline{XACK}$, $\overline{AACK}$	I_{OL} = 32mA			0.50	
V_{IH}	Guaranteed Input Logical HIGH Voltage		Input(s): All		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage		Input(s): All	MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN	Input(s): All	I_{IN} = −18mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	Input(s): A0, M/$\overline{IO}$, RCLK, B/$\overline{W}$, R/$\overline{W}$, $\overline{STR}$, $\overline{AS}$, $\overline{INTACK}$	MIL			−0.42	mA
				COM'L			−0.40	
			$\overline{FR}$, $\overline{SUP}$, $\overline{ERRACK}$, $\overline{MCE}$	MIL			−0.82	mA
				COM'L			−0.8	
			$\overline{CLK}$, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			−2.1	mA
				COM'L			−2.0	
			$\overline{MERR}$	MIL			−2.6	mA
				COM'L			−2.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	Input(s): $\overline{MERR}$	MIL			100	μA
				COM'L			70	
			CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			70	μA
				COM'L			50	
			$\overline{FR}$, $\overline{SUP}$, $\overline{MCE}$, $\overline{ERRACK}$				40	μA
			M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$				20	
			$\overline{AS}$, $\overline{STR}$, $\overline{INTACK}$				20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	Input(s): CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$, $\overline{MERR}$				1.0	mA
			$\overline{SUP}$, $\overline{MCE}$, $\overline{FR}$				1.0	
		V_{CC} = MAX, V_{IN} = 7.0V	M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$, $\overline{INTACK}$, $\overline{AS}$, $\overline{STR}$				0.10	
			$\overline{ERRACK}$				0.20	
I_{OH}	Output HIGH Current	V_{CC} = MIN, V_{OH} = 5.5V	Output(s): $\overline{INTMERR}$, $\overline{INTERR}$				100	μA
			$\overline{XACK}$, $\overline{AACK}$				150	

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
I_{OS}	Output Short Circuit Current	V_{CC} = MAX +0.5V V_O = 0.5V	**Output(s):** All (Note 3)		−15		−85	mA
I_{CC}	Power Supply Current	8163	25°C, 5V			280		mA
			0 to 70°C	COM'L			365	mA
		8167	0 to 70°C	COM'L			390	mA
		8163	−55 to +125°C	MIL			385	mA
		8167	−55 to +125°C	MIL			420	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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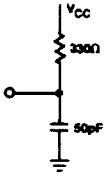
Refer to Page 13-1 for Essential Information on Military Devices

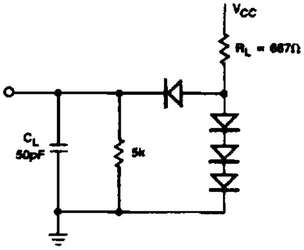
SWITCHING TEST CIRCUIT

$\overline{INTERR}$, $\overline{INT\ MERR}$



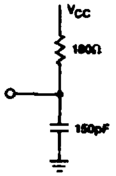
TC000640

OTHER OUTPUTS



TC000650

$\overline{XACT}$, $\overline{AACK}$



TC000660

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters		Description	Min	Typ	Max	Units
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	0	−4		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	0	−10		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	5	2		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 5	tp + 2		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		12	18	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		12	18	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1	0		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	9	5		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20	9		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	2	0		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp	−(tp + 10)		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10	6		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		36	41	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		26	34	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		17	22	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		21	26	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay – 8163	18	23		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay – 8167		17	22	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8163		34	43	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8167		21	26	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		30	35	ns
20	t_{PHL}	CLK to $\overline{AACK}$↓ Propagation Delay		33	41	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		17	22	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		20	26	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		16	22	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay – 8163	1.0	3.0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay – 8167		21	26	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		20	26	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		17	22	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	15	20		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8163	4.5	7.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8167		24	30	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		24	30	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0	−1.5		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0	−10		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		15	21	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		21	26	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		21	26	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		24	30	ns
36	t_{PHL}	CLK to $\overline{XACK}$↑ Propagation Delay		29	36	ns
37	t_{PLH}	DS↑ to $\overline{XACK}$↑ Propagation Delay		24	30	ns
38	t_{PHL}	DS↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		13	18	ns

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Parameters		Description	Min	Typ	Max	Units
39	t_{PLH}	DS↑ to $\overline{OEBL}$↑, $\overline{OEBH}$↑, $\overline{OEBW}$↑ Propagation Delay		13	18	ns
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	1.5	0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	6.5	4		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		19	24	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		23	30	ns
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		30	39	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		9	14	ns
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20	9		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20	9		ns
48	t_S	$\overline{SUP}$↓ to $\overline{DS}$↓ Setup Time	0	−5		ns
49	t_H	$\overline{WE}$↑ to SUP↑ Hold Time	0	−10		ns
50	t_{PHL}	CLK to $\overline{RFSH}$↓ Propagation Delay		16	21	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8163		4tp		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8167		5tp		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8163		3tp		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8167		4tp		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8163		7tp		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8167		9tp		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8163		6tp		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8167		8tp		
55a	f_{OSC}	CLK Frequency – 8163			16	MHz
55b	f_{OSC}	CLK Frequency – 8167			22	MHz

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Refer to Page 13-1 for Essential Information on Military Devices

Switching Characteristics (Cont.)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters		Description	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	5		5		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	5		5		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	9		9		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 10		tp + 10		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		22		22	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		22		22	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1.5		1.5		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	10		10		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20		20		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	5		5		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp		−tp		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10		12		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		45		45	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		40		40	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		25		25	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		30		30	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay – 8163	16		16		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay – 8167		25		25	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8163		50		50	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay – 8167		30		30	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		40		40	ns
20	t_{PHL}	CLK to $\overline{AACK}$↓ Propagation Delay		46		46	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		25		25	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		30		30	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		25		25	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay – 8163	0		0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay – 8167		30		30	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		30		30	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		25		25	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	10		10		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay – 8163	4.0		4.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ – 8167		35		35	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		35		35	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0		1.0		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0		0		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		25		25	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		30		30	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		30		30	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		35		35	ns
36	t_{PHL}	CLK to $\overline{XACK}$↑ Propagation Delay		40		41	ns
37	t_{PLH}	$\overline{DS}$↑ to $\overline{XACK}$↑ Propagation Delay		35		35	ns
38	t_{PHL}	DS↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		22		22	ns
39	t_{PLH}	$\overline{DS}$↑ to $\overline{OEBL}$↑, $\overline{OEBH}$↑, $\overline{OEBW}$↑ Propagation Delay		22		22	ns
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	2.0		3.0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	8.0		8.0		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		28		28	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		38		38	ns
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		46		46	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		20		20	ns

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters		Description	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20		20		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20		20		ns
48	t_S	$\overline{SUP}$↓ to $\overline{DS}$↓ Setup Time	5		5		ns
49	t_H	$\overline{WE}$↑ to SUP↑ Hold Time	5		5		ns
50	t_{PHL}	CLK to $\overline{RFSH}$↓ Propagation Delay		25		25	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) - 8163	4tp-3ns		4tp-3ns		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) - 8167	5tp-3ns		5tp-3ns		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) - 8163	3tp-3ns		3tp-3ns		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) - 8167	4tp-3ns		4tp-3ns		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) - 8163	7tp-3ns		7tp-3ns		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) - 8167	9tp-3ns		9tp-3ns		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) - 8163	6tp-3ns		6tp-3ns		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) - 8167	8tp-3ns		8tp-3ns		
55a	t_{OSC}	CLK Frequency - 8163		16		16	MHz
55b	t_{OSC}	CLK Frequency - 8167		22		22	MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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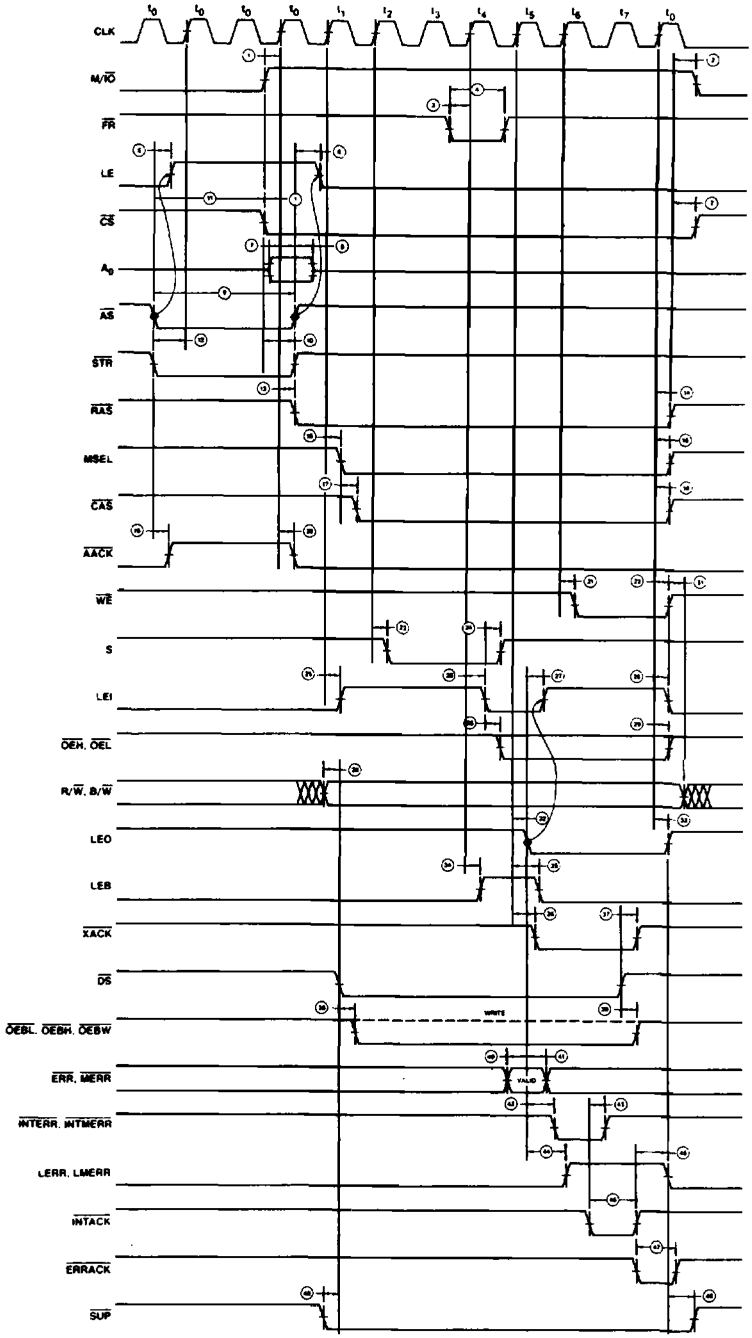
Refer to Page 13-1 for Essential Information on Military Devices

TIMING WAVEFORMS

Am8163 TIMING



WF001820

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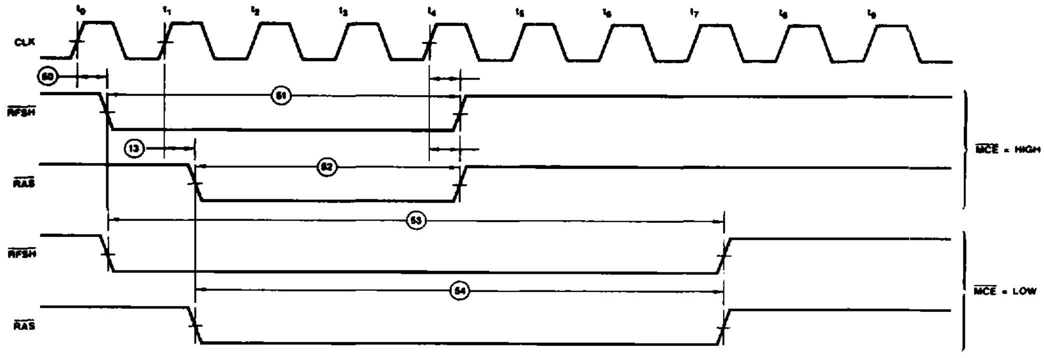
TIMING WAVEFORMS (Cont.)

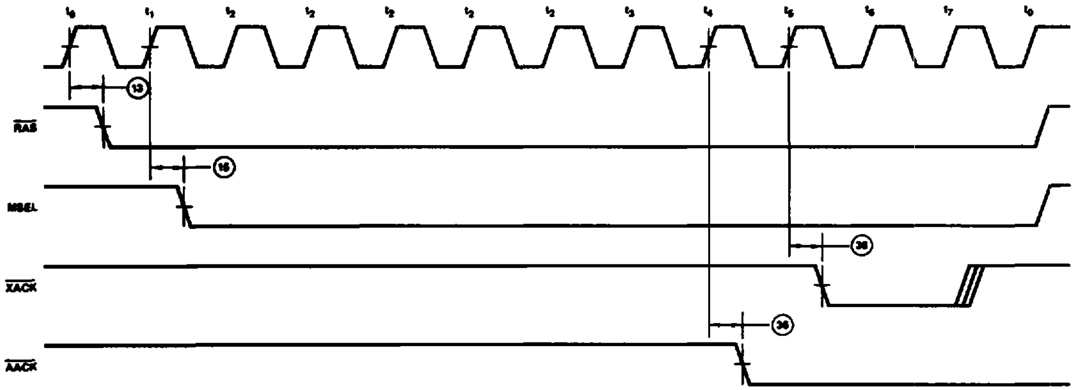
Am8163 REFRESH TIMING



WF002500

Am8163 MEMORY CYCLE EXTEND TIMING

($\overline{MCE}$ = LOW)



WF001800

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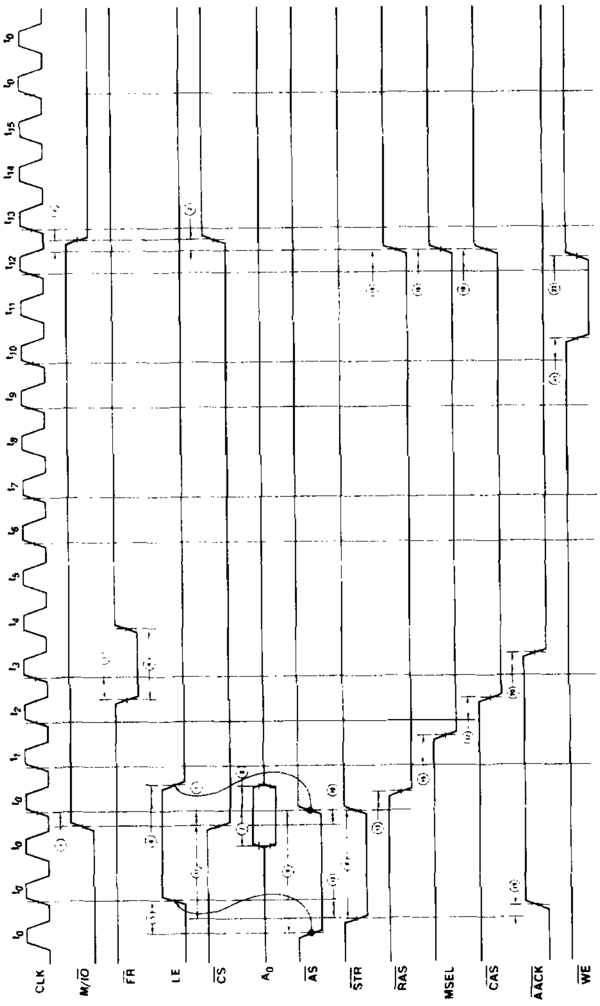
Refer to Page 13-1 for Essential Information on Military Devices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t13
t14
t15

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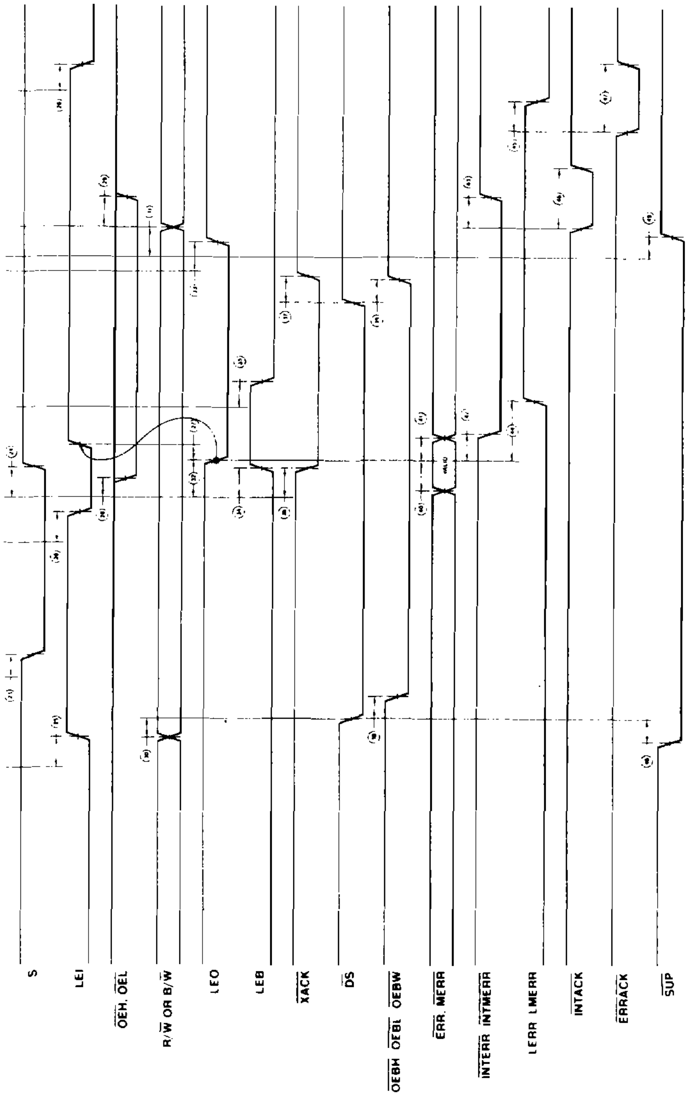
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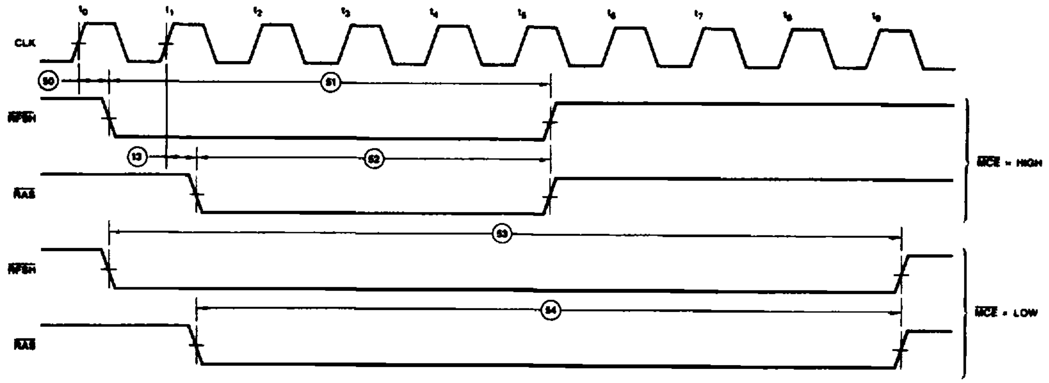
LEO
LEB
XACK
DS
OEBH OEBL OEBW
ERR, MERR
INTERR INTMERR
LERR LMERR
INTACK
ERRACK
SUP

01553A

TIMING WAVEFORMS (Cont.)

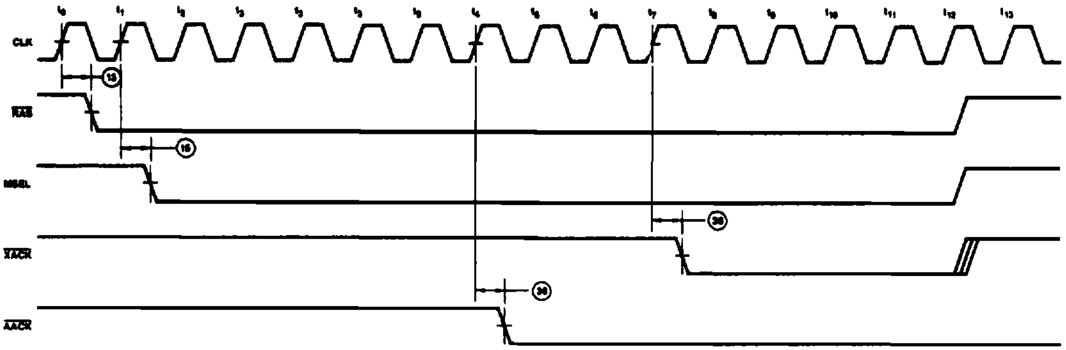
Am8167 REFRESH TIMING



WF001780

Am8167 MEMORY CYCLE EXTEND TIMING

(MCE = LOW)



WF001790