

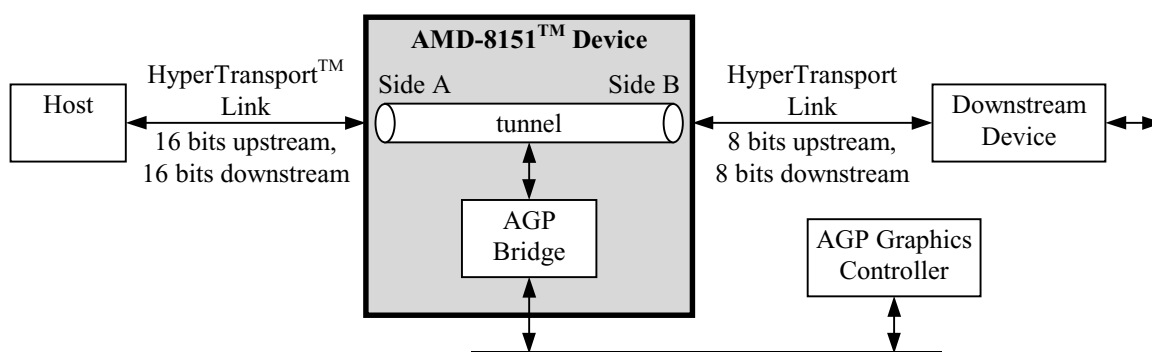
## AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Data Sheet

### 1 Overview

The AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel (referred to as *the IC* in this document) is a HyperTransport™ technology (referred to as *link* in this document) tunnel developed by AMD that provides an AGP 3.0 compliant (8x transfer rate) bridge.

#### 1.1 Device Features

- HyperTransport technology tunnel with side A and side B.
  - Side A is 16 bits (input and output); side B is 8 bits.
  - Either side may connect to the host or to a downstream HyperTransport technology compliant device.
  - Each side supports HyperTransport technology-defined reduced bit widths: 8-bit, 4-bit, and 2-bit.
  - Side A supports transfer rates of 1600, 1200, 800, and 400 mega-transfers per second. Side B supports transfer rates of 800 and 400 mega-transfers per second.
  - Maximum bandwidth is 6.4 gigabytes per second across side A (half upstream and half downstream) and 1.6 gigabytes per second across side B.
  - Independent transfer rate and bit width selection for each side.
  - Link disconnect protocol supported.
- AGP 8x bridge.
  - Compliance with AGP 3.0 specification signaling, supporting 4x and 8x transfer rates.
  - Compliance with AGP 2.0 specification 1.5-volt signaling, supporting 1x, 2x, and 4x data-transfer modes.
  - Supports up to 32 outstanding requests.
- 31 x 31 millimeter, 564-ball BGA package.
- 1.5 volt AGP signaling; some 3.3 volt IO; 1.2 volt link signaling; 1.8 volt core.



**Figure 1: System block diagram.**

© 2004 Advanced Micro Devices, Inc.

All rights reserved. The contents of this document are provided in connection with Advanced Micro Devices, Inc. ("AMD") products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD's Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right. AMD's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD's product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

## Trademarks

AMD, the AMD Arrow logo, and combinations thereof, and AMD-8151 are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

# Table of Contents

|           |                                             |           |
|-----------|---------------------------------------------|-----------|
| <b>1</b>  | <b>Overview</b>                             | <b>1</b>  |
| 1.1       | Device Features                             | 1         |
| <b>2</b>  | <b>Ordering Information</b>                 | <b>6</b>  |
| <b>3</b>  | <b>Signal Descriptions</b>                  | <b>6</b>  |
| 3.1       | Terminology                                 | 6         |
| 3.2       | Tunnel Link Signals                         | 7         |
| 3.3       | AGP Signals                                 | 8         |
| 3.4       | Test and Miscellaneous Signals              | 10        |
| 3.5       | Power and Ground                            | 10        |
| 3.5.1     | Power Plane Sequencing                      | 10        |
| <b>4</b>  | <b>Functional Operation</b>                 | <b>11</b> |
| 4.1       | Overview                                    | 11        |
| 4.2       | Reset And Initialization                    | 11        |
| 4.3       | Clocking                                    | 11        |
| 4.3.1     | Clock Gating                                | 11        |
| 4.4       | Tunnel Links                                | 12        |
| 4.4.1     | Link PHY                                    | 12        |
| 4.5       | AGP                                         | 12        |
| 4.5.1     | Tags, UnitIDs, And Ordering                 | 12        |
| 4.5.2     | Various Behaviors                           | 13        |
| 4.5.2.1   | AGP Compensation And Calibration Cycles     | 13        |
| <b>5</b>  | <b>Registers</b>                            | <b>14</b> |
| 5.1       | Register Overview                           | 14        |
| 5.1.1     | Configuration Space                         | 14        |
| 5.1.2     | Register Naming and Description Conventions | 14        |
| 5.2       | AGP Device Configuration Registers          | 15        |
| 5.3       | AGP Bridge Configuration Registers          | 30        |
| <b>6</b>  | <b>Electrical Data</b>                      | <b>34</b> |
| 6.1       | Absolute Ratings                            | 34        |
| 6.2       | Operating Ranges                            | 34        |
| 6.3       | DC Characteristics                          | 35        |
| 6.4       | AC Characteristics                          | 37        |
| <b>7</b>  | <b>Ball Designations</b>                    | <b>39</b> |
| <b>8</b>  | <b>Package Specification</b>                | <b>42</b> |
| <b>9</b>  | <b>Test</b>                                 | <b>43</b> |
| 9.1       | High Impedance Mode                         | 43        |
| 9.2       | NAND Tree Mode                              | 43        |
| <b>10</b> | <b>Appendix</b>                             | <b>45</b> |
| 10.1      | Revision History                            | 45        |

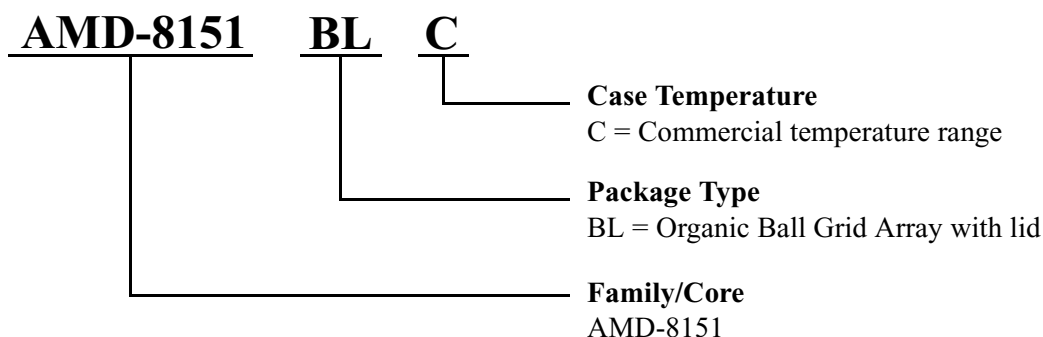
# List of Figures

|           |                                 |    |
|-----------|---------------------------------|----|
| Figure 1: | System block diagram.....       | 1  |
| Figure 2: | Configuration space. ....       | 14 |
| Figure 3: | Ball designations. ....         | 39 |
| Figure 4: | Package mechanical drawing..... | 42 |
| Figure 5: | NAND tree. ....                 | 43 |

# List of Tables

|           |                                                                                  |    |
|-----------|----------------------------------------------------------------------------------|----|
| Table 1:  | IO signal types. ....                                                            | 6  |
| Table 2:  | Translation from AGP requests to link requests. ....                             | 13 |
| Table 3:  | Configuration spaces. ....                                                       | 15 |
| Table 4:  | Memory mapped address spaces. ....                                               | 15 |
| Table 5:  | Register attributes. ....                                                        | 15 |
| Table 6:  | Absolute maximum ratings. ....                                                   | 34 |
| Table 7:  | Operating ranges. ....                                                           | 34 |
| Table 8:  | Current and power consumption. ....                                              | 35 |
| Table 9:  | DC characteristics for signals on the VDD33 power plane. ....                    | 35 |
| Table 10: | DC characteristics for signals on the VDD15 power plane, AGP 2.0 signaling. .... | 36 |
| Table 11: | DC characteristics for signals on the VDD15 power plane, AGP 3.0 signaling. .... | 36 |
| Table 12: | AC data for clocks. ....                                                         | 37 |
| Table 13: | AC data for common clock operation of AGP signals. ....                          | 37 |
| Table 14: | AC data for clock-forwarded operation of AGP signals. ....                       | 38 |
| Table 15: | Signal BGA positions. ....                                                       | 40 |
| Table 16: | Power and ground BGA positions. ....                                             | 41 |
| Table 17: | Test modes. ....                                                                 | 43 |

## 2 Ordering Information



## 3 Signal Descriptions

### 3.1 Terminology

See section 5.1.2 for a description of the register naming convention used in this document. See the AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Design Guide for additional information.

Signals with a # suffix are active low.

Signals described in this chapter utilize the following IO cell types:

| Name   | Notes                                                                                                                    |
|--------|--------------------------------------------------------------------------------------------------------------------------|
| Input  | Input signal only.                                                                                                       |
| Output | Output signal only. This includes outputs that are capable of being in the high-impedance state.                         |
| OD     | Open drain output. These signals are driven low and expected to be pulled high by external circuitry.                    |
| IO     | Input or output signal.                                                                                                  |
| IOD    | Input or open-drain output.                                                                                              |
| Analog | Analog signal.                                                                                                           |
| w/PU   | With pullup. The signal includes a pullup resistor to the signal's power plane. The resistor value is nominally 8K ohms. |

**Table 1: IO signal types.**

The following provides definitions and reference data about each of the IC's pins. "During Reset" provides the state of the pin while RESET# is asserted. "After Reset" provides the state of the pin immediately after RESET# is deasserted. "Func." means that the pin is functional and operating per its defined function.

### 3.2 Tunnel Link Signals

The following are signals associated with the HyperTransport™ links. [B, A] in the signal names below refer to the A and B sides of the tunnel. [P, N] are the positive and negative sides of differential pairs.

| Pin name and description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | IO cell type                  | Power plane*                     | During reset        | After reset |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|----------------------------------|---------------------|-------------|-------------------------------|--------------------|-----|-------------------------------|-----------------|--------|-----------------------|----------------------------------|--------|---------|--|--|
| <b>LDTCOMP[3:0]</b> . Link compensation pins for both sides of the tunnel. These are designed to be connected through resistors as follows:<br><br><table><tr><th>Bit</th><th>Function</th><th>External Connection</th></tr><tr><td>[0]</td><td>Positive receive compensation</td><td>Resistor to VDD12B</td></tr><tr><td>[1]</td><td>Negative receive compensation</td><td>Resistor to VSS</td></tr><tr><td>[3, 2]</td><td>Transmit compensation</td><td>Resistor from bit [2] to bit [3]</td></tr></table><br>These resistors are used by the compensation circuit. The output of this circuit is combined with DevA:0x[E8, E4, E0] to determine compensation values that are passed to the link PHYs. | Bit                           | Function                         | External Connection | [0]         | Positive receive compensation | Resistor to VDD12B | [1] | Negative receive compensation | Resistor to VSS | [3, 2] | Transmit compensation | Resistor from bit [2] to bit [3] | Analog | VDD-12B |  |  |
| Bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Function                      | External Connection              |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| [0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Positive receive compensation | Resistor to VDD12B               |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Negative receive compensation | Resistor to VSS                  |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| [3, 2]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Transmit compensation         | Resistor from bit [2] to bit [3] |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LRACAD_[P, N][15:0]; LRBCAD_[P, N][7:0]</b> . Receive link command-address-data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Link input                    | VDD12                            |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LRACLK[1, 0]_[P, N]; LRBCLK0_[P, N]</b> . Receive link clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Link input                    | VDD12                            |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LR[B, A]CTL_[P, N]</b> . Receive link control signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Link input                    | VDD12                            |                     |             |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LTACAD_[P, N][15:0]; LTBCAD_[P, N][7:0]</b> . Transmit link command-address-data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Link output                   | VDD12                            | Diff High**         | Func.       |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LTACLK[1, 0]_[P, N]; LTBCLK0_[P, N]</b> . Transmit link clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Link output                   | VDD12                            | Func.               | Func.       |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |
| <b>LT[B, A]CTL_[P, N]</b> . Transmit link control signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Link output                   | VDD12                            | Diff Low**          | Func.       |                               |                    |     |                               |                 |        |                       |                                  |        |         |  |  |

\* The signals connected to the A side of the tunnel are powered by VDD12A and the signals connected to the B side of the tunnel are powered by VDD12B.

\*\* Diff High and Diff Low for these link pins specifies differential high and low; e.g., Diff High specifies that the \_P signal is high and the \_N signal is low.

If one of the sides of the tunnel is not used on a platform then the unconnected link should be treated as follows, for every 10 differential pairs: connect all of the \_P differential inputs together and through a resistor to VSS; connect all the \_N differential inputs together and through a resistor to VDD12; leave the differential outputs unconnected. If there are unused link signals on an active link (because the IC is connected to a device with a reduced bit width), then the unused differential inputs and outputs should also be connected in this way.

### 3.3 AGP Signals

In the table below, “Term” indicates the standard AGP 3.0 termination impedance to ground; “PU” indicates a weak pullup resistor; “PD” indicates a weak pulldown resistor.

| Pin name and description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | IO cell type                   | Power plane                  | AGP 3.0 Signaling          |             | AGP 2.0 Signaling           |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|------------------------------|----------------------------|-------------|-----------------------------|------------------|---------|------------------------------|-------------------|--------|-------------------------------|-----------------|---------|--------------------------------|-------------------|--------|-------|--|--|--|--|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                |                              | During reset               | After reset | During reset                | After reset      |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_ADSTB0_[P, N].</b> AGP differential strobe for A_AD[15:0] and A_CBE_L[1:0]. When AGP 3.0 signaling is enabled, A_ADSTB0_P is the first strobe and A_ADSTB0_N is the second strobe.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | IO                             | VDD15                        | Term                       | Term        | _P: PU<br>_N: PD            | _P: PU<br>_N: PD |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_ADSTB1_[P, N].</b> AGP differential strobe for AD[31:16], A_CBE_L[3:2], and A_DBI[H,L]. When AGP 3.0 signaling is enabled, A_ADSTB1_P is the first strobe and A_ADSTB1_N is the second strobe.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | IO                             | VDD15                        | Term                       | Term        | _P: PU<br>_N: PD            | _P: PU<br>_N: PD |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_AD[31:0].</b> AGP address-data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | IO                             | VDD15                        | Term                       | Term        | PU                          | Low              |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_CBE_L[3:0].</b> AGP command-byte enable bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO                             | VDD15                        | Term                       | Term        | PU                          | Low              |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_CAL[D, S] and A_CAL[D, S]#.</b> Compensation pins for matching impedance of system board AGP traces. See DevA:0x[54, 50] for more information. These are designed to be connected through resistors as follows:<br><br><table><tr><td><u>Signal</u></td><td><u>Compensation Function</u></td><td><u>External Connection</u></td></tr><tr><td>A_CALD</td><td>Rising edge of data signals</td><td>Resistor to VSS</td></tr><tr><td>A_CALD#</td><td>Falling edge of data signals</td><td>Resistor to VDD15</td></tr><tr><td>A_CALS</td><td>Rising edge of strobe signals</td><td>Resistor to VSS</td></tr><tr><td>A_CALS#</td><td>Falling edge of strobe signals</td><td>Resistor to VDD15</td></tr></table><br>These resistors are used by the compensation circuit. The output of this circuit is combined with DevA:0x[54, 50] to determine compensation values that are passed to the link PHYs. | <u>Signal</u>                  | <u>Compensation Function</u> | <u>External Connection</u> | A_CALD      | Rising edge of data signals | Resistor to VSS  | A_CALD# | Falling edge of data signals | Resistor to VDD15 | A_CALS | Rising edge of strobe signals | Resistor to VSS | A_CALS# | Falling edge of strobe signals | Resistor to VDD15 | Analog | VDD15 |  |  |  |  |
| <u>Signal</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <u>Compensation Function</u>   | <u>External Connection</u>   |                            |             |                             |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| A_CALD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Rising edge of data signals    | Resistor to VSS              |                            |             |                             |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| A_CALD#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Falling edge of data signals   | Resistor to VDD15            |                            |             |                             |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| A_CALS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Rising edge of strobe signals  | Resistor to VSS              |                            |             |                             |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| A_CALS#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Falling edge of strobe signals | Resistor to VDD15            |                            |             |                             |                  |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_DBI[H, L].</b> Data bus inversion [high, low]. When DevA:0xA4[AGP3MD]=1, A_DBIL applies to AD[15:0]; A_DBIH applies to AD[31:16]. 1=AD signals are inverted. 0=A_AD signals are not inverted. The IC uses these signals in determining the polarity of the A_AD signals when they are inputs. These may also be enabled to support the DBI function of the IC output signals by DevA:0x40[DBIEN]. Both A_DBIH and A_DBIL are strobed with A_ADSTB1_[P, N].<br><br>When DevA:0xA4[AGP3MD]=0: A_DBIL is pulled low with the AGP termination value and not used by the IC; A_DBIH is pulled up to VDD15 through a weak resistor and becomes the AGP 2.0 PIPE# input signal.                                                                                                                                                                                                                          | IO                             | VDD15                        | Term                       | Term        | PU                          | PU               |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_DEVSEL#.</b> AGP device select.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | IO                             | VDD15                        | Term                       | Term        | PU                          | PU               |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_FRAME#.</b> AGP frame signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO                             | VDD15                        | Term                       | Term        | PU                          | PU               |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |
| <b>A_GC8XDET#.</b> 0=Specifies that the graphics device supports AGP 3.0 signaling. The state of this signal is latched on the rising edge of A_RESET# before being passed to internal logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Input w/PU                     | VDD15                        | PU                         | PU          | PU                          | PU               |         |                              |                   |        |                               |                 |         |                                |                   |        |       |  |  |  |  |

| Pin name and description                                                                                                                                                                                                                                                                                      | IO cell type  | Power plane | AGP 3.0 Signaling |             | AGP 2.0 Signaling |                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------|-------------------|-------------|-------------------|------------------|
|                                                                                                                                                                                                                                                                                                               |               |             | During reset      | After reset | During reset      | After reset      |
| <b>A_GNT#.</b> AGP master grant signal.                                                                                                                                                                                                                                                                       | Output        | VDD15       | Term              | Low         | PU                | High             |
| <b>A_IRDY#.</b> AGP master ready signal.                                                                                                                                                                                                                                                                      | IO            | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_MB8XDET#.</b> This pin is controlled by DevA:0x40[8XDIS]. It is designed to be connected to the AGP connector to indicate support for AGP 3.0 signaling.                                                                                                                                                 | Output        | VDD15       | Low               | Low         | Low               | Low              |
| <b>A_PAR.</b> AGP parity signal.                                                                                                                                                                                                                                                                              | IO            | VDD15       | Term              | Term        | PU                | Low              |
| <b>A_PCLK.</b> 66 MHz AGP clock.                                                                                                                                                                                                                                                                              | Output        | VDD33       | Func.             | Func.       | Func.             | Func.            |
| <b>A_PLLCLKO.</b> PLL clock output. See section 4.3 for details.                                                                                                                                                                                                                                              | Output        | VDD33       | Func.             | Func.       | Func.             | Func.            |
| <b>A_PLLCLKI.</b> PLL clock input. See section 4.3 for details.                                                                                                                                                                                                                                               | Input         | VDD33       |                   |             |                   |                  |
| <b>A_REFCG.</b> AGP signal reference output.                                                                                                                                                                                                                                                                  | Analog output | VDD15       |                   |             |                   |                  |
| <b>A_REFGC.</b> AGP signal reference input.                                                                                                                                                                                                                                                                   | Analog input  | VDD15       |                   |             |                   |                  |
| <b>A_REQ#.</b> AGP master request signal.                                                                                                                                                                                                                                                                     | Input         | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_RESET#.</b> AGP bus reset signal. This is asserted whenever RESET# is asserted or when programmed by DevB:0x3C[SBRST]. Assertion of this pin does not reset any logic internal to the IC.                                                                                                                | Output        | VDD33       | Low               | High        | Low               | High             |
| <b>A_RBF#.</b> AGP read buffer full signal.                                                                                                                                                                                                                                                                   | Input         | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_SBSTB_[P, N].</b> AGP differential side band address strobe. In AGP 3.0 signaling mode, A_SBSTB_P is the first strobe and A_SBSTB_N is the second strobe.                                                                                                                                                | Input         | VDD15       | Term              | Term        | _P: PU<br>_N: PD  | _P: PU<br>_N: PD |
| <b>A_SBA[7:0].</b> AGP side band address signals.                                                                                                                                                                                                                                                             | Input         | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_ST[2:0].</b> AGP status signals.                                                                                                                                                                                                                                                                         | Output        | VDD15       | Term              | Low         | PU                | Low              |
| <b>A_STOP#.</b> AGP target abort signal.                                                                                                                                                                                                                                                                      | IO            | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_TRDY#.</b> AGP target ready signal.                                                                                                                                                                                                                                                                      | IO            | VDD15       | Term              | Term        | PU                | PU               |
| <b>A_TYPEDET#.</b> AGP IO voltage level type detect. 0=1.5 volts; 1=3.3 volts (not supported by the IC). The state of this pin is provided in DevA:0x40[TYPEDET]. This pin is also used for test-mode selection; see section 9. This signal requires an external pullup resistor to VDD33 on the systemboard. | Input         | VDD33       |                   |             |                   |                  |
| <b>A_WBF#.</b> AGP write buffer full signal.                                                                                                                                                                                                                                                                  | Input         | VDD15       | Term              | Term        | PU                | PU               |

The SERR# and PERR# signals are not supported on the AGP bridge.

### 3.4 Test and Miscellaneous Signals

| Pin name and description                                                                                                                                                                                                                                                                                           | IO cell type | Power plane | During reset | After reset |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|--------------|-------------|
| <b>CMPOVR.</b> Link automatic compensation override. 0=Link automatic compensation is enabled. 1=The compensation values stored in DevA:0x[E0, E4, E8] control the compensation circuit. The state of this signal determines the default value for DevA:0x[E0, E4, E8][ACTL and BCTL] at the rising edge of PWROK. | Input        | VDD33       |              |             |
| <b>FREE[7:1].</b> These should be left unconnected.                                                                                                                                                                                                                                                                |              |             |              |             |
| <b>LDTSTOP#.</b> Link disconnect control signal. This pin is also used for test-mode selection; see section 9.                                                                                                                                                                                                     | Input        | VDD33       |              |             |
| <b>NC[1:0].</b> These should be left unconnected.                                                                                                                                                                                                                                                                  |              |             |              |             |
| <b>PWROK.</b> Power OK. 1=All power planes are valid. The rising edge of this signal is deglitched; it is not observed internally until it is high for more than 6 consecutive REFCLK cycles. See section 4.2 for more details about this signal.                                                                  | Input        | VDD33       |              |             |
| <b>REFCLK.</b> 66 MHz reference clock. This is required to be operational and valid for a minimum of 200 microseconds prior to the rising edge of PWROK and always while PWROK is high.                                                                                                                            | Input        | VDD33       |              |             |
| <b>RESET#.</b> Reset input. See section 4.2 for details.                                                                                                                                                                                                                                                           | Input        | VDD33       |              |             |
| <b>STRAPL[19:13, 11:0].</b> Strapping option to be tied low. These pins should be tied to ground. STRAPL0 is used for test-mode selection; see section 9.                                                                                                                                                          | IO           | VDD15       | 3-State      | 3-State     |
| <b>STRAPL[22:20].</b> Strapping option to be tied low. These pins should be tied to ground.                                                                                                                                                                                                                        | IO           | VDD33       | 3-State      | 3-State     |
| <b>TEST.</b> This is required to be tied low for functional operation. See section 9 for details.                                                                                                                                                                                                                  | Input        | VDD33       |              |             |

### 3.5 Power and Ground

**VDD12[B, A].** 1.2 volt power plane for the HyperTransport™ technology pins. VDD12A provides power to the A side of the tunnel. VDD12B provides power to the B side of the tunnel.

**VDD15.** 1.5 volt power plane for AGP.

**VDD18.** 1.8-volt power plane for the core of the IC.

**VDDA18.** Analog 1.8-volt power plane for the PLLs in the core of the IC. This power plane is required to be filtered from digital noise.

**VDD33.** 3.3-volt power plane for IO.

**VSS.** Ground.

#### 3.5.1 Power Plane Sequencing

The following are power plane requirements that may imply power supply sequencing requirements.

- VDD33 is required to always be higher than VDD18, VDDA18, VDD15, and VDD12[B, A].
- VDD18 and VDDA18 are required to always be higher than VDD15 and VDD12[B, A].
- VDD15 is required to always be higher than VDD12[B, A].

## 4 Functional Operation

### 4.1 Overview

The IC connects to the host through either the side A or side B HyperTransport™ link interface. The other side of the tunnel may or may not be connected to another device. Host-initiated transactions that do not target the IC or the bridge flow through the tunnel to the downstream device. Transactions claimed by the device are passed to internal registers or to the AGP bridge.

See section 5.1 for details about the software view of the IC. See section 5.1.2 for a description of the register naming convention. See the AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Design Guide for additional information.

### 4.2 Reset And Initialization

RESET# and PWROK are both required to be low while the power planes to the IC are invalid and for at least 1 millisecond after the power planes are valid. Deassertion of PWROK is referred to as a *cold reset*. After PWROK is brought high, RESET# is required to stay low for at least 1 additional millisecond. After RESET# is brought high, the links go through the initialization sequence.

After a cold reset, the IC may be reset by asserting RESET# while PWROK remains high. This is referred to as a *warm reset*. RESET# must be asserted for no less than 1 millisecond during a warm reset.

### 4.3 Clocking

It is required that REFCLK be valid in order for the IC to operate. Also, the LR[B, A]CLK inputs from the operation links must also be valid at the frequency defined DevA:0xCC[FREQA] and DevA:0xD0[FREQB]. The IC provides A\_PCLK as the clock to the AGP device.

The systemboard is required to include a connection from A\_PLLCLKO to A\_PLLCLKI. The length of this connection is required to be approximately the same as length of the A\_PCLK trace from the IC to the external AGP devices (including approximately 2.5 inches of etch on the AGP card). The IC uses this loopback to help match the external trace delay.

#### 4.3.1 Clock Gating

Internal clocks may be disabled during power-managed system states such as power-on suspend. It is required that all upstream requests initiated by the IC be suspended while in this state.

To enable clock gating, DevA:0xF0[ICGSMAF] is programmed to the values in which clock gating will be enabled. Stop Grant cycles and STPCLK deassertion link broadcasts interact to define the window in which the IC is enabled for clock gating during LDTSTOP# assertions. The system is placed into power managed states by steps that include a broadcast over the links of the Stop Grant cycle that includes the System Management Action Field (SMAF) followed by the assertion of LDTSTOP#. When the IC detects the Stop Grant broadcast which is enabled for clock gating, it enables clock gating for the next assertion of LDTSTOP#. While exiting the power-managed state, the system is required to broadcast a STPCLK deassertion message. The IC uses this message to disable clock gating during LDTSTOP# assertions. This is important because an LDTSTOP# assertion is not guaranteed to occur after the Stop Grant broadcast is received. The clock gating window must be closed to insure that clock gating does not occur during Stop Grant for LDTSTOP# assertions that are not associated with the power states specified by DevA:0xF0[ICGSMAF].

In summary, Stop Grant broadcasts with SMAF fields specified by DevA:0xF0[ICGSMAF] enable the clock gating window and STPCLK deassertion broadcasts disable the window. If LDTSTOP# is asserted while the clock gating window is enabled, then clock gating occurs.

Also, DevA:0xF0[ECGSMAF] may be used in a similar way to disable A\_PCLK and the internal clock grids associated with the AGP bridge. The same rules for the clock gating window that apply to DevA:0xF0[ICGSMAF] also apply to DevA:0xF0[ECGSMAF]. If clock gating is enabled, then A\_PCLK is forced low within two clock periods after LDTSTOP# is asserted. It becomes active again within two clock periods after LDTSTOP# is deasserted. It is required that there be no AGP-card-initiated upstream or downstream traffic while A\_PCLK is gated. In addition, it is required that there be no host accesses to the bridge or internal registers in progress from the time that LDTSTOP# is asserted for clock gating until the link reconnects after LDTSTOP# is deasserted.

## 4.4 Tunnel Links

HyperTransport link A supports CLK receive and transmit frequencies of 200, 400, 600, and 800 MHz. Link B supports frequencies of 200 and 400 MHz. The side A and side B frequencies are independent of each other.

### 4.4.1 Link PHY

The PHY includes automatic compensation circuitry and a software override mechanism, as specified by DevA:0x[E8, E4, E0]. The IC only implements synchronous mode clock forwarding FIFOs. So only the link receive and transmit frequencies specified in DevA:0x[D0, CC][FREQB, FREQA] are allowed.

## 4.5 AGP

The AGP bridge supports AGP 3.0 signaling at 8x and 4x data rates and 1.5-volt AGP 2.0 signaling at 4x, 2x, and 1x data rates. 64-bit upstream and 32-bit downstream addressing is supported. AGP 3.0 dynamic bus inversion is supported on output signals in 8X mode only, not in 4X mode; dynamic bus inversion on input signals is supported in both 4X and 8X modes.

### 4.5.1 Tags, UnitIDs, And Ordering

The IC requires three HyperTransport™ technology-defined UnitIDs. They are allocated as follows:

- First UnitID is not used. This is to avoid a potential conflict with the host (because it may be zero; see DevA:0xC0[BUID]).
- Second UnitID is used for PCI-mode upstream requests and responses to host requests.
- Third UnitID is used for AGP (high priority and low priority) upstream requests.

The SrcTag value that is assigned to upstream non-posted AGP requests increments with each request from 0 to 27 and then rolls over to 0 again; the first SrcTag assigned after reset is 0. Up to 28 non-posted link requests may be outstanding at a time. The SrcTag value that is assigned to non-posted PCI requests is always 28.

All AGP transactions are compliant to AGP ordering rules. APG transactions are translated into link transactions as follows:

| AGP transaction     | Link transaction                               |
|---------------------|------------------------------------------------|
| High priority write | WrSized, posted channel, PassPW = 1            |
| High priority read  | RdSized, PassPW = 1, response PassPW = 1       |
| Low priority write  | WrSized, posted channel, PassPW = 0            |
| Low priority read   | RdSized, PassPW = 0, response PassPW = 1       |
| Low priority flush  | Flush, PassPW = 0                              |
| Low priority fence  | None (wait for all outstanding read responses) |

**Table 2: Translation from AGP requests to link requests.**

#### 4.5.2 Various Behaviors

- The AGP bridge does not claim link special cycles. However, special cycles that are encoded in configuration cycles to device 31 of the AGP secondary bus number (per the PCI-to-PCI bridge specification) are translated to AGP bus special cycles.
- AGP and PCI read transactions that receive NXA responses from the host complete onto the AGP bus with the data provided by the host (which is required to be all 1's, per the link specification).
- In the translation from type 1 link configuration cycles to secondary bus type 0 configuration cycles, the IC converts the device number to IDSEL AD signal as follows: device 0 maps to AD[16]; device 1 maps to AD[17]; and so forth. Device numbers 16 through 31 are not valid.
- The compensation values for drive strength and input impedance that are assigned to non-clock forwarded AGP signals are automatically determined and set by the IC during the first compensation cycle after RESET#. Once set, they do not change until the next RESET# assertion.
- Per the link protocol, when the COMPAT bit is set in the transaction, the IC does not ever claim the transaction. Such transactions are automatically passed to the other side of the tunnel (or master aborted if the IC is at the end of the chain). This is true of all transactions within address space that is otherwise claimed by the IC, including the space defined by DevB:0x3C[VGAEN].

##### 4.5.2.1 AGP Compensation And Calibration Cycles

The AGP PHY includes one compensation circuit for the clock forwarded data signals, A\_AD[31:0], A\_CBE\_L[3:0], and A\_DBI[H, L], and one compensation circuit for the strobes, A\_ADSTB[1:0]. Each compensation circuit calculates the required rising-edge (P) and falling-edge (N) signal drive strength through a free-running state machine that generates a new value approximately every four microseconds. These values are provided in DevA:0x[50, 54][NCOMP, PCOMP].

Programmable skew values between data signals and strobes are also provided in DevA:0x58.

The compensation values provided to the AGP PHY are software selectable between the calculated compensation values, fixed programmable bypass values, or fixed programmable offsets from the calculated values. Regardless of which value is selected, the value presented to the PHY is never updated until there is a calibration cycle.

Calibration cycles consist of taking control of the AGP bus, updating the AGP PHY compensation values, and then releasing (see DevA:0xA8[PCALCYC]). If enabled by DevA:0xB0[CALDIS], they occur periodically with the period specified by DevA:0xA8[PCALCYC].

The first calibration cycle occurs approximately 4 milliseconds after the deassertion of RESET# (whether AGP 2.0 or 3.0 signaling is enabled).

## 5 Registers

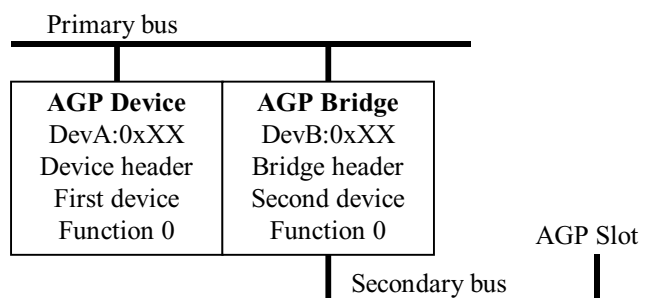
### 5.1 Register Overview

The IC includes several sets of registers accessed through a variety of address spaces. IO address space refers to register addresses that are accessed through x86 IO instructions such as IN and OUT. PCI configuration space is typically accessed by the host through IO cycles to CF8h and CFCh. There is also memory space and indexed address space in the IC.

#### 5.1.1 Configuration Space

The address space for the IC configuration registers is broken up into *busses*, *devices*, *functions*, and, *offsets*, as defined by the link specification. It is accessed by HyperTransport™ technology-defined type 0 configuration cycles. The device number is mapped into bits[15:11] of the configuration address. The function number is mapped into bits[10:8] of the configuration address. The offset is mapped to bits[7:2] of the configuration address.

The following diagram shows the devices in configuration space as viewed by software.



**Figure 2: Configuration space.**

Device A, above, is programmed to be the link base UnitID and device B is the link base UnitID plus 1.

#### 5.1.2 Register Naming and Description Conventions

Configuration register locations are referenced with mnemonics that take the form of Dev[A|B]:[7:0]x[FF:0], where the first set of brackets contain the device number, the second set of brackets contain the function number, and the last set of brackets contain the offset.

Other register locations (e.g. memory mapped registers) are referenced with an assigned mnemonic that specifies the address space and offset. These mnemonics start with two or three characters that identify the space followed by characters that identify the offset within the space.

Register fields within register locations are also identified with a name or bit group in brackets following the register location mnemonic.

The following are configuration spaces:

| Device | Function | Mnemonic  | Registers                                           |
|--------|----------|-----------|-----------------------------------------------------|
| "A"    | 0        | DevA:0xXX | AGP device header; link and AGP capabilities blocks |
| "B"    | 0        | DevB:0xXX | PCI-PCI bridge registers for AGP                    |

**Table 3: Configuration spaces.**

The IC does not claim configuration-register accesses to unimplemented functions within its devices (they are forwarded to the other side of the tunnel). Accesses to unimplemented register locations within implemented functions are claimed; such writes are ignored and reads always respond with all zeros.

The following are memory mapped spaces:

| Base address register | Size (bytes) | Mnemonic | Registers                                                 |
|-----------------------|--------------|----------|-----------------------------------------------------------|
| DevA:0x10             | Variable     | None     | Graphic virtual memory aperture; minimum of 32 megabytes. |
| DevA:0xB8             | 4K           | None     | GART block in physical memory.                            |

**Table 4: Memory mapped address spaces.**

The following are register attributes found in the register descriptions.

| Type              | Description                                                                                                                                                                                                                                                                                                                        |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Read or read-only | Capable of being read by software. Read-only implies that the register cannot be written to by software.                                                                                                                                                                                                                           |
| Write             | Capable of being written by software.                                                                                                                                                                                                                                                                                              |
| Set by hardware   | Register bit is set high by hardware.                                                                                                                                                                                                                                                                                              |
| Write once        | After RESET#, these registers may be written to once. After being written, they become read only until the next RESET# assertion. The write-once control is byte based. So, for example, software may write each byte of a write-once DWORD as four individual transactions. As each byte is written, that byte becomes read only. |
| Write 1 to clear  | Software must write a 1 to the bit in order to clear it. Writing a 0 to these bits has no effect.                                                                                                                                                                                                                                  |
| Write 1 only      | Software can set the bit high by writing a 1 to it. However subsequent writes of 0 will have no effect. RESET# must be asserted in order to clear the bit.                                                                                                                                                                         |

**Table 5: Register attributes.**

## 5.2 AGP Device Configuration Registers

These registers are located in PCI configuration space, in the first device (device A), function 0. See section 5.1.2 for a description of the register naming convention.

### AGP Vendor And Device ID Register

DevA:0x00

Default: 7454 1022h

Attribute: Read only.

| Bits  | Description    |
|-------|----------------|
| 31:16 | AGP device ID. |
| 15:0  | Vendor ID.     |

**AGP Device Status And Command Register****DevA:0x04**

Default: 0210 0000h

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                        |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | <b>DPE: detected parity error.</b> Read only. This bit is fixed in the low state.                                                                                                                                                                                                  |
| 30    | <b>SSE: signaled system error.</b> Read; set by hardware; write 1 to clear. 1=A system error was signaled (both links were flooded with sync packets) as a result of a CRC error (see DevA:0x[C8:C4][CRCFEN, CRCERR]). Note: this bit is cleared by PWROK reset but not by RESET#. |
| 29    | <b>RMA: received master abort.</b> Read; set by hardware; write 1 to clear. 1=A request (AGP or PCI) sent to the host bus received a master abort (an NXA error response). Note: this bit is cleared by PWROK reset but not by RESET#.                                             |
| 28    | <b>RTA: received target abort.</b> Read; set by hardware; write 1 to clear. 1=A request (AGP or PCI) sent to the host bus received a target abort (a non-NXA error response). Note: this bit is cleared by PWROK reset but not by RESET#.                                          |
| 27:21 | Read only. These bits are fixed in their default state.                                                                                                                                                                                                                            |
| 20    | <b>Capabilities pointer.</b> Read only. This bit is fixed in the high state.                                                                                                                                                                                                       |
| 19:3  | Read only. These bits are fixed in their default state.                                                                                                                                                                                                                            |
| 2     | <b>MASEN: PCI master enable.</b> Read-write. This bit controls no hardware in the IC.                                                                                                                                                                                              |
| 1     | <b>MEMEN: memory enable.</b> Read-write. 1=Enables access to the memory space specified by DevA:0x10. This bit controls no hardware in the IC.                                                                                                                                     |
| 0     | <b>IO enable.</b> Read only. This bit is fixed in the low state.                                                                                                                                                                                                                   |

**AGP Device Revision and Class Code Register****DevA:0x08**

Default: 0600 00??h

Attribute: See below.

| Bits | Description                                                             |
|------|-------------------------------------------------------------------------|
| 31:8 | <b>CLASSCODE.</b> Read; write once. Provides the AGP bridge class code. |
| 7:0  | <b>REVISION.</b> Read only.                                             |

**AGP Device BIST-Header-Latency-Cache Register****DevA:0x0C**

Default: 0000 0000h

Attribute: Read only.

| Bits  | Description                                               |
|-------|-----------------------------------------------------------|
| 31:24 | <b>BIST.</b> These bits fixed at their default values.    |
| 23:16 | <b>HEADER.</b> These bits fixed at their default values.  |
| 15:8  | <b>LATENCY.</b> These bits fixed at their default values. |
| 7:0   | <b>CACHE.</b> These bits fixed at their default values.   |

**AGP Device Graphic Virtual Memory Aperture Register****DevA:0x10**

It is expected that the state of this register is copied into the host by software. This register controls no hardware in the IC.

Default: 0000 0000 0000 0008h

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                               |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63:32 | <b>APBARHI.</b> Read-write. Aperture base address register high. Note: bits[63:40] are required to be programmed low; setting any of these bits high results in undefined behavior. Note: if DevA:0x10[64BIT]=0, then these bits are read only, all zero. |
| 31:22 | <b>APBARLO.</b> Aperture base address register low. These bits are a combination of read-write and read-only zero, based on the state of DevA:0xB4[APSIZE]; see that register for details.                                                                |
| 21:4  | Reserved.                                                                                                                                                                                                                                                 |
| 3     | Read only. This bit is fixed at its default value to indicate that this register points prefetchable space.                                                                                                                                               |
| 2     | <b>64BIT: 64-bit pointer.</b> Read; write once. 1=DevA:0x10 is a 64-bit pointer. 0=DevA:0x10 is a 32-bit pointer; bits[63:32] are reserved.                                                                                                               |
| 1:0   | Read only. These bits are fixed at their default value to indicate that this register points memory space.                                                                                                                                                |

**AGP Device Subsystem ID and Subsystem Vendor ID Register****DevA:0x2C**

Default: 0000 0000h

Attribute: Read; write once.

| Bits  | Description                                                  |
|-------|--------------------------------------------------------------|
| 31:16 | <b>Subsystem ID.</b> This field controls no hardware.        |
| 15:0  | <b>Subsystem vendor ID.</b> This field controls no hardware. |

**AGP Capabilities Pointer****DevA:0x34**

Default: 0000 00A0h

Attribute: Read only.

| Bits | Description                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved.                                                                                                 |
| 7:0  | <b>Capabilities pointer.</b> Specifies the offset in DevA:0 address space for the AGP capabilities block. |

## AGP Miscellaneous Control Register

DevA:0x40

Default: 0000 0000h

Attribute: See below.

| Bits | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 6    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 4    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3    | <b>FWDIS: fast write disable.</b> Read-write. 1=DevA:0xA4[FWSUP] is low. 0=DevA:0xA4[FWSUP] is high.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2    | <b>8XDIS: AGP 3.0 signaling mode disable.</b> Read-write. 0=The IC drives A_MB8XDET# low to indicate support for AGP 3.0 signaling. 1=The IC does not drive A_MB8XDET low. This bit may be used in conjunction with DevB:0x3C[SBRST] to revert back to AGP 2.0 signaling. To do this, software should (1) set DevB:0x3C[SBRST] in order to reset the AGP card, (2) set 8XDIS to cause A_MB8XDET# to float high, and (3) clear DevB:0x3C[SBRST].                                                                                                                                                                                                                                          |
| 1    | <b>TYPEDET: AGP voltage type detection.</b> Read only. This bit reflects the state of the A_TYPEDET# pin. 0=The AGP master supports 1.5 volt signaling. 1=The AGP master requires 3.3 volt signaling and is therefore not compatible with the IC. If this bit is detected high by BIOS, an error should be signaled.                                                                                                                                                                                                                                                                                                                                                                     |
| 0    | <b>DBIEN: dynamic bus inversion enable.</b> Read-write. 1= A_DBI[H, L] enabled to dynamically invert the state of the A_AD signals when the IC is driving these. This only applies to AGP 3.0 transfers in the downstream direction (fast writes and read responses to AGP master requests). For PCI transfers in the downstream direction, A_DBI[H, L] are held inactive and no inversion takes place. 0=When the IC drives the A_AD lines, A_DBI[H, L] are driven low. Note: this bit is only valid when 8x transfer rates are enabled; if (1) DevA:0xA4[AGP3MD]=0 or (2) DevA:0xA4[AGP3MD]=1 and DevA:0xA8[DRATE] is not 010b, then this field is ignored and the DBI is not enabled. |

**AGP PHY Control Register****DevA:0x[54, 50]**

These registers apply to the compensation values of AGP clock-forwarded data and strobe signals as follows:

- DevA:0x50: data signals A\_AD[31:0], A\_CBE\_L[3:0], A\_DBI[H, L], and A\_SBA[7:0].
- DevA:0x54: strobe signals A\_ADSTB[1:0]\_[P, N] and A\_SBSTB\_[P, N].

NCTL, NDATA, and NCOMP are related to (1) the falling edge drive strength of the signals as outputs and (2) the impedance of the signals as inputs. PCTL, PDATA, and PCOMP are related to the rising edge drive strength of the signals as outputs only. For the [N, P]DATA and [N, P]COMP fields of these registers, 00h corresponds to the weakest drive strength and the highest receive impedance. For the [N, P]DATA and [N, P]COMP fields of these registers, the highest values corresponds to the strongest drive strength and lowest receive impedance.

External compensation resistors are used by the IC to determine the proper drive strength values. The resistors correlate the calculated values as follows:

- A\_CALD is used to calculate DevA:0x50[PCOMP] (data signal rising edge drive strength).
- A\_CALD# is used to calculate DevA:0x50[NCOMP] (data signal falling edge drive strength and receive impedance).
- A\_CALS is used to calculate DevA:0x54[PCOMP] (strobe rising edge drive strength).
- A\_CALS# is used to calculate DevA:0x54[NCOMP] (strobe falling edge drive strength and receive impedance).

Note: when new values are written to these registers, new compensation values are not updated to the AGP PHY automatically; the periodic calibration cycle specified by DevA:0xA8[PCALCYC] must pass in order for the AGP PHY calibration values to take effect.

Default: 000? 000?h

Attribute: See below.

| Bits        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|-----|-------------------------------------------------|-----|-------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 31:30       | <p><b>NCTL: AGP PHY N (falling edge) compensation control.</b> Read-write. These two bits combine to specify the PHY falling edge compensation value that is applied to AGP signals as follows:</p> <table> <tr> <th><u>NCTL</u></th><th><u>Description</u></th></tr> <tr> <td>00b</td><td>Apply NCOMP directly as the compensation value.</td></tr> <tr> <td>01b</td><td>Apply NDATA directly as the compensation value.</td></tr> <tr> <td>10b</td><td>Apply the sum of NCOMP and NDATA as the compensation value. If the sum exceeds 3Fh, then 3Fh is applied.</td></tr> <tr> <td>11b</td><td>Apply the difference of NCOMP minus NDATA as the compensation value. If the difference is less than 00h, then 00h is applied.</td></tr> </table> | <u>NCTL</u> | <u>Description</u> | 00b | Apply NCOMP directly as the compensation value. | 01b | Apply NDATA directly as the compensation value. | 10b | Apply the sum of NCOMP and NDATA as the compensation value. If the sum exceeds 3Fh, then 3Fh is applied. | 11b | Apply the difference of NCOMP minus NDATA as the compensation value. If the difference is less than 00h, then 00h is applied. |
| <u>NCTL</u> | <u>Description</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 00b         | Apply NCOMP directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 01b         | Apply NDATA directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 10b         | Apply the sum of NCOMP and NDATA as the compensation value. If the sum exceeds 3Fh, then 3Fh is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 11b         | Apply the difference of NCOMP minus NDATA as the compensation value. If the difference is less than 00h, then 00h is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 29:28       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 27:22       | <b>NDATA: AGP falling edge drive strength control.</b> Read-write. This value is applied to the falling-edge (N transistor) PHY compensation as described in NCTL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 21:16       | <b>NCOMP: AGP falling edge drive strength.</b> Read only. This provides the calculated value of the falling-edge (N transistor) drive strength of the AGP signals. The default for this field varies. This field is updated by the hardware approximately every 8 microseconds.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |

| 15:14       | <b>PCTL: AGP PHY P (rising edge) compensation control.</b> Read-write. These two bits combine to specify the PHY rising edge compensation value that is applied to AGP signals as follows:<br><br><table> <tr> <th><u>PCTL</u></th><th><u>Description</u></th></tr> <tr> <td>00b</td><td>Apply PCOMP directly as the compensation value.</td></tr> <tr> <td>01b</td><td>Apply PDATA directly as the compensation value.</td></tr> <tr> <td>10b</td><td>Apply the sum of PCOMP and PDATA as the compensation value. If the sum exceeds 1Fh, then 1Fh is applied.</td></tr> <tr> <td>11b</td><td>Apply the difference of PCOMP minus PDATA as the compensation value. If the difference is less than 00h, then 00h is applied.</td></tr> </table> | <u>PCTL</u> | <u>Description</u> | 00b | Apply PCOMP directly as the compensation value. | 01b | Apply PDATA directly as the compensation value. | 10b | Apply the sum of PCOMP and PDATA as the compensation value. If the sum exceeds 1Fh, then 1Fh is applied. | 11b | Apply the difference of PCOMP minus PDATA as the compensation value. If the difference is less than 00h, then 00h is applied. |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|-----|-------------------------------------------------|-----|-------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| <u>PCTL</u> | <u>Description</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 00b         | Apply PCOMP directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 01b         | Apply PDATA directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 10b         | Apply the sum of PCOMP and PDATA as the compensation value. If the sum exceeds 1Fh, then 1Fh is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 11b         | Apply the difference of PCOMP minus PDATA as the compensation value. If the difference is less than 00h, then 00h is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 13:12       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 11          | <b>RW: read-write bit.</b> Read-write. This controls no logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 10:6        | <b>PDATA: AGP rising edge drive strength control.</b> Read-write. This value is applied to the rising-edge (P transistor) PHY compensation as described in PCTL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 5           | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |
| 4:0         | <b>PCOMP: AGP rising edge drive strength.</b> Read only. This provides the calculated value of the rising-edge (P transistor) drive strength of the AGP signals. The default for this field varies. This field is updated by the hardware approximately every 8 microseconds.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |             |                    |     |                                                 |     |                                                 |     |                                                                                                          |     |                                                                                                                               |

**AGP PHY Skew Control Register****DevA:0x58**

DSKEW and SSKEW are designed such that when they are both programmed to the same value, the AGP output strobes transition near the center of the data eye. To move the strobe to a later point in the data eye, the value of SSKEW is increased. To move the strobe to an earlier point in the data eye, DSKEW is increased. These values translate into skew approximately as follows:

For values 0h to 8h, the skew is about:  $[D, S]SKEW \times 80$  picoseconds.

For values 9h to Fh, the skew is about:  $800 + ([D, S]SKEW - 8) \times 400$  picoseconds.

However, these values vary with process, temperature, and voltage. Note that the lower values provide fine resolution and the upper values provide coarse resolution.

Default: 0000 0000h.

Attribute: Read-write.

| Bits | Description                                                                                                                                                                                                                                      |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved.                                                                                                                                                                                                                                        |
| 7:4  | <b>DSKEW: AGP data skew.</b> Read-write. This specifies the alignment of the AGP data signal outputs, A_AD[31:0], A_CBE_L[3:0], and A_DBI[H, L], relative internal clocks. 0h=The strobe transitions earliest. Fh=The strobe transitions latest. |
| 3:0  | <b>SSKEW: AGP strobe skew.</b> Read-write. This specifies the alignment of the AGP strobe signal outputs, A_ADSTB[1:0], relative internal clocks. 0h=The strobe transitions earliest. Fh=The strobe transitions latest.                          |

**AGP Most Recent Request Register****DevA:0x60**

As each PIPE mode or SBA mode AGP request is transferred into the IC, the fields are placed into this register. Thus, this register provides the fields of the most recent AGP requests. Any sticky bits from prior requests that have not been updated in the current request are also valid. Note: fences are not captured by this register.

Default: 0000 0000 0000 0000h

Attribute: Read only.

| Bits  | Description                                                                                                                                                                                                                     |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63:44 | Reserved.                                                                                                                                                                                                                       |
| 43:40 | <b>MRC: most recent command field.</b> Specifies the command field of the most recent AGP request. 0h=LP (low priority) read. 1h=HP (high priority) read. 4h=LP write. 5h=HP write. 8h=LP long read. 9h=HP long read. Ah=Flush. |
| 39:3  | <b>MRA: most recent address.</b> Specifies address bits[39:3] of the most recent AGP request.                                                                                                                                   |
| 2:0   | <b>MRL: most recent length field.</b> Specifies the length field of the most recent AGP request.                                                                                                                                |

**AGP Revision and Capability Register****DevA:0xA0**

Default: 0030 C002h

Attribute: Read only.

| Bits  | Description                                                                                                         |
|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:24 | Reserved.                                                                                                           |
| 23:16 | <b>AGP specification.</b> This field is hardwired to indicate that the IC conforms to AGP specification revision 3. |
| 15:8  | <b>Next capabilities block.</b> Specifies the offset to the next capabilities block.                                |
| 7:0   | <b>Capabilities type.</b> Specifies the AGP capabilities block.                                                     |

**AGP Status Register****DevA:0xA4**

Default: 1F00 0B2?h (see bit descriptions for bits[3:0]) Attribute: Read only.

| Bits  | Description                                                                                                             |
|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:24 | <b>RQ: maximum number of outstanding requests.</b> This field is set to indicate support for 32 outstanding requests.   |
| 23:18 | Reserved.                                                                                                               |
| 17    | <b>Isochronous support.</b> This bit fixed in the low state to indicate that the IC does not support isochronous modes. |
| 16:13 | Reserved.                                                                                                               |
| 12:10 | <b>Calibration cycle.</b> This field is set to indicate a requirement for calibration cycles every 64 milliseconds.     |
| 9     | <b>SBA support.</b> This field is set to indicate support for SBA.                                                      |
| 8     | <b>Coherency.</b> This bit fixed high.                                                                                  |
| 7     | <b>64-bit GART support.</b> This bit fixed low.                                                                         |
| 6     | <b>Host translation#.</b> This bit fixed low.                                                                           |
| 5     | <b>Greater-than 4 gigabyte support.</b> This bit fixed high.                                                            |

|     |                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | <b>FWSUP: fast write support flag.</b> 0=Fast writes are not supported. 1=Fast writes are supported. The state of this bit is controlled by DevA:0x40[FWDIS].                                                                                                                                                                                                              |
| 3   | <b>AGP3MD: AGP 3.0 signaling mode detected.</b> 1=The IC detected connection to an AGP 3.0-capable master and is programmed for AGP 3.0 signaling. 0=The IC detected connection to an AGP 2.0 or earlier capable master or is not programmed for 1.5-volt, AGP 2.0 signaling. If DevA:0x40[8XDIS]=0 and the pin A_GC8XDET#=0, then this bit is high. Otherwise, it is low. |
| 2:0 | <b>RATE: data rate.</b> When AGP3MD=1, then this field defaults to 011b to indicate support for 4x and 8x data rates. When AGP3MD=0, this field defaults to 111b to indicate support for 4x, 2x, and 1x data rates.                                                                                                                                                        |

**AGP Command Register****DevA:0xA8**

Default: 0000 0000h

Attribute: Read-write.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 12:10 | <b>PCALCYC: periodic calibration cycle.</b> Specifies the period between calibration cycles as follows: 000b=4 milliseconds; 001b=16 milliseconds; 010=64 milliseconds; 011b=256 milliseconds; all other values are reserved. When DevA:0xA4[AGP3MD]=1, calibration cycles are as specified in the AGP 3.0 specification. When DevA:0xA4[AGP3MD]=0, calibration cycles consist of (1) the internal calibration logic requests the bus; (2) once granted, the calibration values are update in less than 6 A_PCLK cycles while the AGP bus is in a quiescent state. Note: after changing this value, the IC may not perform another calibration cycle until the internal counter rolls over as much as 256 microseconds later; in order to avoid this, DevA:0xB0[CALDIS] should be set high before changing PCALCYC and then DevA:0xB0[CALDIS] should be cleared afterward. |
| 9     | <b>SBA_EN: side band address enable.</b> 1=SBA addressing is enabled. Note: when DevA:0xA4[AGP3MD]=1, SBA addressing is enabled and the state of this bit is ignored.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 8     | <b>AGPEN: AGP operation enable.</b> 1=The IC accepts master-initiated AGP commands. 0=AGP commands are ignored.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 7:6   | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5     | <b>R4GEN: receive greater-than 4-gigabyte access enable.</b> 1=The IC accepts AGP accesses to addresses greater than 4 gigabytes.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 4     | <b>FWEN: fast write enable.</b> 1=Fast writes are enabled. When DevA:0xA4[FWSUP]=0, this bit is required to be programmed low; if, in this case, this bit is programmed high, then undefined behavior results.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

|     |                                                                                                                               |              |                                 |
|-----|-------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------------------|
| 2:0 | <b>DRATE: data transfer mode rate.</b> This field is combined with DevA:0xA4[AGP3MD] to specify the AGP data rate as follows: |              |                                 |
|     | <u>AGP3MD</u>                                                                                                                 | <u>DRATE</u> |                                 |
|     | X                                                                                                                             | 000          | No AGP mode selected.           |
|     | 0                                                                                                                             | 001          | 1x AGP rate; AGP 2.0 signaling. |
|     | 0                                                                                                                             | 010          | 2x AGP rate; AGP 2.0 signaling. |
|     | 0                                                                                                                             | 100          | 4x AGP rate; AGP 2.0 signaling. |
|     | 1                                                                                                                             | 001          | 4x AGP rate; AGP 3.0 signaling. |
|     | 1                                                                                                                             | 010          | 8x AGP rate; AGP 3.0 signaling. |
|     | 1                                                                                                                             | 100          | Reserved.                       |

**AGP Control Register****DevA:0xB0**

Default: 0000 0000h

Attribute: Read-write.

| Bits  | Description                                                                                                                                                                           |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | Reserved.                                                                                                                                                                             |
| 9     | <b>CALDIS: calibration cycle disable.</b> 1=Calibration cycles (as defined in DevA:0xA8[PCALCYC]) are disabled.                                                                       |
| 8     | <b>APEREN: graphics aperture enable.</b> This bit controls no hardware in the IC. It is expected that the state of this bit is copied into the host by software.                      |
| 7     | <b>GTLBEN: graphics translation look-aside buffer enable.</b> This bit controls no hardware in the IC. It is expected that the state of this bit is copied into the host by software. |
| 6:0   | Reserved.                                                                                                                                                                             |

**AGP Aperture Size Register****DevA:0xB4**

Default: 0001 0F00h

Attribute: See below.

| Bits  | Description                                                                                                                         |
|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | <b>PGSZSEL: page size select.</b> Read-write. The only legal value for these bits is 0000b, which specifies a 4-kilobyte page.      |
| 27    | Reserved.                                                                                                                           |
| 26:16 | <b>Page size support.</b> Read only. These bits are fixed in their default state to indicate that the IC supports 4-kilobyte pages. |
| 15:12 | Reserved.                                                                                                                           |

11:0

**APSIZE: graphic virtual memory aperture size.** Read-write (except bits[11, 7:6, and 2:0] which are read only, fixed at the default value). This field specifies the size of the aperture pointed to by DevA:0x10. This field also controls read only versus read-write control over several bits in DevA:0x10. It is encoded as follows:

| <u>Bits[10, 9, 8, 5, 4, 3]</u> | <u>Aperture size</u> | DevA:0x10<br><u>read-write bits</u> | DevA:0x10<br><u>read-only bits</u> |
|--------------------------------|----------------------|-------------------------------------|------------------------------------|
| 1 1 1 1 1 1                    | 32 MB                | [63:25]                             | [24:0]                             |
| 1 1 1 1 1 0                    | 64 MB                | [63:26]                             | [25:0]                             |
| 1 1 1 1 0 0                    | 128 MB               | [63:27]                             | [26:0]                             |
| 1 1 1 0 0 0                    | 256 MB               | [63:28]                             | [27:0]                             |
| 1 1 0 0 0 0                    | 512 MB               | [63:29]                             | [28:0]                             |
| 1 0 0 0 0 0                    | 1024 MB              | [63:30]                             | [29:0]                             |
| 0 0 0 0 0 0                    | 2048 MB              | [63:31]                             | [30:0]                             |

It is expected that the state of this field is copied into the host by software. Note: DevA:0x10[2] is “read; write once,” even though it is shown as read-only above. Also, based on the state of DevA:0x10[2], DevA:0x10[63:32] may be read-only, all zeros.

**AGP Device GART Pointer****DevA:0xB8**

This register controls no hardware in the IC. It is expected that the state of this register is copied into the host by software.

Default: 0000 0000 0000 0000h

Attribute: Read-write.

| Bits  | Description                                     |
|-------|-------------------------------------------------|
| 63:32 | <b>GARTHI: GART base address register high.</b> |
| 31:12 | <b>GARTLO: GART base address register low.</b>  |
| 11:0  | Reserved.                                       |

**Link Command Register****DevA:0xC0**

Default: 0060 0008h

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | <b>Slave/primary interface type.</b> Read only.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 28    | <b>DOUI: drop on uninitialized link.</b> Read-write. This specifies the behavior of transactions that are sent to uninitialized links. 0=Transactions that are received by the IC and forwarded to a side of the tunnel, when DevA:0x[C4/C8][INITCPLT and ENDOCH] for that side of the tunnel are both low, remain in buffers awaiting transmission indefinitely (waiting for INITCPLT to be set high). 1=Transactions that are received by the IC and forwarded to a side of the tunnel, when DevA:0x[C4/C8][INITCPLT and ENDOCH] for that side of the tunnel are both low, behave as if ENDOCH were high. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 27    | <b>DEFDIR: default direction.</b> Read-write. 0=Send AGP master requests to the master link host as specified by DevA:0xC0[MASHST]. 1=Send AGP master requests to the opposite side of the tunnel.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26    | <b>MASHST: master host.</b> Read; set and cleared by hardware. This bit indicates which link is the path to the master (or only) host bridge on the HyperTransport™ technology chain. 1=The hardware set this bit as a result of a write command from the B side of the tunnel to any of the bytes of DevA:0xC0[31:16]. 0=The hardware cleared this bit as a result of a write command from the A side of the tunnel to any of the bytes of DevA:0xC0[31:16]. This bit, along with DEFDIR, is used to determine the side of the tunnel to which AGP master requests are sent.                                                                                                                                                                                                                                                                                            |
| 25:21 | <b>UnitID count.</b> Read only. Specifies the number of UnitIDs used by the IC (three).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 20:16 | <b>BUID: base UnitID.</b> Read-write. This specifies the link-protocol base UnitID. The IC's logic uses this value to determine the UnitIDs for link request and response packets. When a new value is written to this field, the response includes a UnitID that is based on the new value in this register. Note: some legacy operating systems may require that this value be set to zero for normal operation so that the AGP capability block is part of device 0. Since the IC does not use the base unit ID in any link transactions, there is no conflict with the host unit ID. However, at boot, BIOS is required to temporarily change the BUID value of the IC so that the BUID values in downstream devices may be initialized. After downstream BUID values are initialized, this field may be set to zero to be compatible with legacy operating systems. |
| 15:8  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0   | <b>Capabilities ID.</b> Read only. Specifies the capabilities ID for link configuration space.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Link Configuration And Control Register****DevA:0xC4 and DevA:0xC8**

DevA:0xC4 applies side A of the tunnel and DevA:0xC8 applies to side B of the tunnel. The default value for bit[5] may vary (see the definition).

Default: ??11 0020h for DevA:0xC4 and ??00 0020h for DevA:0xC8. Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 30:28 | <b>LWO: link width out.</b> Read-write. Specifies the operating width of the outgoing link. Legal values are 001b (16 bits; DevA:0xC4 only), 000b (8 bits), 101b (4 bits), 100b (2 bits), and 111b (not connected). Note: this field is cleared by PWROK reset but not by RESET#; the default value of this field depends on the widths of the links of the connecting device, per the link specification. Note: after this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs through or LDTSTOP#.          |
| 27    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 26:24 | <b>LWI: link width in.</b> Read-write. Specifies the operating width of the incoming link. Legal values are 001b (16 bits; DevA:0xC4 only), 000b (8 bits), 101b (4 bits), 100b (2 bits), and 111b (not connected). Note: this field is cleared by PWROK reset but not by RESET#; the default value of this field depends on the widths of the links of the connecting device, per the link specification. Note: after this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs through an LDTSTOP# assertion. |
| 23    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 22:20 | <b>Max link width out.</b> Read only. This specifies the width of the outgoing link to be 16 bits wide for side A and 8 bits wide for side B.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18:16 | <b>Max link width in.</b> Read only. This specifies the width of the incoming link to be 16 bits wide for side A and 8 bits wide for side B.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 14    | <b>EXTCTL: extended control time during initialization.</b> Read-write. This specifies the time in which LT[B, A]CTL is held asserted during the initialization sequence that follows an LDTSTOP# deassertion, after LR[B, A]CTL is detected asserted. 0=At least 16 bit times. 1=About 50 microseconds. Note: this bit is cleared by PWROK reset but not by RESET#.                                                                                                                                                                                                                                                                                                                                                                                 |
| 13    | <b>LDT3SEN: link three-state enable.</b> Read-write. 1=During the LDTSTOP# disconnect sequence, the link transmitter signals are placed into the high impedance state and the receivers are prepared for the high impedance mode. For the receivers, this includes cutting power to the receiver differential amplifiers and ensuring that there are no resultant high-current paths in the circuits. 0=During the LDTSTOP# disconnect sequence, the link transmitter signals are driven, but in an undefined state, and the link receiver signals are assumed to be driven. Note: this bit is cleared by PWROK reset but not by RESET#. AMD recommends that this bit be set high in single-processor systems and be low in multi-processor systems. |
| 12:10 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 9:8   | <b>CRCERR: CRC Error.</b> Read; set by hardware; write 1 to clear. Bit[9] applies to the upper byte of the link (DevA:0xC4 only) and bit[8] applies to the lower byte. 1=The hardware detected a CRC error on the incoming link. Note: this bit is cleared by PWROK reset but not by RESET#.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7     | <b>TXOFF: transmitter off.</b> Read; write 1 only. 1=No output signals on the link toggle; the input link receivers are disabled and the pins may float.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | <b>ENDUCH: end of chain.</b> Read; write 1 only or set by hardware. 1=The link is not part of the logical HyperTransport technology chain; packets which are issued or forwarded to this link are either dropped or result in an NXA error response, as appropriate; packets received from this link are ignored and CRC is not checked; if the transmitter is still enabled (TXOFF), then it drives only NOP packets with good CRC. ENDOCH may be set by writing a 1 to it or it may be set by hardware if the link is determined to be disconnected at the rising edge of RESET#.                                                                                                                                                                  |
| 5     | <b>INITCPLT: initialization complete.</b> Read only. This bit is set by hardware when low-level link initialization has successfully completed. If there is no device on the other end of the link, or if the device on the other side of the link is unable to properly perform link initialization, then the bit is not set. This bit is cleared when RESET# is asserted or after the link disconnect sequence completes after the assertion of LDTSTOP#.                                                                                                                                                                                                                                                                                          |
| 4     | <b>LKFAIL: link failure.</b> Read; set by hardware; write 1 to clear. This bit is set high by the hardware when a CRC error is detected on the link (if enabled by CRCFEN) or if the link is not used in the system. Note: this bit is cleared by PWROK reset, not by RESET#.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3     | <b>CRCERRCMD: CRC error command.</b> Read-write. 1=The link transmission logic generates erroneous CRC values. 0=Transmitted CRC values match the values calculated per the link specification. This bit is intended to be used to check the CRC failure detection logic of the device on the other side of the link.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1     | <b>CRCFEN: CRC flood enable.</b> Read-write. 1=CRC errors (in link A for DevA:0xC4[CRCFEN]; in link B for DevA:0xC8[CRCFEN]) result in sync packets to both outgoing links, DevA:0x04[SSE] is set, and the LKFAIL bit is set. 0=CRC errors do not result in sync packets, setting of DevA:0x04[SSE] or the LKFAIL bit.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 0     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Link Frequency Capability 0 Register****DevA:0xCC**

Default: 0035 0022h.

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | <b>FREQCAPA: link A frequency capability.</b> Read only. These bits indicate that A side of the tunnel supports 200, 400, 600, and 800 MHz link frequencies.                                                                                                                                                                                                                        |
| 15:12 | Reserved.                                                                                                                                                                                                                                                                                                                                                                           |
| 11:8  | <b>FREQA: link A frequency.</b> Read-write. Specifies the link side A frequency. Legal values are 0h (200 MHz), 2h (400 MHz), 4h (600 MHz), and 5h (800 MHz). Note: this bit is cleared by PWROK reset, not by RESET#. Note: after this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs through LDTSTOP#. |
| 7:0   | <b>REVISION.</b> Read only. Revision A of the IC is designed to version 1.02 of the link specification.                                                                                                                                                                                                                                                                             |

**Link Frequency Capability 1 Register****DevA:0xD0**

Default: 0035 0002h.

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | <b>FREQCAPB: link B frequency capability.</b> Read only. These bits indicate that that B side of the tunnel supports 200, 400, 600, and 800 MHz link frequencies.                                                                                                                                                                                                                                                                                                                                                                               |
| 15:12 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11:8  | <b>FREQB: link B frequency.</b> Read-write. Specifies the link side B frequency. Legal values are 0h (200 MHz), and 2h (400 MHz), 4h (600 MHz), and 5h (800 MHz). Note: although it is possible to program this field for higher frequencies, the B link of the IC is only designed to support 200 and 400 MHz operation. Note: this bit is cleared by PWROK reset, not by RESET#. Note: after this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs through LDTSTOP#. |
| 7:0   | <b>Link device feature capability indicator.</b> Read only. These bits are set to indicate that the IC supports LDTSTOP#.                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Link Enumeration Scratchpad Register****DevA:0xD4**

Default: 0000 0000h.

Attribute: See below.

| Bits  | Description                                                                                                                                             |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved.                                                                                                                                               |
| 15:0  | <b>ESP: enumeration scratchpad.</b> Read-write. This field controls no hardware within the IC. Note: this bit is cleared by PWROK reset, not by RESET#. |

**Link PHY Compensation Control Registers****DevA:0x[E8, E4, E0]**

The link PHY circuitry includes automatic compensation that is used to adjust the electrical characteristics for the link transmitters and receivers on both sides of the tunnel. There is one compensation circuit for the receivers and one for each polarity of the transmitters. These registers provide visibility into the calculated output of the compensation circuits, the ability to override the calculated value with software-controlled values, and the ability to offset the calculated values with a fixed difference. The overrides and difference values may be different between sides A and B of the tunnel. These registers specify the compensation parameters as follows:

- DevA:0xE0: transmitter rising edge (P) drive strength compensation.
- DevA:0xE4: transmitter falling edge (N) drive strength compensation.
- DevA:0xE8: receiver impedance compensation.

For DevA:0x[E4, E0], higher values represent higher drive strength; the values range from 01h to 13h (19 steps). For DevA:0xE8, higher values represent lower impedance; the values range from 00h to 1Fh (32 steps).

Note: the default state of these registers is set by PWROK reset; assertion of RESET# does not alter any of the fields.

Default: See below.

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------|-----|----------------------------------------------------|-----|-------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|
| 31    | <b>Must be low.</b> Read-write. This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 30:21 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 20:16 | <b>CALCCOMP: calculated compensation value.</b> Read only. This provides the calculated value from the auto compensation circuitry. The default value of this field is not predictable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 15    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 14:13 | <p><b>BCTL: link side B PHY control value.</b> Read-write. These two bits combine to specify the PHY compensation value that is applied to side B of the tunnel as follows:</p> <table> <tr> <th>BCTL</th><th>Description</th></tr> <tr> <td>00b</td><td>Apply CALCCOMP directly as the compensation value.</td></tr> <tr> <td>01b</td><td>Apply BDATA directly as the compensation value.</td></tr> <tr> <td>10b</td><td>Apply the sum of CALCCOMP and BDATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied.</td></tr> <tr> <td>11b</td><td>Apply the difference of CALCCOMP minus BDATA as the compensation value. If the difference is less than 01h, then 01h is applied.</td></tr> </table> <p>The default value of this field (from PWROK reset) is controlled by the CMPOVR signal. If CMPOVR = 0, the default is 00b. If CMPOVR = 1, the default is 01b.</p> | BCTL | Description | 00b | Apply CALCCOMP directly as the compensation value. | 01b | Apply BDATA directly as the compensation value. | 10b | Apply the sum of CALCCOMP and BDATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied. | 11b | Apply the difference of CALCCOMP minus BDATA as the compensation value. If the difference is less than 01h, then 01h is applied. |
| BCTL  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 00b   | Apply CALCCOMP directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 01b   | Apply BDATA directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 10b   | Apply the sum of CALCCOMP and BDATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 11b   | Apply the difference of CALCCOMP minus BDATA as the compensation value. If the difference is less than 01h, then 01h is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 12:8  | <b>BDATA: link side B data value.</b> Read-write. This value is applied to the side B of the tunnel PHY compensation as described in BCTL. The default for DevA:0x[E4, E0] is 08h. The default for DevA:0xE8 is 0Fh.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 7     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |      |             |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |

| 6:5         | <p><b>ACTL: link side A PHY control value.</b> Read-write. These two bits combine to specify the PHY compensation value that is applied to side A of the tunnel as follows:</p> <table> <tr> <th><u>ACTL</u></th><th><u>Description</u></th></tr> <tr> <td>00b</td><td>Apply CALCCOMP directly as the compensation value.</td></tr> <tr> <td>01b</td><td>Apply ADATA directly as the compensation value.</td></tr> <tr> <td>10b</td><td>Apply the sum of CALCCOMP and ADATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied.</td></tr> <tr> <td>11b</td><td>Apply the difference of CALCCOMP minus ADATA as the compensation value. If the difference is less than 01h, then 01h is applied.</td></tr> </table> <p>The default value of this field (from PWROK reset) is controlled by the CMPOVR signal. If CMPOVR = 0, the default is 00b. If CMPOVR = 1, the default is 01b.</p> | <u>ACTL</u> | <u>Description</u> | 00b | Apply CALCCOMP directly as the compensation value. | 01b | Apply ADATA directly as the compensation value. | 10b | Apply the sum of CALCCOMP and ADATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied. | 11b | Apply the difference of CALCCOMP minus ADATA as the compensation value. If the difference is less than 01h, then 01h is applied. |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|-----|----------------------------------------------------|-----|-------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|
| <u>ACTL</u> | <u>Description</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 00b         | Apply CALCCOMP directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 01b         | Apply ADATA directly as the compensation value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 10b         | Apply the sum of CALCCOMP and ADATA as the compensation value. In DevA:0x[E4, E0], if the sum exceeds 13h, then 13h is applied. In DevA:0x[E8], if the sum exceeds 1Fh, then 1Fh is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 11b         | Apply the difference of CALCCOMP minus ADATA as the compensation value. If the difference is less than 01h, then 01h is applied.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |
| 4:0         | <p><b>ADATA: link side A data value.</b> Read-write. This value is applied to the side A of the tunnel PHY compensation as described in ACTL. The default for DevA:0x[E4, E0] is 08h. The default for DevA:0xE8 is 0Fh.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |             |                    |     |                                                    |     |                                                 |     |                                                                                                                                                                                              |     |                                                                                                                                  |

## Clock Control Register

DevA:0xF0

See section 4.3.1 for details on clock gating. AMD system recommendations for System Management Action Field (SMAF) codes are: 0=ACPI C2; 1=ACPI C3; 2=FID/VID change; 3=ACPI S1; 4=ACPI S3; 5=Throttling; 6=ACPI S4/S5. For server and desktop platforms, AMD recommends setting this register to 0004\_0008h (to gate clocks during S1). For mobile platforms, AMD recommends setting this register to 0004\_0A0Ah (to gate clocks during C3 and S1).

Default: 0000 0000h.

Attribute: Read-write.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 18    | <b>CGEN: clock gate enable.</b> 1=Internal clock gating, as specified by bits[7:0] of this register, is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 17    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 16    | <b>Must be low.</b> This bit is required to be low at all times; setting it high results in undefined behavior.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15:8  | <b>ECGSMAF: external clock gating system management action fields.</b> Each of the bits of this field correspond to SMAF values that are captured in Stop Grant cycles from the host. For each bit, 1=When LDTSTOP# is asserted prior to a Stop Grant cycle in which the SMAF field matches the ECGSMAF bit that is asserted, then A_PCLK and internal clock grids associated with the AGP bridges are forced low. 0=A_PCLK and the internal clock grids are active while LDTSTOP# is asserted. For example, if A_PCLK gating is required for SMAF values of 3 and 5, then ECGSMAF[3, 5] must be high. See section 4.3.1 for details. |
| 7:0   | <b>ICGSMAF: internal clock gating system management action fields.</b> Each of the bits of this field correspond to SMAF values that are captured in Stop Grant cycles from the host. For each bit, 1=When LDTSTOP# is asserted prior to a Stop Grant cycle in which the SMAF field matches the ICGSMAF bit that is asserted, then the IC power is reduced through gating of internal clocks. 0=No power reduction while LDTSTOP# is asserted. For example, if clock gating is required for SMAF values of 3 and 5, then ICGSMAF[3, 5] must be high. See section 4.3.1 for details.                                                   |

### 5.3 AGP Bridge Configuration Registers

These registers are located in PCI configuration space, in the second device (device B), function 0. See section 5.1.2 for a description of the register naming convention.

#### AGP Bridge Vendor And Device ID Register

DevB:0x00

Default: 7455 1022h

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                         |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | AGP bridge device ID. Bits[31:20] are read only; bits[19:16] are write-once. When the LSBs are left at the default value, some operating systems may load a generic graphics driver. System BIOS should program the LSBs to 6h in order to circumvent the loading of such a driver. |
| 15:0  | Vendor ID. Read only.                                                                                                                                                                                                                                                               |

#### AGP Bridge Status And Command Register

DevB:0x04

Default: 0220 0000h

Attribute: See below.

| Bits | Description                                                                                                   |
|------|---------------------------------------------------------------------------------------------------------------|
| 31:9 | Read only. These bits are fixed in their default state.                                                       |
| 8    | <b>SERREN: SERR# enable.</b> Read-write. This bit controls no hardware.                                       |
| 7:3  | <b>Special cycle enable.</b> Read only. This bit is hardwired low.                                            |
| 2    | <b>MASEN: PCI master enable.</b> Read-write. 1=Enables the AGP bus master to initiate PCI cycles to the host. |
| 1    | <b>MEMEN: memory enable.</b> Read-write. 1=Enables access to the AGP bus memory space.                        |
| 0    | <b>IOEN: IO enable.</b> Read-write. 1=Enables access to the AGP bus IO space.                                 |

#### AGP Bridge Revision and Class Code Register

DevB:0x08

Default: 0604 00??h

Attribute: Read only.

| Bits | Description       |
|------|-------------------|
| 31:8 | <b>CLASSCODE.</b> |
| 7:0  | <b>REVISION.</b>  |

#### AGP Bridge BIST-Header-Latency-Cache Register

DevB:0x0C

Default: 0001 0000h

Attribute: See below.

| Bits  | Description                                                         |
|-------|---------------------------------------------------------------------|
| 31:24 | <b>BIST.</b> Read only. These bits fixed at their default values.   |
| 23:16 | <b>HEADER.</b> Read only. These bits fixed at their default values. |

|      |                                                                    |
|------|--------------------------------------------------------------------|
| 15:8 | <b>LATENCY.</b> Read-write. These bits control no hardware.        |
| 7:0  | <b>CACHE.</b> Read only. These bits fixed at their default values. |

**AGP Bridge Bus Numbers And Secondary Latency Register****DevB:0x18**

Default: 0000 0000h

Attribute: Read-write.

| Bits  | Description                                                             |
|-------|-------------------------------------------------------------------------|
| 31:24 | <b>SECLAT.</b> Secondary latency timer. These bits control no hardware. |
| 23:16 | <b>SUBBUS.</b> Subordinate bus number.                                  |
| 15:8  | <b>SECBUS.</b> Secondary bus number.                                    |
| 7:0   | <b>PRIBUS.</b> Primary bus number.                                      |

**AGP Bridge Memory Base-Limit Registers****DevB:0x[30:1C]**

These registers specify the IO-space (DevB:0x1C and DevB:0x30), non-prefetchable memory-space (DevB:0x20), and prefetchable memory-space (DevB:0x24) address windows for transactions that are mapped from the 40-bit link address space to the AGP bus.

The links support 25 bits of IO space. AGP supports 32 bits of IO space. Host accesses to the link-defined IO region are mapped to the AGP IO window with the 7 MSB always zero. AGP IO accesses in which any of the 7 MSBs are other than zero are ignored. The AGP IO space window is defined as follow:

```
AGP IO window =
    {7'h00, DevB:30[24:16], DevB:0x1C[15:12], 12'hFFF} >= address >=
    {7'h00, DevB:30[8:0], DevB:0x1C[7:4], 12'h000};
```

The links support 40 bits of memory space. AGP supports 32 bits of non-prefetchable memory space. The AGP non-prefetchable window is defined to be within the lowest 4 gigabytes of link address space. AGP accesses above 4 gigabytes cannot access non-prefetchable memory space. The AGP non-prefetchable memory space window is defined as follows:

```
AGP non-prefetchable memory window =
    {32'h00, DevB:0x20[31:20], 20'hF_FFFF} >= address >=
    {32'h00, DevB:0x20[15:4], 20'h0_0000};
```

The links support 40 bits of memory space. AGP supports 32 bits of prefetchable memory space. The AGP prefetchable window is defined to be within the lowest 4 gigabytes of link address space. The AGP prefetchable memory space window is defined as follows:

```
AGP prefetchable memory window =
    {32'h00, DevB:0x24[31:20], 20'hF_FFFF} >= address >=
    {32'h00, DevB:0x24[15:4], 20'h0_0000};
```

These windows may also be altered by DevB:0x3C[VGAEN, ISAEN]. When the address (from either the host or from an AGP bus master) is inside one of the windows, then the transaction targets the AGP bus. Therefore, the following transactions are possible:

- Host-initiated transactions inside the windows are routed to the AGP bus.
- PCI transactions initiated on the AGP bus inside the windows are not claimed by the IC.
- Host initiated transactions outside the windows are passed through the tunnel or master aborted if the IC is at the end of a HyperTransport technology chain.
- PCI transactions initiated on the AGP bus outside the windows are claimed by the IC using medium decoding and passed to the host.

So, for example, if IOBASE > IOLIM, then no host-initiated IO-space transactions are forwarded to the AGP bus and all AGP-bus-initiated IO-space (not configuration) transactions are forwarded to the host. If MEMBASE > MEMLIM and PMEMBASE > PMEMLIM, then no host-initiated memory-space transactions are forwarded to the AGP bus and all AGP-bus-initiated memory-space (not configuration) transactions are forwarded to the host.

**DevB:0x1C.** Default: 0220 01F1h

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                   |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | Reserved.                                                                                                                                                                                                                                                                                                                                                     |
| 29    | <b>RMA: received master abort.</b> Read; set by hardware; write 1 to clear. 1=The IC received a master abort as a PCI master on the AGP bus. Note: this bit is cleared by PWROK reset but not by RESET#.                                                                                                                                                      |
| 28    | <b>RTA: received target abort.</b> Read; set by hardware; write 1 to clear. 1=The IC received a target abort as a PCI master on the AGP bus. Note: this bit is cleared by PWROK reset but not by RESET#.                                                                                                                                                      |
| 27    | <b>STA: signaled target abort.</b> Read; set by hardware; write 1 to clear. 1=The IC generated a target abort as a PCI target on the AGP bus. The IC generates target aborts if it receives a target abort (a non-NXA error) response from the host to an AGP bus PCI master transaction request. Note: this bit is cleared by PWROK reset but not by RESET#. |
| 26:16 | Read only. These bits are fixed in their default state.                                                                                                                                                                                                                                                                                                       |
| 15:12 | <b>IOLIM.</b> IO limit address bits[15:12]. See DevB:0x[30:1C] above.                                                                                                                                                                                                                                                                                         |
| 11:8  | Reserved.                                                                                                                                                                                                                                                                                                                                                     |
| 7:4   | <b>IOBASE.</b> IO base address bits[15:12]. See DevB:0x[30:1C] above.                                                                                                                                                                                                                                                                                         |
| 3:0   | Reserved.                                                                                                                                                                                                                                                                                                                                                     |

**DevB:0x20.** Default: 0000 FFF0h

Attribute: Read-write.

| Bits  | Description                                                                                 |
|-------|---------------------------------------------------------------------------------------------|
| 31:20 | <b>MEMLIM.</b> Non-prefetchable memory limit address bits[31:20]. See DevB:0x[30:1C] above. |
| 19:16 | Reserved.                                                                                   |
| 15:4  | <b>MEMBASE.</b> Non-prefetchable memory base address bits[31:20]. See DevB:0x[30:1C] above. |
| 3:0   | Reserved.                                                                                   |

**DevB:0x24.** Default: 0000 FFF0h

Attribute: Read-write.

| Bits  | Description                                                                              |
|-------|------------------------------------------------------------------------------------------|
| 31:20 | <b>PMEMLIM.</b> Prefetchable memory limit address bits[31:20]. See DevB:0x[30:1C] above. |
| 19:16 | Reserved.                                                                                |
| 15:4  | <b>PMEMBASE.</b> Prefetchable memory base address bits[31:20]. See DevB:0x[30:1C] above. |
| 3:0   | Reserved.                                                                                |

**DevB:0x30.** Default: 0000 FFFFh

Attribute: Read-write.

| Bits  | Description                                                           |
|-------|-----------------------------------------------------------------------|
| 31:16 | <b>IOLIM.</b> IO limit address bits[31:16]. See DevB:0x[30:1C] above. |
| 15:0  | <b>IOBASE.</b> IO base address bits[31:16]. See DevB:0x[30:1C] above. |

**AGP Bridge Interrupt and Bridge Control Register****DevB:0x3C**

Default: 0000 00FFh

Attribute: See below.

| Bits  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:23 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 22    | <b>SBRST: AGP bus reset.</b> Read-write. 1=A_RESET# asserted; AGP bus placed into reset state. 0=A_RESET# not asserted.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 21:20 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19    | <b>VGAEN: VGA decoding enable.</b> Read-write. 1=Host-initiated commands targeting VGA-compatible address ranges are routed to the AGP bus. These include memory accesses from A0000h to BFFFFh (within the bottom megabyte of memory space only), IO accesses in which address bits[9:0] range from 3B0h to 3BBh or 3C0h to 3DFh (address bits[15:10] are not decoded, regardless of DevB:0x3C[ISAEN]; also this only applies to the first 64K of IO space; i.e., address bits[31:16] must be low). 0=The IC does not decode VGA-compatible address ranges. |
| 18    | <b>ISAEN: ISA decoding enable.</b> Read-write. 1=The IO address window specified by DevB:0x1C[15:0] and DevB:0x30 is limited to the first 256 bytes of each 1K byte block specified; this only applies to the first 64K bytes of IO space. 0=The PCI IO window is the whole range specified by DevB:0x1C[15:0] and DevB:0x30.                                                                                                                                                                                                                                |
| 17:16 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15:8  | <b>INTERRUPT_PIN.</b> Read; write once. These bits control no internal logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0   | <b>INTERRUPT_LINE.</b> Read-write. These bits control no internal logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

## 6 Electrical Data

### 6.1 Absolute Ratings

The IC is not designed to operate beyond the parameters shown in the following table.

| Parameter                      | Minimum | Maximum | Comments |
|--------------------------------|---------|---------|----------|
| VDD12[B, A]                    | -0.5 V  | 1.7 V   |          |
| VDD15                          | -0.5 V  | 2.0 V   |          |
| VDD18, VDDA18                  | -0.5 V  | 2.3 V   |          |
| VDD33                          | -0.5 V  | 3.6 V   |          |
| T <sub>CASE</sub> (Under Bias) |         | 85 °C   |          |
| T <sub>STORAGE</sub>           | -65 °C  | 150 °C  |          |

**Table 6: Absolute maximum ratings.**

### 6.2 Operating Ranges

The IC is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in the following table.

| Parameter                      | Minimum | Typical | Maximum | Units | Comments |
|--------------------------------|---------|---------|---------|-------|----------|
| VDD12[B, A]                    | 1.14    | 1.2     | 1.26    | V     |          |
| VDD15                          | 1.425   | 1.5     | 1.575   | V     |          |
| VDD18, VDDA18                  | 1.71    | 1.8     | 1.89    | V     |          |
| VDD33                          | 3.135   | 3.3     | 3.465 V | V     |          |
| T <sub>CASE</sub> (Under Bias) |         |         | 85      | deg C |          |

**Table 7: Operating ranges.**

### 6.3 DC Characteristics

See the HyperTransport™ Technology Electrical Specification for the DC characteristics of link signals.

The following table shows current consumption in amps and power in watts for each power plane.

| Supply | Parameter Description                                                                   | Typical |        | Max     |        | Comments |
|--------|-----------------------------------------------------------------------------------------|---------|--------|---------|--------|----------|
|        |                                                                                         | Current | Power  | Current | Power  |          |
| VDD12  | VDD12[B, A] current, power                                                              | 0.21 A  | 0.25 W | 0.27 A  | 0.34 W |          |
| VDD15  | VDD15 current, power                                                                    | 0.05 A  | 0.08 W | 0.08 A  | 0.13 W |          |
| VDD18  | VDD18 current, power; operational                                                       | 1.30 A  | 2.34 W | 1.75 A  | 3.30 W |          |
| VDD18  | VDD18 current, power; internal clock gating enabled (DevA:0xF0[ICGSMAF])                | 0.40 A  | 0.72 W | 0.50 A  | 0.95 W |          |
| VDD18  | VDD18 current, power; internal and external clock gating enabled (DevA:0xF0[I/ECGSMAF]) | 0.21 A  | 0.38 W | 0.30 A  | 0.57 W |          |
| VDDA18 | VDDA18 current, power                                                                   | 0.02 A  | 0.04 W | 0.03 A  | 0.06 W |          |
| VDD33  | VDD33 current, power                                                                    | 0.05 A  | 0.17 W | 0.07 A  | 0.24 W |          |
|        | Total power (no clock gating enabled)                                                   |         | 2.88 W |         | 4.07 W |          |

**Table 8: Current and power consumption.**

The following table shows DC characteristics for signals on the VDD33 power plane.

| Symbol          | Parameter Description                           | Min       | Max         | Units | Comments |
|-----------------|-------------------------------------------------|-----------|-------------|-------|----------|
| V <sub>IL</sub> | Input low voltage                               | -0.5      | 0.3 VDD33   | V     |          |
| V <sub>IH</sub> | Input high voltage                              | 0.6 VDD33 | 0.5 + VDD33 | V     |          |
| V <sub>OL</sub> | Output low voltage; I <sub>OUT</sub> = 1.5 mA   |           | 0.1 VDD33   | V     |          |
| V <sub>OH</sub> | Output high voltage; I <sub>OUT</sub> = -0.5 mA | 0.9 VDD33 |             | V     |          |
| I <sub>LI</sub> | Input leakage current                           |           | +/- 10      | uA    |          |
| C <sub>IN</sub> | Input capacitance                               |           | 8           | pF    |          |

**Table 9: DC characteristics for signals on the VDD33 power plane.**

The following table shows DC characteristics for signals on the VDD15 power plane when AGP 2.0 signaling is enabled.

| Symbol            | Parameter Description                          | Min        | Max         | Units | Comments |
|-------------------|------------------------------------------------|------------|-------------|-------|----------|
| V <sub>IL</sub>   | Input low voltage                              | -0.5       | 0.4 VDD15   | V     |          |
| V <sub>IH</sub>   | Input high voltage                             | 0.6 VDD15  | 0.5 + VDD15 | V     |          |
| V <sub>OL</sub>   | Output low voltage; I <sub>OUT</sub> = 1.0 mA  |            | 0.15 VDD15  | V     |          |
| V <sub>OH</sub>   | Output high voltage; I <sub>OUT</sub> = 0.2 mA | 0.85 VDD15 |             | V     |          |
| V <sub>REFI</sub> | Input reference voltage on A_REFGC             | 0.48 VDD15 | 0.52 VDD15  | V     |          |
| V <sub>REFO</sub> | Output reference voltage on A_REFCG            | 0.48 VDD15 | 0.52 VDD15  | V     |          |
| I <sub>IL</sub>   | Input leakage current                          |            | +/- 10      | uA    |          |
| C <sub>IN</sub>   | Input capacitance                              |            | 8           | pF    |          |

**Table 10: DC characteristics for signals on the VDD15 power plane, AGP 2.0 signaling.**

The following table shows DC characteristics for signals on the VDD15 power plane when AGP 3.0 signaling is enabled.

| Symbol            | Parameter Description                                                               | Min                     | Max                     | Units | Comments |
|-------------------|-------------------------------------------------------------------------------------|-------------------------|-------------------------|-------|----------|
| V <sub>IL</sub>   | Input low voltage                                                                   | -0.3                    | V <sub>REFI</sub> - 0.1 | V     |          |
| V <sub>IH</sub>   | Input high voltage                                                                  | V <sub>REFI</sub> + 0.1 | VDD15 + 0.3             | V     |          |
| V <sub>OL</sub>   | Output low voltage; I <sub>OUT</sub> = 1.5 mA                                       |                         | 0.05                    | V     |          |
| V <sub>OH</sub>   | Output high voltage; 50 ohm load to ground                                          | 0.750                   | 0.850                   | V     |          |
| V <sub>REFI</sub> | Input reference voltage on A_REFGC                                                  | 0.34                    | 0.36                    | V     |          |
| V <sub>REFO</sub> | Output reference voltage on A_REFCG                                                 | 0.226 VDD15             | 0.240 VDD15             | V     |          |
| C <sub>DIE</sub>  | Input die capacitance                                                               |                         | 8                       | pF    |          |
| Z <sub>TERM</sub> | Terminator equivalent impedance; V <sub>OH</sub> = 0.8V; Z <sub>TARG</sub> = 50 Ohm | 45                      | 55                      | Ohms  |          |
| Z <sub>PU</sub>   | Pull-up equivalent impedance; V <sub>OH</sub> = 0.8V; Z <sub>TARG</sub> = 50 Ohm    | 39.3                    | 46.2                    | Ohms  |          |

**Table 11: DC characteristics for signals on the VDD15 power plane, AGP 3.0 signaling.**

## 6.4 AC Characteristics

See the HyperTransport Technology Electrical Specification for the AC characteristics of link signals.

The following table shows AC specification data for clocks.

| Symbol            | Parameter Description | Min | Max | Units | Comments       |
|-------------------|-----------------------|-----|-----|-------|----------------|
| t <sub>REF</sub>  | REFCLK cycle time     | 15  | 18  | ns    |                |
| t <sub>CYC</sub>  | A_PCLK cycle time     | 15  |     | ns    | Matches REFCLK |
| t <sub>HIGH</sub> | A_PCLK high time      | 6   |     | ns    |                |
| t <sub>LOW</sub>  | A_PCLK low time       | 6   |     | ns    |                |
| t <sub>SLEW</sub> | A_PCLK slew rate      | 1   | 4   | V/ns  |                |

**Table 12: AC data for clocks.**

The following table shows AC specification data for common clock (A\_PCLK) operation of AGP signals.

| Symbol           | Parameter Description                   | Min | Max | Units | Notes |
|------------------|-----------------------------------------|-----|-----|-------|-------|
| t <sub>VAL</sub> | A_PCLK to signal valid delay            | 1   | 5.5 | ns    |       |
| t <sub>ON</sub>  | A_PCLK to signal float-to-active delay  | 1   | 6   | ns    |       |
| t <sub>OFF</sub> | A_PCLK to signal active-to-float delay  | 1   | 14  | ns    |       |
| t <sub>SU</sub>  | Signal input setup time to A_PCLK       | 6   |     | ns    |       |
| t <sub>H</sub>   | AGP signal input hold time after A_PCLK | 0   |     | ns    |       |
| t <sub>RF</sub>  | Signal output rise and fall slew rate   | 2   | 3.5 | V/ns  |       |

**Table 13: AC data for common clock operation of AGP signals.**

The following table shows AC specification data for clock-forwarded operation of AGP signals.

| Symbol            | Parameter Description                                         | AGP 2X |     | AGP 4X |     | AGP 8X |      | Units | Notes |
|-------------------|---------------------------------------------------------------|--------|-----|--------|-----|--------|------|-------|-------|
|                   |                                                               | Min    | Max | Min    | Max | Min    | Max  |       |       |
| t <sub>TSF</sub>  | A_PCLK to transmit strobe first strobe edge                   | 2      | 12  | 1.9    | 8   | 1.5    |      | ns    |       |
| t <sub>TSR</sub>  | A_PCLK to transmit strobe final strobe edge                   |        | 20  |        | 20  |        | 19.5 | ns    |       |
| t <sub>DVB</sub>  | Data valid before strobe                                      | 1.7    |     | -0.95  |     | 0.527  |      | ns    |       |
| t <sub>DVA</sub>  | Data valid after strobe                                       | 1.9    |     | 1.15   |     | 0.477  |      | ns    |       |
| t <sub>OND</sub>  | A_PCLK to float-to-active delay                               | -1     | 9   | -1     | 7   | -1     | 7    | ns    |       |
| t <sub>OFFD</sub> | A_PCLK to active-to-float delay                               | 1      | 12  | 1      | 14  | 1      | 14   | ns    |       |
| t <sub>ONS</sub>  | Strobe active to first edge delay                             | 6      | 10  | 4      | 9   | 4      | 9    | ns    |       |
| t <sub>OFFS</sub> | Strobe final edge to float delay                              | 6      | 10  | 4      | 9   | 4      | 9    | ns    |       |
| t <sub>RSSU</sub> | Receive requirement for last strobe setup time to next A_PCLK | 6      |     | 6      |     | 6      |      | ns    |       |
| t <sub>RSH</sub>  | Receive requirement for first strobe hold time after A_PCLK   | 1      |     | 0.5    |     | 0.5    |      | ns    |       |
| t <sub>DSU</sub>  | Receive data setup time to strobe                             | 1      |     | 0.4    |     | 0.085  |      | ns    |       |
| t <sub>DH</sub>   | Receive data hold time after strobe                           | 1      |     | 0.7    |     | 0.210  |      | ns    |       |
| t <sub>RF</sub>   | Transmit rise and fall slew rate                              | 2      | 3.5 | 2      | 3.5 | 2      | 3.5  | V/ns  |       |

**Table 14: AC data for clock-forwarded operation of AGP signals.**

## 7 Ball Designations

|    | 1           | 2           | 3         | 4           | 5          | 6          | 7          | 8          | 9          | 10          | 11          | 12        | 13         | 14         | 15         | 16         | 17         | 18        | 19          | 20         | 21        | 22        | 23        | 24        |    |
|----|-------------|-------------|-----------|-------------|------------|------------|------------|------------|------------|-------------|-------------|-----------|------------|------------|------------|------------|------------|-----------|-------------|------------|-----------|-----------|-----------|-----------|----|
| A  |             |             | LTACAD_P0 | LTACAD_N0   | LTACAD_P2  | LTACAD_N2  | LTACLK0_P  | LTACLK0_N  | LTACAD_P5  | LTACAD_N5   | LTACAD_P7   | LTACAD_N7 | LRACLK0_P  | LRACLK0_N  | LRACAD_P6  | LRACAD_N6  | LRACAD_P4  | LRACAD_N4 | LRACAD_P3   | LRACAD_N3  | LRACAD_P1 | LRACAD_N1 |           |           | A  |
| B  |             | VDD12A      | VSS       | LTACAD_P1   | VDD18      | LTACAD_P3  | VSS        | LTACAD_P4  | VDD18      | LTACAD_P6   | VSS         | LTACTL_P  | VDD18      | LRACAD_N7  | VSS        | LRACAD_N5  | VDD18      | LRACLK0_N | VSS         | LRACAD_N2  | VDD18     | LRACAD_N0 | VDD12A    |           | B  |
| C  | VDD12A      | VSS         | LTACAD_N8 | LTACAD_N1   | LTACAD_N10 | LTACAD_N3  | LTACLK1_N  | LTACAD_N4  | LTACAD_N13 | LTACAD_N6   | LTACAD_N15  | LTACTL_N  | FREE4      | LRACAD_P7  | LRACAD_P14 | LRACAD_P5  | LRACAD_P12 | LRACLK0_P | LRACAD_P11  | LRACAD_P2  | LRACAD_P9 | LRACAD_P0 | VSS       | VDD12A    | C  |
| D  | VSS         | VDD12A      | LTACAD_P8 | VDD18       | LTACAD_P10 | VSS        | LTACLK1_P  | VDD18      | LTACAD_P13 | VSS         | LTACAD_P15  | VDD18     | FREE5      | VSS        | LRACAD_N14 | VDD18      | LRACAD_N12 | VSS       | LRACAD_N11  | VDD18      | LRACAD_N9 | VSS       | VSS       | VDD12A    | D  |
| E  | VDD12A      | VSS         | LTACAD_P9 | LTACAD_N9   | LTACAD_P11 | LTACAD_N11 | LTACAD_P12 | LTACAD_N12 | LTACAD_P14 | LTACAD_N14  | FREE7       | FREE6     | LRACAD_N15 | LRACAD_P15 | LRACAD_N13 | LRACAD_P13 | LRACLK1_N  | LRACLK1_P | LRACAD_N10  | LRACAD_P10 | LRACAD_N8 | LRACAD_P8 | VDD12A    | VSS       | E  |
| F  | A_DB1H      | VDD12A      | VSS       | VDD12A      | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD18       | VSS         | VDD18     | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD18     | VSS         | VDD18      | VSS       | VDD12A    | VSS       | VDD12B    | F  |
| G  | A_SBA0      | A_DB1L      | VDD12A    | VDD12A      | VDD12A     | VSS        | VDD18      | VSS        | VDD18      | VSS         | VDD18       | VSS       | VDD18      | VSS        | VDD18      | VSS        | VDD18      | VSS       | VDD18       | VSS        | VDD12A    | VSS       | VDD12B    | VDD12B    | G  |
| H  | A_SBA2      | A_SBA1      | STRAPL0   | VDD15       | VSS        | VDD12A     | VSS        | VDD18      | VSS        | VDD18       | VSS         | VDD18     | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD12A    | VDD12A      | VDD12A     | VSS       | VDD12B    | VSS       | VSS       | H  |
| J  | A_SBA3      | VSS         | STRAPL10  | STRAPL1     | STRAPL8    | VSS        | VDD12A     | VDD12A     | VDD12A     | VSS         | VDD18       | VSS       | VDD18      | VSS        | VDD18      | VSS        | VDD12A     | VSS       | VDD12B      | VDD12B     | VDD12B    | VSS       | VDD18     | LTBCAD_P0 | J  |
| K  | A_SB_STB_P  | A_SB_STB_N  | FREE1     | A_GC8X_DET# | VSS        | VDD15      | VSS        | VDD15      | VSS        | VDD18       | VSS         | VDD18     | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD12B    | VSS         | VSS        | VDD18     | LTBCAD_N1 | LTBCAD_P1 | LTBCAD_N0 | K  |
| L  | A_SBA5      | A_SBA4      | VSS       | A_GNT#      | STRAPL9    | VSS        | VDD15      | VSS        | VDD15      | VSS         | VDD18       | VSS       | VDD18      | VSS        | VDD18      | VSS        | VDD18      | VSS       | VDD18       | LTBCAD_P5  | LTBCAD_P4 | LTBCAD_N4 | VSS       | LTBCAD_P2 | L  |
| M  | A_SBA6      | VSS         | STRAPL11  | VDD15       | VSS        | VDD15      | VSS        | VDD15      | VSS        | VDD18       | VSS         | VDD18     | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD18     | VSS         | LTBCAD_N5  | VSS       | LTBCAD_N3 | LTBCAD_P3 | LTBCAD_N2 | M  |
| N  | A_AD31      | A_SBA7      | NC1       | A_REQ#      | VSS        | VSS        | VDD15      | VSS        | VDD15      | VSS         | VDD18       | VSS       | VDD18      | VSS        | VDD18      | VSS        | VDD18      | VSS       | VDD18       | LTBCAD_P7  | LTBCAD_P6 | LTBCAD_N6 | VDD18     | LTBCLK0_P | N  |
| P  | A_AD29      | A_AD30      | VSS       | STRAPL13    | STRAPL7    | VDD15      | VSS        | VDD15      | VSS        | VDD18       | VSS         | VDD18     | VSS        | VDD18      | VSS        | VDD18      | VSS        | VDD18     | VSS         | LTBCAD_N7  | VDD18     | LTBCTL_P  | LTBCTL_P  | LTBCLK0_P | P  |
| R  | A_AD28      | VSS         | FREE2     | VDD15       | VSS        | VSS        | VDD15      | VSS        | VDD15      | VSS         | VDD18       | VSS       | VDD18      | VSS        | VDD18      | VSS        | VDD18      | VSS       | VDD18       | LRBCAD_N6  | LRBCAD_N7 | LRBCAD_P7 | VSS       | LRBCTL_N  | R  |
| T  | A_AD26      | A_AD27      | FREE3     | A_ST0       | VSS        | VDD15      | VSS        | VDD15      | VSS        | VDD15       | VSS         | VDD15     | VSS        | VDD15      | VSS        | VDD12B     | VSS        | VDD18     | VSS         | LRBCAD_P6  | VSS       | LRBCLK0_P | LRBCLK0_N | LRBCTL_P  | T  |
| U  | A_AD25      | A_AD24      | VSS       | A_ST1       | VSS        | VSS        | VDD15      | VSS        | VDD15      | VSS         | VDD15       | VSS       | VDD15      | VSS        | VSS        | VDD12B     | VDD18      | VSS       | VDD18       | LRBCAD_N4  | LRBCAD_N5 | LRBCAD_P5 | VDD18     | LRBCAD_N3 | U  |
| V  | A_AD_STB1_P | VSS         | A_ST2     | VDD15       | VSS        | VDD15      | VSS        | VDD15      | VSS        | VDD15       | VSS         | VDD15     | VSS        | VDD15      | VSS        | VDD12B     | VSS        | VDD18     | VSS         | LRBCAD_P4  | VDD18     | LRBCAD_P2 | LRBCAD_N2 | LRBCAD_P3 | V  |
| W  | A_AD23      | A_AD_STB1_N | A_CBE_L3  | A_MB8X_DET# | VSS        | VSS        | VDD15      | VSS        | VDD15      | VSS         | VDD15       | VSS       | VDD15      | VSS        | VDD15      | VSS        | VDD12B     | VSS       | VDD18       | LDTCOM_P0  | LDTCOM_P1 | LDTCOM_P2 | VSS       | LRBCAD_N1 | W  |
| Y  | A_AD21      | A_AD22      | VSS       | NC0         | A_RBF#     | VSS        | A_CALS     | STRAPL5    | STRAPL6    | VSS         | STRAPL4     | STRAPL18  | STRAPL19   | VDD15      | STRAPL20   | STRAPL21   | VSS        | VDD12B    | VSS         | LDTCOM_P3  | VSS       | LRBCAD_P0 | LRBCAD_N0 | LRBCAD_P1 | Y  |
| AA | A_AD20      | VSS         | STRAPL14  | VDD15       | A_WBF#     | A_CALD     | VDD15      | A_CALS#    | A_FRAME#   | VDD15       | A_STOP#     | A_PAR     | VDD15      | STRAPL3    | A_PLL_CLKO | STRAPL22   | TEST       | VSS       | VDD12B      | VSS        | VDD12B    | VSS       | VDD12B    | VSS       | AA |
| AB | A_AD19      | A_AD17      | A_AD18    | STRAPL15    | VSS        | A_CALD#    | STRAPL16   | A_IRDY#    | A_DEVS_EL# | A_TRDY#     | VSS         | A_AD5     | STRAPL2    | VSS        | A_PLL_CLKI | REFCLK     | VSS        | RESET#    | VSS         | VDD12B     | VDD12B    | VDD12B    | VSS       | VDD12B    | AB |
| AC |             | VSS         | A_AD16    | VSS         | A_CBE_L1   | A_AD14     | VSS        | A_AD12     | A_AD9      | VSS         | A_AD_STB0_P | A_AD6     | VSS        | A_AD2      | A_AD1      | VSS        | CMP_OVR    | LDT_STOP# | A_PCLK      | VSS        | VDD33     | VSS       | VDD12B    |           | AC |
| AD |             | A_CBE_L2    | STRAPL17  | A_AD15      | A_AD13     | A_AD11     | A_AD10     | A_AD8      | A_CBE_L0   | A_AD_STB0_N | A_AD7       | A_AD4     | A_AD3      | A_AD0      | A_REF_GC   | A_REF.CG   | PWROK      | A_RESET#  | A_TYPE_DET# | VDD33      | VDDA18    |           |           |           | AD |
|    | 1           | 2           | 3         | 4           | 5          | 6          | 7          | 8          | 9          | 10          | 11          | 12        | 13         | 14         | 15         | 16         | 17         | 18        | 19          | 20         | 21        | 22        | 23        | 24        |    |

Top side view.

Figure 3: Ball designations.

Alphabetical listing of signals and corresponding BGA designators.

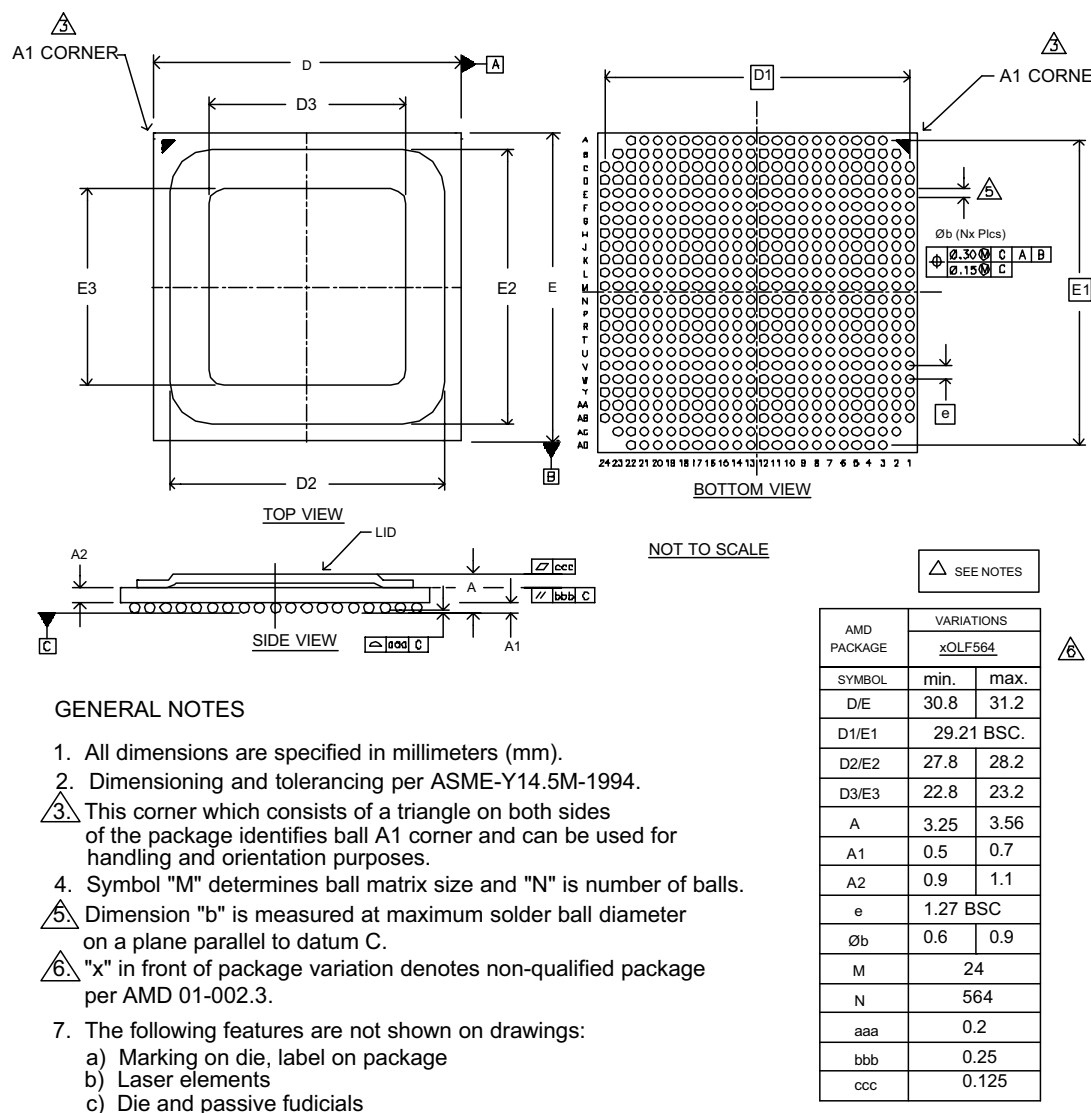
| Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball |
|-------------|------|-------------|------|-------------|------|-------------|------|-------------|------|
| A_AD0       | 15AD | A_PAR       | 12AA | LRACAD_N13  | 15E  | LTACAD_N7   | 12A  | NC1         | 3N   |
| A_AD1       | 15AC | A_PCLK      | 19AC | LRACAD_N14  | 15D  | LTACAD_N8   | 3C   | PWROK       | 18AD |
| A_AD2       | 14AC | A_PLLCLKI   | 15AB | LRACAD_N15  | 13E  | LTACAD_N9   | 4E   | REFCLK      | 16AB |
| A_AD3       | 14AD | A_PLLCLKO   | 15AA | LRACAD_P0   | 22C  | LTACAD_N10  | 5C   | RESET#      | 18AB |
| A_AD4       | 13AD | A_RBF#      | 5Y   | LRACAD_P1   | 22A  | LTACAD_N11  | 6E   | STRAPL0     | 3H   |
| A_AD5       | 12AB | A_REFCG     | 17AD | LRACAD_P2   | 20C  | LTACAD_N12  | 8E   | STRAPL1     | 4J   |
| A_AD6       | 12AC | A_REFGC     | 16AD | LRACAD_P3   | 20A  | LTACAD_N13  | 9C   | STRAPL2     | 13AB |
| A_AD7       | 12AD | A_REQ#      | 4N   | LRACAD_P4   | 18A  | LTACAD_N14  | 10E  | STRAPL3     | 14AA |
| A_AD8       | 9AD  | A_RESET#    | 19AD | LRACAD_P5   | 16C  | LTACAD_N15  | 11C  | STRAPL4     | 11Y  |
| A_AD9       | 9AC  | A_SBA0      | 1G   | LRACAD_P6   | 16A  | LTACAD_P0   | 3A   | STRAPL5     | 8Y   |
| A_AD10      | 8AD  | A_SBA1      | 2H   | LRACAD_P7   | 14C  | LTACAD_P1   | 4B   | STRAPL6     | 9Y   |
| A_AD11      | 7AD  | A_SBA2      | 1H   | LRACAD_P8   | 22E  | LTACAD_P2   | 5A   | STRAPL7     | 5P   |
| A_AD12      | 8AC  | A_SBA3      | 1J   | LRACAD_P9   | 21C  | LTACAD_P3   | 6B   | STRAPL8     | 5J   |
| A_AD13      | 6AD  | A_SBA4      | 2L   | LRACAD_P10  | 20E  | LTACAD_P4   | 8B   | STRAPL9     | 5L   |
| A_AD14      | 6AC  | A_SBA5      | 1L   | LRACAD_P11  | 19C  | LTACAD_P5   | 9A   | STRAPL10    | 3J   |
| A_AD15      | 5AD  | A_SBA6      | 1M   | LRACAD_P12  | 17C  | LTACAD_P6   | 10B  | STRAPL11    | 3M   |
| A_AD16      | 3AC  | A_SBA7      | 2N   | LRACAD_P13  | 16E  | LTACAD_P7   | 11A  | STRAPL13    | 4P   |
| A_AD17      | 2AB  | A_SBSTB_N   | 2K   | LRACAD_P14  | 15C  | LTACAD_P8   | 3D   | STRAPL14    | 3AA  |
| A_AD18      | 3AB  | A_SBSTB_P   | 1K   | LRACAD_P15  | 14E  | LTACAD_P9   | 3E   | STRAPL15    | 4AB  |
| A_AD19      | 1AB  | A_ST0       | 4T   | LRACLK0_N   | 18B  | LTACAD_P10  | 5D   | STRAPL16    | 7AB  |
| A_AD20      | 1AA  | A_ST1       | 4U   | LRACLK0_P   | 18C  | LTACAD_P11  | 5E   | STRAPL17    | 4AD  |
| A_AD21      | 1Y   | A_ST2       | 3V   | LRACLK1_N   | 17E  | LTACAD_P12  | 7E   | STRAPL18    | 12Y  |
| A_AD22      | 2Y   | A_STOP#     | 11AA | LRACLK1_P   | 18E  | LTACAD_P13  | 9D   | STRAPL19    | 13Y  |
| A_AD23      | 1W   | A_TRDY#     | 10AB | LRACCTL_N   | 13A  | LTACAD_P14  | 9E   | STRAPL20    | 15Y  |
| A_AD24      | 2U   | A_TYPEDET#  | 20AD | LRACCTL_P   | 14A  | LTACAD_P15  | 11D  | STRAPL21    | 16Y  |
| A_AD25      | 1U   | A_WBF#      | 5AA  | LRBCAD_N0   | 23Y  | LTACLK0_N   | 8A   | STRAPL22    | 16AA |
| A_AD26      | 1T   | CMPOVR      | 17AC | LRBCAD_N1   | 24W  | LTACLK0_P   | 7A   | TEST        | 17AA |
| A_AD27      | 2T   | FREE1       | 3K   | LRBCAD_N2   | 23V  | LTACLK1_N   | 7C   |             |      |
| A_AD28      | 1R   | FREE2       | 3R   | LRBCAD_N3   | 24U  | LTACLK1_P   | 7D   |             |      |
| A_AD29      | 1P   | FREE3       | 3T   | LRBCAD_N4   | 20U  | LTACTL_N    | 12C  |             |      |
| A_AD30      | 2P   | FREE4       | 13C  | LRBCAD_N5   | 21U  | LTACTL_P    | 12B  |             |      |
| A_AD31      | 1N   | FREE5       | 13D  | LRBCAD_N6   | 20R  | LTBCAD_N0   | 24K  |             |      |
| A_ADSTB0_N  | 11AD | FREE6       | 12E  | LRBCAD_N7   | 21R  | LTBCAD_N1   | 22K  |             |      |
| A_ADSTB0_P  | 11AC | FREE7       | 11E  | LRBCAD_P0   | 22Y  | LTBCAD_N2   | 24M  |             |      |
| A_ADSTB1_N  | 2W   | LDTCOMP0    | 20W  | LRBCAD_P1   | 24Y  | LTBCAD_N3   | 22M  |             |      |
| A_ADSTB1_P  | 1V   | LDTCOMP1    | 21W  | LRBCAD_P2   | 22V  | LTBCAD_N4   | 22L  |             |      |
| A_CALD      | 6AA  | LDTCOMP2    | 22W  | LRBCAD_P3   | 24V  | LTBCAD_N5   | 20M  |             |      |
| A_CALD#     | 6AB  | LDTCOMP3    | 20Y  | LRBCAD_P4   | 20V  | LTBCAD_N6   | 22N  |             |      |
| A_CALS      | 7Y   | LDTSTOP#    | 18AC | LRBCAD_P5   | 22U  | LTBCAD_N7   | 20P  |             |      |
| A_CALS#     | 8AA  | LRACAD_N0   | 22B  | LRBCAD_P6   | 20T  | LTBCAD_P0   | 24J  |             |      |
| A_CBE_L0    | 10AD | LRACAD_N1   | 21A  | LRBCAD_P7   | 22R  | LTBCAD_P1   | 23K  |             |      |
| A_CBE_L1    | 5AC  | LRACAD_N2   | 20B  | LRBCLK0_N   | 23T  | LTBCAD_P2   | 24L  |             |      |
| A_CBE_L2    | 3AD  | LRACAD_N3   | 19A  | LRBCLK0_P   | 22T  | LTBCAD_P3   | 23M  |             |      |
| A_CBE_L3    | 3W   | LRACAD_N4   | 17A  | LRBCTL_N    | 24R  | LTBCAD_P4   | 21L  |             |      |
| A_DBIH      | 1F   | LRACAD_N5   | 16B  | LRBCTL_P    | 24T  | LTBCAD_P5   | 20L  |             |      |
| A_DBIL      | 2G   | LRACAD_N6   | 15A  | LTACAD_N0   | 4A   | LTBCAD_P6   | 21N  |             |      |
| A_DEVSEL#   | 9AB  | LRACAD_N7   | 14B  | LTACAD_N1   | 4C   | LTBCAD_P7   | 20N  |             |      |
| A_FRAME#    | 9AA  | LRACAD_N8   | 21E  | LTACAD_N2   | 6A   | LTBCLK0_N   | 24P  |             |      |
| A_GC8XDET#  | 4K   | LRACAD_N9   | 21D  | LTACAD_N3   | 6C   | LTBCLK0_P   | 24N  |             |      |
| A_GNT#      | 4L   | LRACAD_N10  | 19E  | LTACAD_N4   | 8C   | LTBCTL_N    | 22P  |             |      |
| A_IRDY#     | 8AB  | LRACAD_N11  | 19D  | LTACAD_N5   | 10A  | LTBCTL_P    | 23P  |             |      |
| A_MB8XDET#  | 4W   | LRACAD_N12  | 17D  | LTACAD_N6   | 10C  | NC0         | 4Y   |             |      |

**Table 15: Signal BGA positions.**

| Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball | Signal name | Ball |
|-------------|------|-------------|------|-------------|------|-------------|------|-------------|------|-------------|------|-------------|------|
| VDD12A      | 1C   | VDD15       | 6T   | VDD18       | 12F  | VDD18       | 23U  | VSS         | 8R   | VSS         | 14AB | VSS         | 21Y  |
| VDD12A      | 1E   | VDD15       | 6V   | VDD18       | 12H  | VDD33       | 21AC | VSS         | 8U   | VSS         | 15B  | VSS         | 22D  |
| VDD12A      | 2B   | VDD15       | 7L   | VDD18       | 12K  | VDD33       | 21AD | VSS         | 8W   | VSS         | 15F  | VSS         | 22G  |
| VDD12A      | 2D   | VDD15       | 7N   | VDD18       | 12M  | VDDA18      | 22AD | VSS         | 9F   | VSS         | 15H  | VSS         | 22J  |
| VDD12A      | 2F   | VDD15       | 7R   | VDD18       | 12P  | VSS         | 1D   | VSS         | 9H   | VSS         | 15K  | VSS         | 22AA |
| VDD12A      | 3G   | VDD15       | 7U   | VDD18       | 13B  | VSS         | 2C   | VSS         | 9K   | VSS         | 15M  | VSS         | 22AC |
| VDD12A      | 4F   | VDD15       | 7W   | VDD18       | 13G  | VSS         | 2E   | VSS         | 9M   | VSS         | 15P  | VSS         | 23C  |
| VDD12A      | 4G   | VDD15       | 7AA  | VDD18       | 13J  | VSS         | 2J   | VSS         | 9P   | VSS         | 15T  | VSS         | 23D  |
| VDD12A      | 5G   | VDD15       | 8K   | VDD18       | 13L  | VSS         | 2M   | VSS         | 9T   | VSS         | 15U  | VSS         | 23F  |
| VDD12A      | 6H   | VDD15       | 8M   | VDD18       | 13N  | VSS         | 2R   | VSS         | 9V   | VSS         | 15V  | VSS         | 23H  |
| VDD12A      | 7J   | VDD15       | 8P   | VDD18       | 13R  | VSS         | 2V   | VSS         | 10D  | VSS         | 16G  | VSS         | 23L  |
| VDD12A      | 8J   | VDD15       | 8T   | VDD18       | 14F  | VSS         | 2AA  | VSS         | 10G  | VSS         | 16J  | VSS         | 23R  |
| VDD12A      | 9J   | VDD15       | 8V   | VDD18       | 14H  | VSS         | 2AC  | VSS         | 10J  | VSS         | 16L  | VSS         | 23W  |
| VDD12A      | 17J  | VDD15       | 9L   | VDD18       | 14K  | VSS         | 3B   | VSS         | 10L  | VSS         | 16N  | VSS         | 23AB |
| VDD12A      | 18H  | VDD15       | 9N   | VDD18       | 14M  | VSS         | 3F   | VSS         | 10N  | VSS         | 16R  | VSS         | 24E  |
| VDD12A      | 19H  | VDD15       | 9R   | VDD18       | 14P  | VSS         | 3L   | VSS         | 10R  | VSS         | 16W  | VSS         | 24H  |
| VDD12A      | 20H  | VDD15       | 9U   | VDD18       | 15G  | VSS         | 3P   | VSS         | 10U  | VSS         | 16AC | VSS         | 24AA |
| VDD12A      | 21G  | VDD15       | 9W   | VDD18       | 15J  | VSS         | 3U   | VSS         | 10W  | VSS         | 17F  |             |      |
| VDD12A      | 22F  | VDD15       | 10T  | VDD18       | 15L  | VSS         | 3Y   | VSS         | 10Y  | VSS         | 17H  |             |      |
| VDD12A      | 23B  | VDD15       | 10V  | VDD18       | 15N  | VSS         | 4AC  | VSS         | 10AC | VSS         | 17K  |             |      |
| VDD12A      | 23E  | VDD15       | 10AA | VDD18       | 15R  | VSS         | 5F   | VSS         | 11B  | VSS         | 17M  |             |      |
| VDD12A      | 24C  | VDD15       | 11U  | VDD18       | 16D  | VSS         | 5H   | VSS         | 11F  | VSS         | 17P  |             |      |
| VDD12A      | 24D  | VDD15       | 11W  | VDD18       | 16F  | VSS         | 5K   | VSS         | 11H  | VSS         | 17T  |             |      |
| VDD12B      | 16T  | VDD15       | 12T  | VDD18       | 16H  | VSS         | 5M   | VSS         | 11K  | VSS         | 17V  |             |      |
| VDD12B      | 16U  | VDD15       | 12V  | VDD18       | 16K  | VSS         | 5N   | VSS         | 11M  | VSS         | 17Y  |             |      |
| VDD12B      | 16V  | VDD15       | 13U  | VDD18       | 16M  | VSS         | 5R   | VSS         | 11P  | VSS         | 17AB |             |      |
| VDD12B      | 17W  | VDD15       | 13W  | VDD18       | 16P  | VSS         | 5T   | VSS         | 11T  | VSS         | 18D  |             |      |
| VDD12B      | 18K  | VDD15       | 13AA | VDD18       | 17B  | VSS         | 5U   | VSS         | 11V  | VSS         | 18G  |             |      |
| VDD12B      | 18Y  | VDD15       | 14T  | VDD18       | 17G  | VSS         | 5V   | VSS         | 11AB | VSS         | 18J  |             |      |
| VDD12B      | 19J  | VDD15       | 14V  | VDD18       | 17L  | VSS         | 5W   | VSS         | 12G  | VSS         | 18L  |             |      |
| VDD12B      | 19AA | VDD15       | 14Y  | VDD18       | 17N  | VSS         | 5AB  | VSS         | 12J  | VSS         | 18N  |             |      |
| VDD12B      | 20J  | VDD15       | 15W  | VDD18       | 17R  | VSS         | 6D   | VSS         | 12L  | VSS         | 18R  |             |      |
| VDD12B      | 20AB | VDD18       | 4D   | VDD18       | 17U  | VSS         | 6G   | VSS         | 12N  | VSS         | 18U  |             |      |
| VDD12B      | 21J  | VDD18       | 5B   | VDD18       | 18F  | VSS         | 6J   | VSS         | 12R  | VSS         | 18W  |             |      |
| VDD12B      | 21AA | VDD18       | 6F   | VDD18       | 18M  | VSS         | 6L   | VSS         | 12U  | VSS         | 18AA |             |      |
| VDD12B      | 21AB | VDD18       | 7G   | VDD18       | 18P  | VSS         | 6N   | VSS         | 12W  | VSS         | 19B  |             |      |
| VDD12B      | 22H  | VDD18       | 8D   | VDD18       | 18T  | VSS         | 6R   | VSS         | 13F  | VSS         | 19F  |             |      |
| VDD12B      | 22AB | VDD18       | 8F   | VDD18       | 18V  | VSS         | 6U   | VSS         | 13H  | VSS         | 19K  |             |      |
| VDD12B      | 23G  | VDD18       | 8H   | VDD18       | 19G  | VSS         | 6W   | VSS         | 13K  | VSS         | 19M  |             |      |
| VDD12B      | 23AA | VDD18       | 9B   | VDD18       | 19L  | VSS         | 6Y   | VSS         | 13M  | VSS         | 19P  |             |      |
| VDD12B      | 23AC | VDD18       | 9G   | VDD18       | 19N  | VSS         | 7B   | VSS         | 13P  | VSS         | 19T  |             |      |
| VDD12B      | 24F  | VDD18       | 10F  | VDD18       | 19R  | VSS         | 7F   | VSS         | 13T  | VSS         | 19V  |             |      |
| VDD12B      | 24G  | VDD18       | 10H  | VDD18       | 19U  | VSS         | 7H   | VSS         | 13V  | VSS         | 19Y  |             |      |
| VDD12B      | 24AB | VDD18       | 10K  | VDD18       | 19W  | VSS         | 7K   | VSS         | 13AC | VSS         | 19AB |             |      |
| VDD15       | 4H   | VDD18       | 10M  | VDD18       | 20D  | VSS         | 7M   | VSS         | 14D  | VSS         | 20G  |             |      |
| VDD15       | 4M   | VDD18       | 10P  | VDD18       | 20F  | VSS         | 7P   | VSS         | 14G  | VSS         | 20K  |             |      |
| VDD15       | 4R   | VDD18       | 11G  | VDD18       | 21B  | VSS         | 7T   | VSS         | 14J  | VSS         | 20AA |             |      |
| VDD15       | 4V   | VDD18       | 11J  | VDD18       | 21K  | VSS         | 7V   | VSS         | 14L  | VSS         | 20AC |             |      |
| VDD15       | 4AA  | VDD18       | 11L  | VDD18       | 21P  | VSS         | 7AC  | VSS         | 14N  | VSS         | 21F  |             |      |
| VDD15       | 6K   | VDD18       | 11N  | VDD18       | 21V  | VSS         | 8G   | VSS         | 14R  | VSS         | 21H  |             |      |
| VDD15       | 6M   | VDD18       | 11R  | VDD18       | 23J  | VSS         | 8L   | VSS         | 14U  | VSS         | 21M  |             |      |
| VDD15       | 6P   | VDD18       | 12D  | VDD18       | 23N  | VSS         | 8N   | VSS         | 14W  | VSS         | 21T  |             |      |

Table 16: Power and ground BGA positions.

## 8 Package Specification



**Figure 4: Package mechanical drawing.**

## 9 Test

The IC includes the following test modes.

| Mode           | TEST | A_TYPERDET | LDTSTOP# | STRAPL0 | Notes |
|----------------|------|------------|----------|---------|-------|
| Operational    | 0    | X          | X        | X       |       |
| High impedance | 1    | 0          | 0        | 0       |       |
| NAND tree      | 1    | 0          | 0        | 1       |       |

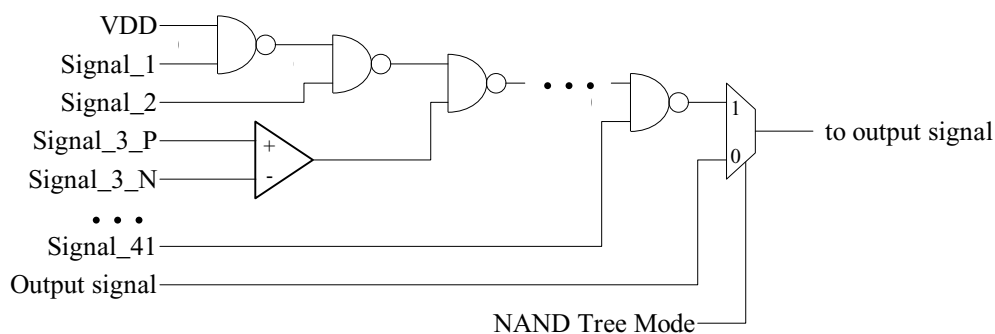
**Table 17: Test modes.**

### 9.1 High Impedance Mode

In high-impedance mode, all the signals of the IC are placed into the high-impedance state.

### 9.2 NAND Tree Mode

There are several NAND trees in the IC. Some of the inputs are differential (e.g., LR[B, A] pins); for these, the \_P and \_N pairs of signals are converted into a single signal that is part of the NAND tree, as shown in Signal\_3 in the following diagram.



**Figure 5: NAND tree.**

NAND tree 1: output signal is STRAPL[5]. However, the gate connected to the last signal in this NAND tree (LDTCOMP[3]) is an AND gate rather than a NAND gate; so the expected output of this NAND tree is inverted compared to the other NAND trees.

|    |                 |    |             |    |             |    |            |
|----|-----------------|----|-------------|----|-------------|----|------------|
| 1  | LRBCLK0_[P,N]   | 11 | LTBCLK0_P   | 21 | LTBCAD_P[4] | 31 | LDTCOMP[2] |
| 2  | LRBCAD_[P,N][0] | 12 | LTBCLK0_N   | 22 | LTBCAD_N[4] | 32 | LDTCOMP[3] |
| 3  | LRBCAD_[P,N][1] | 13 | LTBCAD_P[0] | 23 | LTBCAD_P[5] |    |            |
| 4  | LRBCAD_[P,N][2] | 14 | LTBCAD_N[0] | 24 | LTBCAD_N[5] |    |            |
| 5  | LRBCAD_[P,N][3] | 15 | LTBCAD_P[1] | 25 | LTBCAD_P[6] |    |            |
| 6  | LRBCAD_[P,N][4] | 16 | LTBCAD_N[1] | 26 | LTBCAD_N[6] |    |            |
| 7  | LRBCAD_[P,N][5] | 17 | LTBCAD_P[2] | 27 | LTBCAD_P[7] |    |            |
| 8  | LRBCAD_[P,N][6] | 18 | LTBCAD_N[2] | 28 | LTBCAD_N[7] |    |            |
| 9  | LRBCAD_[P,N][7] | 19 | LTBCAD_P[3] | 29 | LTBCTL_P    |    |            |
| 10 | LRBCTL_[P,N]    | 20 | LTBCAD_N[3] | 30 | LTBCTL_N    |    |            |

NAND tree 2: output signal is STRAPL[4].

|    |                  |    |              |    |              |
|----|------------------|----|--------------|----|--------------|
| 1  | LRACLK0_[P,N]    | 21 | LTACLK0_N    | 41 | LTACAD_N[4]  |
| 2  | LRACLK1_[P,N]    | 22 | LTACLK1_P    | 42 | LTACAD_P[12] |
| 3  | LRACAD_[P,N][0]  | 23 | LTACLK1_N    | 43 | LTACAD_N[12] |
| 4  | LRACAD_[P,N][8]  | 24 | LTACAD_P[0]  | 44 | LTACAD_P[5]  |
| 5  | LRACAD_[P,N][1]  | 25 | LTACAD_N[0]  | 45 | LTACAD_N[5]  |
| 6  | LRACAD_[P,N][9]  | 26 | LTACAD_P[8]  | 46 | LTACAD_P[13] |
| 7  | LRACAD_[P,N][2]  | 27 | LTACAD_N[8]  | 47 | LTACAD_N[13] |
| 8  | LRACAD_[P,N][10] | 28 | LTACAD_P[1]  | 48 | LTACAD_P[6]  |
| 9  | LRACAD_[P,N][3]  | 29 | LTACAD_N[1]  | 49 | LTACAD_N[6]  |
| 10 | LRACAD_[P,N][11] | 30 | LTACAD_P[9]  | 50 | LTACAD_P[14] |
| 11 | LRACAD_[P,N][4]  | 31 | LTACAD_N[9]  | 51 | LTACAD_N[14] |
| 12 | LRACAD_[P,N][12] | 32 | LTACAD_P[2]  | 52 | LTACAD_P[7]  |
| 13 | LRACAD_[P,N][5]  | 33 | LTACAD_N[2]  | 53 | LTACAD_N[7]  |
| 14 | LRACAD_[P,N][13] | 34 | LTACAD_P[10] | 54 | LTACAD_P[15] |
| 15 | LRACAD_[P,N][6]  | 35 | LTACAD_N[10] | 55 | LTACAD_N[15] |
| 16 | LRACAD_[P,N][14] | 36 | LTACAD_P[3]  | 56 | LTACTL_P     |
| 17 | LRACAD_[P,N][7]  | 37 | LTACAD_N[3]  | 57 | LTACTL_N     |
| 18 | LRACAD_[P,N][15] | 38 | LTACAD_P[11] |    |              |
| 19 | LRACTL_[P,N]     | 39 | LTACAD_N[11] |    |              |
| 20 | LTACLK0_P        | 40 | LTACAD_P[4]  |    |              |

NAND tree 3: output signal is STRAPL[3].

|    |            |    |            |    |            |    |            |            |
|----|------------|----|------------|----|------------|----|------------|------------|
| 1  | STRAPL[1]  | 21 | A_DBIL     | 41 | A_CBE_L[2] | 61 | A_AD[12]   | STRAPL[19] |
| 2  | STRAPL[8]  | 22 | A_DBIH     | 42 | A_CBE_L[3] | 62 | A_AD[13]   |            |
| 3  | STRAPL[10] | 23 | A_AD[31]   | 43 | A_ST[0]    | 63 | A_AD[11]   |            |
| 4  | STRAPL[9]  | 24 | A_AD[30]   | 44 | A_ST[1]    | 64 | A_AD[10]   |            |
| 5  | A_GC8XDET# | 25 | A_AD[29]   | 45 | A_ST[2]    | 65 | A_AD[9]    |            |
| 6  | A_SBA[0]   | 26 | A_AD[28]   | 46 | A_MB8XDET# | 66 | A_AD[8]    |            |
| 7  | A_SBA[1]   | 27 | A_AD[27]   | 47 | A_RBF#     | 67 | A_ADSTB0_N |            |
| 8  | A_SBA[2]   | 28 | A_AD[26]   | 48 | A_WBF#     | 68 | A_ADSTB0_P |            |
| 9  | A_SBA[3]   | 29 | A_AD[25]   | 49 | STRAPL[14] | 69 | A_CBE_L[0] |            |
| 10 | A_SBSTB_N  | 30 | A_AD[24]   | 50 | STRAPL[15] | 70 | A_AD[7]    |            |
| 11 | A_SBSTB_P  | 31 | A_ADSTB1_N | 51 | STRAPL[17] | 71 | A_AD[6]    |            |
| 12 | A_SBA[4]   | 32 | A_ADSTB1_P | 52 | STRAPL[16] | 72 | A_AD[5]    |            |
| 13 | A_SBA[5]   | 33 | A_AD[23]   | 53 | A_IRDY#    | 73 | A_AD[4]    |            |
| 14 | A_SBA[6]   | 34 | A_AD[22]   | 54 | A_DEVSEL#  | 74 | A_AD[3]    |            |
| 15 | A_SBA[7]   | 35 | A_AD[21]   | 55 | A_FRAME#   | 75 | A_AD[1]    |            |
| 16 | A_GNT#     | 36 | A_AD[20]   | 56 | STRAPL[6]  | 76 | A_AD[2]    |            |
| 17 | STRAPL[11] | 37 | A_AD[19]   | 57 | A_TRDY#    | 77 | A_AD[0]    |            |
| 18 | A_REQ#     | 38 | A_AD[17]   | 58 | A_CBE_L[1] | 78 | A_STOP#    |            |
| 19 | STRAPL[13] | 39 | A_AD[18]   | 59 | A_AD[15]   | 79 | A_PAR      |            |
| 20 | STRAPL[7]  | 40 | A_AD[16]   | 60 | A_AD[14]   | 80 | STRAPL[18] |            |

Nand tree 4: output signal is STRAPL[2].

|   |           |    |            |    |        |
|---|-----------|----|------------|----|--------|
| 1 | CMPOVR    | 6  | A_PLLCLKI  | 11 | A_PCLK |
| 2 | RESET#    | 7  | STRAPL[20] |    |        |
| 3 | PWROK     | 8  | STRAPL[21] |    |        |
| 4 | REFCLK    | 9  | STRAPL[22] |    |        |
| 5 | A_PLLCLKO | 10 | A_RESET#   |    |        |

Notes:

- LDTSTOP#, A\_TYPERDET#, TEST, STRAPL[0], A\_REFCG, A\_REFGC, A\_CALD, A\_CALD#, A\_CALS, and A\_CALS# are not in the NAND trees.
- While in NAND-tree mode, the link and AGP input compensation is placed at a “mid-band” value.
- While in NAND-tree mode, the AGP signals operate under AGP 2.0 signaling rules.

## 10 Appendix

### 10.1 Revision History

#### Revision 3.02

- Initial release.

#### Revision 3.03

- Removed Preliminary.