intel®

82498 CACHE CONTROLLER AND
82493 CACHE SRAM

For use with the Pentium™ Processor (735/90, 815/100)

- **High Performance Second Level Cache**
  - Zero Wait States at 66 MHz
  - Two-Way Set Associative
  - Writeback with MESI Protocol
  - Concurrent CPU Bus and Memory Bus Operation
  - Boundary Scan

- **Pentium™ Processor (735/90, 815/100)**
  - Chip Set Version of Pentium™ Processor (735/90, 815/100)
  - Superscalar Architecture
  - Enhanced Floating Point
  - On-Chip 8K Code and 8K Data Caches
  - See *Pentium™ Processor Family Data Book* for More Information

- **Highly Flexible**
  - 1 Mbyte to 2 Mbyte
  - 64-, or 128-Bit Wide Memory Bus
  - Synchronous, Asynchronous and Strobed Memory Bus Operation
  - Selectable Bus Widths, Line Sizes, Transfers and Burst Orders

- **Full Multiprocessing Support**
  - Concurrent CPU, Memory Bus and Snoop Operations
  - Complete MESI Protocol
  - Internal/External Parity Generation/Checking
  - Supports Read For Ownership, Write-Allocation and Cache-to-Cache Transfers

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The 82498 Cache Controller and multiple 82493 Cache SRAMs combine with the Pentium processor (735/90, 815/100) and future Pentium Processors to form a CPU Cache chip set designed for high performance servers and function-rich desktops. The high-speed interconnect between the CPU and cache components has been optimized to provide zero-wait state operation. This CPU Cache chip set is fully compatible with existing software, and has new data integrity features for mission critical applications.

The 82498 Cache Controller implements the MESI write-back protocol for full multiprocessing support. Dual ported buffers and registers allow the 82498 to concurrently handle CPU bus, memory bus, and internal cache operation for maximum performance.

The 82493 is a customized high-performance SRAM that supports 64-, and 128-bit wide memory bus widths, 32-, and 64-byte line sizes, and optional sectoring. The data path between the CPU bus and memory bus is separated by the 82493, allowing the CPU bus to handshake synchronously, asynchronously, or with a strobed protocol, and allowing concurrent CPU bus and memory bus operations.