Radiation Tolerant Power Driver with Rotation and Position Sensing

Description

The LX7720 provides four half-bridge drivers with floating current sense for motor coil driving, six bi-level inputs for sensing hall effect sensors or rotary encoders, and a resolver to digital or LVDT interface with primary coil driver. When used with an FPGA or a microcontroller, the LX7720 provides a complete closed loop motor driver with coil current feedback and rotation or linear position sensing. With flexible FPGA programming, the combined system can provide motor control for Stepper motors, Brushless DC and Permanent Magnet motors. Position sensing supports encoders, Hall sensors, resolvers, synchros, and LVDTs. FPGA IP modules are available to support motor driving functions from open loop cardinal step driving to space vector modulation using field oriented control.

The LX7720 contains 7 sigma delta modulators for analog sampling; the sinc3 filters and decimation is performed in the FPGA with available IP module. Four of the modulators sample the voltage across floating current sense inputs and three modulators sample differential analog inputs such as the outputs of a resolver transformer. Speed versus accuracy tradeoffs can be exploited.

The LX7720 supports a ground potential difference between the motor and signal grounds of up to 10V and motor supply voltages up to 50V. Resolver carrier frequencies from 360Hz to 20kHz are supported. The LX7720 offers 1kV HBM ESD pin protection on all sensor and bi-level pins. It is packaged in a 132-pin ceramic quad flat pack and operates over a -55°C to 125°C temperature range. It is radiation tolerant to 100krad TID and 50krad ELDRs as well as single event effects.

Features

- Four half-bridge Nch MOSFET drivers
- Four floating differential current sensors
- Pulse modulated resolver/LVDT transformer driver
- Three differential resolver/LVDT sense inputs
- Six threshold adjustable bi-level logic inputs for hall effect sensor/encoder interfaces
- Fault detection
- Radiation Tolerant: 100krad TID, 50krad ELDRS, Single Event

Applications

- Motor driver servo control
- Linear actuator servo control
- Stepper, BLDC, PMSM motor driver
- Motion control robotics Arm
- Power management and distribution systems

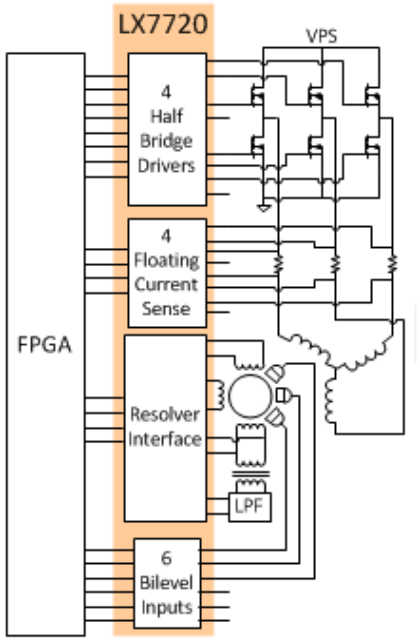


Figure 1 · **Product Highlight**

Pin Configuration and Pinout

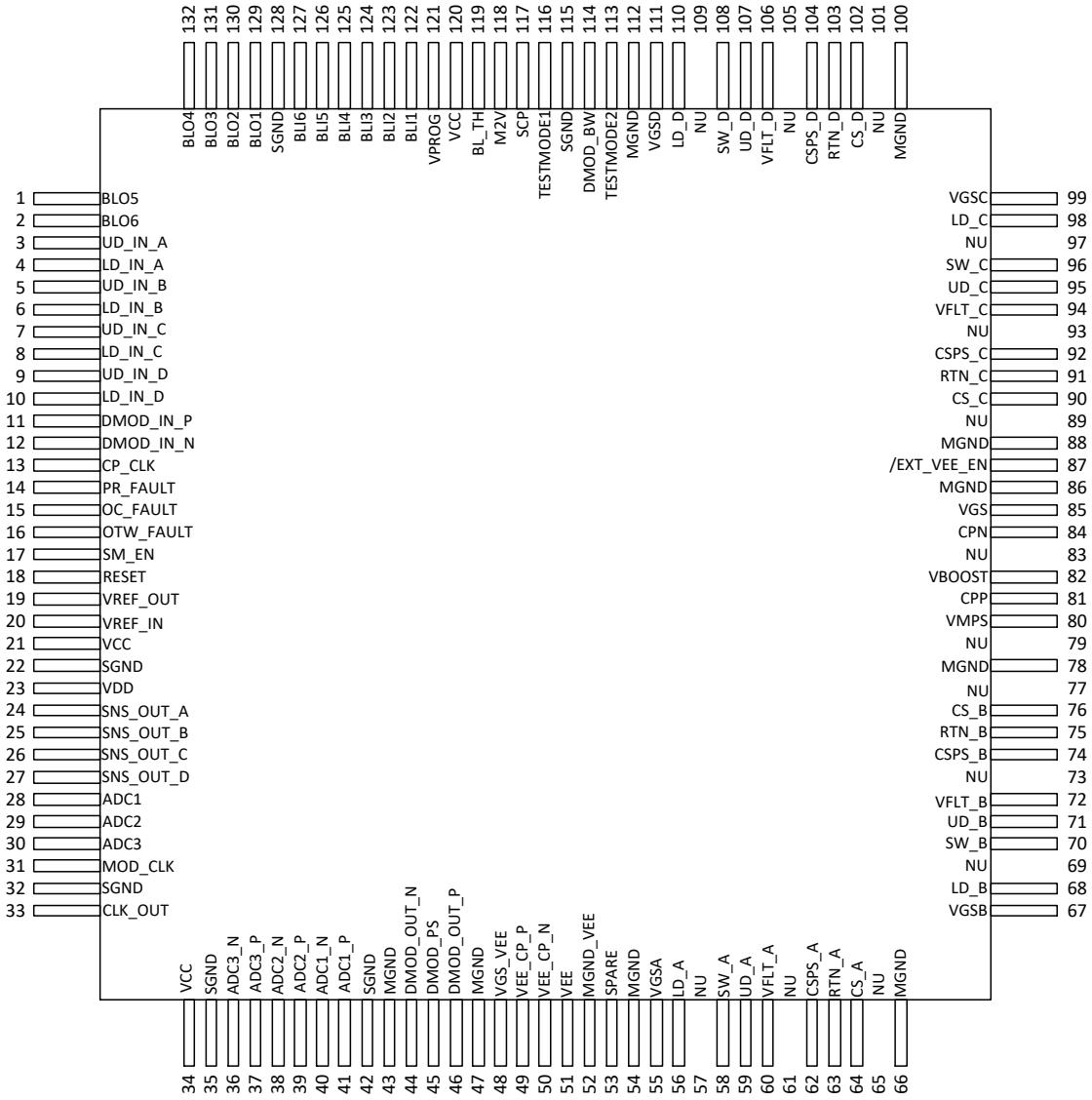


Figure 2 · **Pinout**

Ordering Information

Junction Temperature	Type	Package	Part Number	Packaging Type
-55°C to 125°C	MIL-PRF-38535 Class V	CQFP 132L	LX7720MFQ-EV	Bulk / Tray
-55°C to 125°C	MIL-PRF-38535 Class Q	CQFP 132L	LX7720MFQ-EQ	Bulk / Tray
Commercial	Engineering Samples	CQFP 132L	LX7720-ES	Bulk

Pin Description

Pin Number	Pin Designator	Description
1-2	BLO5 to 6	Fixed Threshold Bi Level detector output - logic output - Provides the state of the Fixed Level Bi Level Input of the same #. BLO5,6 = pins 1,2.
3,5,7,9	UD_IN_#	Phase # upper MOSFET driver control input - logic input - This logic input when asserted causes the upper N-ch MOSFET of the phase # half bridge to turn on. De-assertion causes the MOSFET to turn off. Phase A,B,C,D = pins 3,5,7,9.
4,6, 8,10	LD_IN_#	Phase # lower MOSFET driver control input - logic input - This logic input when asserted causes the lower N-ch MOSFET of the phase # half bridge to turn on. De-assertion causes the MOSFET to turn off. Phase A,B,C,D = pins 4,6,8,10.
11-12	DMOD_IN_#	Pulse width modulated reference - logic input - Provides a pulse coded reference signal that when amplified and filtered produces the exciter drive signal to the resolver or LVDT transformer primary. The DMOD_IN_P (pin 11) drives DMOD_OUT_P. The DMOD_IN_N (pin 12) drives DMOD_OUT_N..
13	CP_CLK	Charge pump clock input - logic input - Provides the timing for the charge pumps that power the floating high side drivers and DMOD timer.
14	PR_FAULT	Power Rail Fault Detected - logic output - When asserted this pin indicates that one of the power rails is below its under voltage threshold or the VGS supply or DMOD_PS supply is overloaded.
15	OC_FAULT	Over Current Fault Detected - logic output - When asserted this pin indicates an overcurrent fault condition exists as detected at one of the current sensors.
16	OTW_FAULT	Over Temperature Warning Fault Detected - logic output - When asserted this pin indicates the die temperature is has exceeded the over temperature warning threshold.
17	SM_EN	Enable Safe Mode - logic input - If this pin is set high (tied to VDD), the LX7720 will detect faults and enable protection countermeasures. If this pin is shorted to SGND, faults will be reported but protection

Pin Number	Pin Designator	Description
		countermeasures will not be taken. This pin has a weak pull up to VDD.
18	RESET	Reset Fault Latch - logic input - If SM_EN is not low, and RESET is asserted, the latched fault condition is reset allowing the LX7720 to attempt to begin functioning normally.
19	VREF_OUT	2.5V reference out- signal output - This pin is a precision reference voltage generated internally. A minimum 200nF bypass capacitor to SGND is required.
20	VREF_IN	2.5V reference in - signal input - This pin provides the reference voltage for the ADC sigma delta modulators. An external reference can be connected here or alternatively the VREF_OUT can be connected to this pin.
21, 34,120	VCC	Main power supply - power input - This pin is the main power supply for the portion of the LX7720 that is referenced to SGND. A bypass capacitor to SGND is required.
22,32,35,42,115,128	SGND	Signal Ground - power pin - This pin provides the ground reference for ADC input signals, bi-level logic and FPGA communication. This ground can be a different potential from the motor ground (MGND).
23	VDD	VDD - power input - This pin is used to reference the I/O logic levels to be compatible with the FPGA. It connects to the FPGA I/O power supply.
24-27	SNS_OUT_#	Phase # current sense output - logic output - This pin provides the output of a 2nd order sigma delta modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between the CS# and RTN# pins. Phase A,B,C,D = pins 24,25,26,27.
28-30	ADC#	A to D Converter # output - logic output - This pin provides the output of a 2nd order sigma delta modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between the ADC#_P and ADC#_N pins. ADC1,2,3 = pins 28,29,30.

Pin Number	Pin Designator	Description
31	MOD_CLK	Modulator clock input - logic input - Provides the clock for the sample rate of the sigma delta modulators.
33	CLK_OUT	Modulator clock output - logic output - Provides the modulator sample clock.
36,41	ADC#_N or P	ADC modulator differential input - differential signal input - These pins provide a differential analog signal feeding into the ADC# sigma delta modulator. For maximum range this input should be referenced to VREF_IN. ADC1,2,3_N = pins 40,38,36. ADC1,2,3_P = pins 41,39,37.
43,47,52,54,66, 78,86,88,100,112	MGND	Motor ground - power pin - This pin is the return rail for the lower motor drivers and connects to the return rail of the motor power supply. This ground may be a different potential than SGND.
44,46	DMOD_OUT_#	Pulse modulated reference out - differential signal output - These pins provide a differential pulse coded signal used to drive the primary of a resolver transformer. The pin voltage amplitude swings from MGND to DMOD_PS. The DMOD_OUT_P (pin 46) is driven by DMOD_IN_P and the DMOD_OUT_N (pin 44) is driven by DMOD_IN_N.
45	DMOD_PS	Demodulator driver power supply input - power input - This pin provides the power to the DMOD_OUT_# differential driver outputs. This pin can be connected to the VGS pin or alternatively to an external power regulator. A bypass capacitor to MGND is required.
48,55,67,85,99,111	VGS#	MOSFET driver power - power input - This pin provides power to the MOSFET drivers and should not exceed the maximum VGS of the external MOSFET switches. A bypass capacitor to MGND is required. All VGS# inputs would typically connect to a common voltage source.
49, 50	VEE_CP_P or N	VEE charge pump transfer capacitor - power pin - A capacitor is connected between the VEE_CP_P and VEE_CP_N pins. The capacitor forms a charge pump used to generate a negative (inverted) voltage from the VGS supply pin.
51	VEE	Negative power rail - power pin - This pin is the negative voltage power rail. It can be generated

Pin Number	Pin Designator	Description
		internally (using the charge pump) or supplied from an external source connected to this pin. A bypass capacitor to GND is required. The charge pump can be disabled by shorting the /EXT_VEE pin to MGND.
56, 68, 98, 110	LD_#	Phase # lower MOSFET gate driver - power pin - This pin connects through a resistor to the gate of the lower side phase # Nch MOSFET. The MGND pin provides the return current path for this driver. LD_A,B,C,D = adjacent pin pairs 56, 68, 98, 110.
58, 70, 96, 108	SW_#	Phase # half-bridge switch pin - power pin - This pin connects to the source of the upper phase # Nch MOSFET and is the upper MOSFET driver return path. SW_A,B,C,D = adjacent pin pairs 58, 70, 96, 108.
59, 71, 95,107	UD_#	Phase # upper MOSFET gate driver - power pin - This pin connects through a resistor to the gate of the phase # high side Nch MOSFET. The SW_# pin provides the return current path for this driver. UD_A,B,C,D = adjacent pin pairs 59, 71, 95, 107.
60, 72, 94, 106	VFLT_#	Phase # floating power rail - power pin - This pin provides power to the floating upper Nch MOSFET driver for phase #. This pin should be bypassed with a capacitor to the SW_# pin. VFLT_A,B,C,D = adjacent pin pairs 60, 72, 94, 106. It is recommended to add an external bootstrap Schottky diode between VGS# and VFLT#. This will lower the power dissipated on the internal bootstrap diode.
62, 74, 92, 104	CSPS_#	Phase # current sense power supply - power pin - This pin provides power to the floating current sense for phase #. It can be connected to either the VFLT_# rail for a SW_# pin sensing or VGS for low side sensing. A bypass capacitor to RTN_# is required. CSPS_A,B,C,D = pins 62, 74, 92, 104.
63, 75, 91, 103	RTN_#	Phase # current sense return - signal/power pin - This pin provides the ground reference for the phase # floating current sense for both powering the circuitry as well as the current measurement. RTN_A,B,C,D = pins 63, 75, 91, 103.
64, 76, 90, 102	CS_#	Phase # current sense - signal pin - This pin provides the current measurement input for the phase # floating current sense. The linear range for current sensing is

Pin Number	Pin Designator	Description
		+/- 200mV across the phase # sense resistor. CS_A,B,C,D = pins 64, 76, 90, 102.
80	VMPS	Motor Power supply - power pin - This pin is the Motor High voltage power rail. The motor power supply is referenced to MGND. This input is used for the boost charge pump to drive the high side driver at 100% duty cycle. A bypass capacitor to GND is required.
81	CPP	Charge pump transfer capacitor positive terminal - power pin - These pins connect to a capacitor that is used to replenish the VBOOST pin. The charge pump accommodates periods of long sustained on times for the upper MOSFET.
82	VBOOST	Upper MOSFET driver charge pump output - power out - This pin is the output of a charge pump that is used to drive the upper MOSFET driver for long duration duty cycles. A bypass capacitor to VMPS is required.
84	CPN	Charge pump transfer capacitor positive terminal - power pin - These pins connect to a capacitor that is used to replenish the VBOOST pin. The charge pump accommodates periods of long sustained on times for the upper MOSFET.
87	/EXT_VEE_EN	Enable external VEE - programming pin - This pin disables the VEE charge pump if it is shorted to MGND. If high (shorted to VGS), the VEE charge pump is enabled. There is a weak pull-up to VGS on this pin.
113, 116,	TESTMODE#	Test and Trim Pins - programming Pins - These pins are used for in-package trim and testing of the device. In normal use TESTMODE1 should be connected to SGND and TESTMODE2 should be connected to MGND.
114	DMOD_BW	DMOD Driver Band Width - logic input - This pin is used to reduce the propagation delay for the exciter. If this pin is connected to SGND, the exciter has increased propagation time but draws less current. This pin has a weak pull down. When DMOD_BW is set high (by shorting it to VCC) the smaller propagation delay is selected. This is the recommended setting for operation at 100kRad (TID).

Pin Number	Pin Designator	Description
117	SCP	Simultaneous Conduction Protection - logic input - If SCP is logic high, logic is enabled that prevents UD# and LD# for a given switch pin from being held on simultaneously. If SCP is low, UD# and LD# can be operated independently. There is a weak pull up on this pin.
118	M2V	Minus 2V - programming pin - This pin is used for in-package trim and testing of the device. In normal use it should be shorted to SGND.
119	BL_TH	External bi-level threshold setting - signal I/O - This pin is used to control the bi-level threshold setting.
121	VPROG	Programming voltage - test input - Connect to VCC during normal operation.
122-127	BLI1 to 6	Fixed threshold Bi Level Signal Input - signal input - This pin is fixed threshold bi-level input. BLI1,2,3,4,5,6 = pins 122,123,124,125,126,127.
129-132	BLO1 to 4	Fixed Threshold Bi Level detector output - logic output - Provides the state of the Fixed Level Bi Level Input of the same #. BLO1,2,3,4 = pins 129,130,131,132

Functional Block Diagram

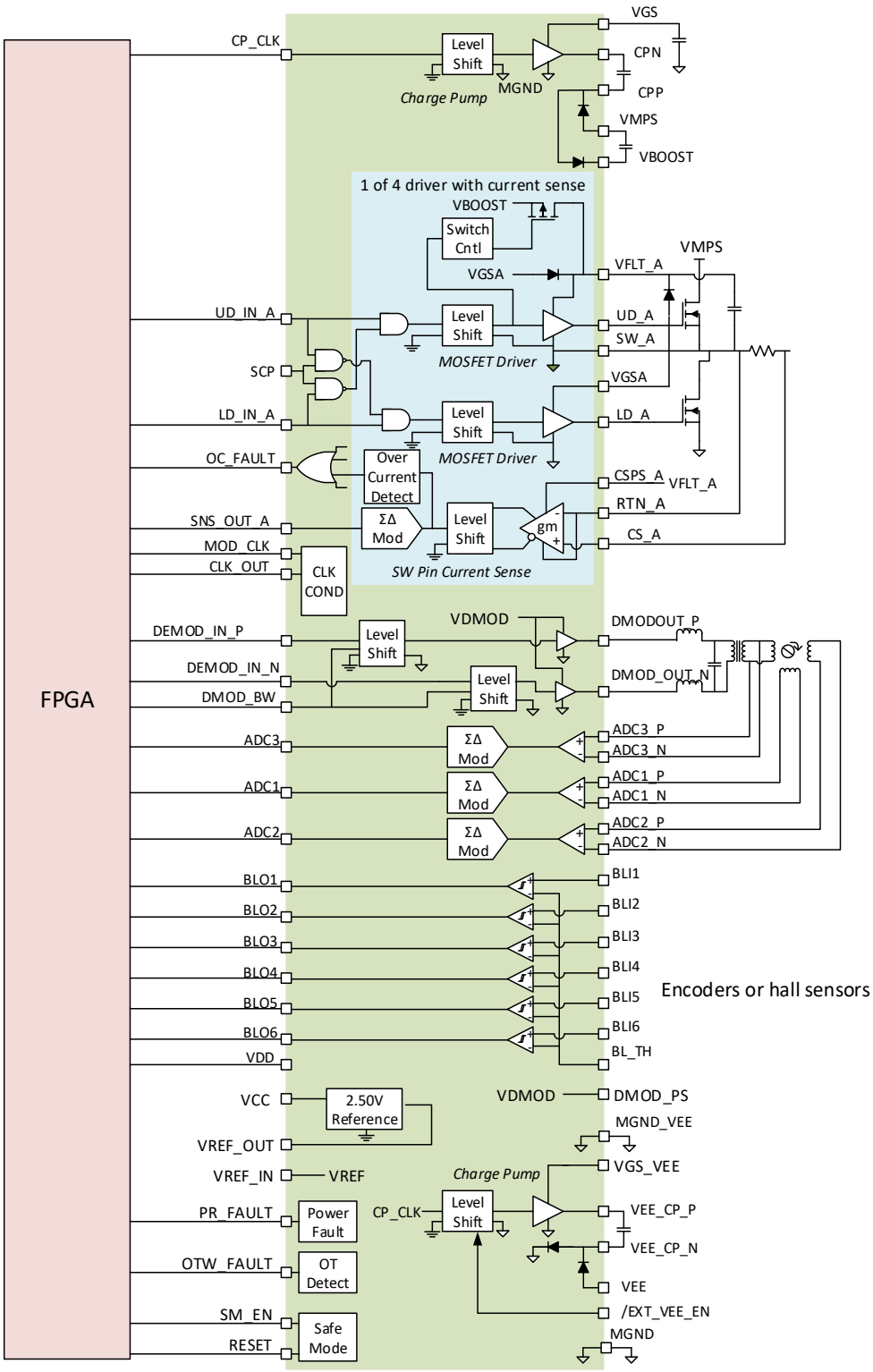


Figure 3 · **LX7720 Top Level Block Diagram**

Absolute Maximum Ratings

Note: Stresses above those listed in “ABSOLUTE MAXIMUM RATINGS”, may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Motor power supply (VMPS) to MGND	-0.5	80	V
Switch pin (SW_#) and RTN_# to MGND	-1.0	80	V
Signal Power Supply (VCC) to SGND	-0.5	7	V
Logic Supply Voltage (VDD) to SGND	-0.5	7	V
Ground potential difference (SGND to MGND)	-10	10	V
Gate Driver Power Supply (VGS) to MGND	-0.5	22	V
Negative Power Supply (VEE_IN) to MGND	-22	0.5	V
Voltage reference (VREF_IN) to SGND	-0.5	7	V
Resolver power (DMOD_PS) to MGND	-0.5	22	V
Current sense power sup (CSPS_#) to RTN_#	-0.5	22	V
Current sense (CS_#) to RTN_#	-5	5	V
FPGA interface (Pins 1-18, 24-31, 33, 117, 129-132) to SGND	-0.5	VDD + 0.5 < 7	V
Bi-Level Inputs (BLI1 to 6, BL_TH) to SGND	-0.5	7	V
Bi-Level Inputs clamp current	-3	3	mA
ADC#_P, ADC#_N to SGND	-0.5	7	V
Operating Junction Temperature	-55	150	°C
Storage Junction Temperature	-65	160	°C
ESD Susceptibility (all pins, HBM, JEDEC JS-001-2017)		500	V
Peak Lead Solder Temperature (10 seconds)		260 (+0, -5)	°C

Operating Ratings

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Motor Power Supply (VMPS) to MGND	20	60	V
Signal Power Supply (VCC) to SGND	4.75	5.25	V
Logic Supply Voltage (VDD) to SGND	2.1	5.5	V
Gate Driver Power Supply (VGS) to MGND (with VGS to SGND > 7V)	10	18	V
Negative voltage reference (VEE_IN)	-VGS	-8	V
VGS voltage if using internally generated VEE	12	18	V
Voltage reference (VREF_IN) to SGND	2.3	2.7	V
DMOD_PS exciter voltage to MGND (with DMOD_PS to SGND > 7V)	10	18	V
DMOD_PS exciter current	0	100	mA
One MOSFET driver average source/sink (Qg x Fsw)	0	25	mA
Current sense power sup (CSPS_#) to RTN_#	10	18	V
Current sense (CS_#) to RTN_#	-250	250	mV
Ground potential difference (MGND to SGND)	-10	8	V

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JC}	2	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: VVCC= 5.0V, VVDD = 3.3V; VVREF_IN = 2.5V; VVGS=15.0V; VVEE =-15.0V (/EXT_VEE=GND); DMOD_PS=15.0V; VBL_TH=2.5V; MOD_CLK = 32MHz; CP_CLK = 200kHz, VMPS = 50V.Typical parameter refers to T_J = 25°C. Positive currents flow into the pin. THD is measured based on fundamental and harmonics up seventh order.

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
Operating Current						
I_{VCC}	VCC Current	All ADCs off, all current sense off	5	15	20	mA
		All ADCs on, all current sense off	25	46	55	mA

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
		All ADCs off, all current sense on	35	67	80	mA
		All ADCs on, all current sense off	60	98	120	mA
I_{VGS}	VGS Current	All UD_IN# and LD_IN# low	10	20	26	mA
		All LD_IN# and UD_IN# high	15	26	33	mA
I_{VEE}	VEE Current	All UD_IN# and LD_IN# low	-12	-8	-4	mA
		All UD_IN# and LD_IN# low; VEE = -15V; no load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	-21	-14	-6	mA
I_{DMOD_PS}	DMOD_PS Current	No load on DMOD_OUT_N/P; DMOD_IN_P and DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	0.2	1	1.5	mA
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	2	6	11	mA
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW high; DMOD_PS = 15V	4	10	17	mA
I_{VDD}	VDD Current	All LD_IN#=HI and UD_IN# =HI	0	25	42	mA
Under Voltage Detection						
V_{VCC}	VCC UVLO	Voltage rising; 200mV Hysteresis	4	4.25	4.5	V
V_{VDD}	VDD UVLO	Voltage rising; 200mV Hysteresis	1.6	1.8	2.0	V
$V_{VGS\ to\ MGND}$	VGS UVLO to MGND	Voltage falling; 200mV Hysteresis	9.1	9.4	9.8	V
$V_{VGS\ to\ SGND}$	VGS UVLO to SGND	Voltage rising; 120mV Hysteresis	6.2	6.4	6.6	V
V_{VEE}	VEE_IN UVLO	Voltage falling; 350mV Hysteresis	-8	-7	-6	V
Internally Regulated Voltages and Currents						
V_{VREF_OUT}	VREF regulator		2.48	2.5	2.52	V
V_{VEE}	Inv Chg Pump	No external load; /EXT_VEE=open; V_{VGS} -|V_{VEE}|	1.0	1.9	2.4	V
V_{VBOOST}	Charge Pump	Boot strap not connected;10mA load [V_{VGS} + V_{VMPS}] - V_{VBOOST}	0.5	1.6	2.1	V
V_{VBOOST} - $V_{VFLT\#}$	VBOOST switch	With UD_IN_# high	0.05	0.3	0.6	V
I_{VREF_OUT}	VREF regulator	Short Circuit Current	25	50		mA
$I_{VGS\ \#}$	Fault threshold	VGSA, VGSB, VGSC and VGSD fault current threshold	110		360	mA
$I_{VGS\#}$	Fault blanking	VGS# spike duration to trigger fault with 400mA load	1.5	3.5		us
I_{DMOD_PS}	Fault threshold	DMOD_PS fault current threshold	110		360	mA

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
I_{DMOD_PS}	Fault blanking	DMOD_PS spike duration to trigger fault with 400mA load	1.5	3.5		us
Clocks						
F_{MOD_CLK}	MOD_CLK	Frequency range	24		32	MHz
F_{MOD_CLK}	MOD_CLK missing	Minimum non-transition dead time		200		ns
P_{CLK_OUT}	CLK_OUT	Delay CLK_OUT to ADC# and SENS_OUT_#	0.5	7	12	ns
F_{CP_CLK}	CP_CLK	Frequency range	100	200	300	kHz
MOSFET DRIVER (Cload = 1000pF)						
$R_{UD\_\#}$	Upper Driver Impedance	VFLT# to UD_#; UD_IN_# = high	0.85		10.0	Ω
		UD_# to SW_#; UD_IN_# = low	0.85		10.0	
		UD_# to SW_#, VGS = 0 to UVLO			20k	
$R_{LD\_\#}$	Lower Driver Impedance	VGS_OUT to UD_#; LD_IN_# = high	0.85		10.0	Ω
		LD_# to MGND; LD_IN_# = low	0.85		10.0	
		LD_# to MGND; VGS = 0 to UVLO			20k	
tPHL,PLH	Propagation Delay	Upper Driver; UD_IN_# to UD_A	140	250	400	ns
		Lower Driver; LD_IN_# to LD_A	140	250	400	
		Matching all drivers, all edges			150	
tR,F	Rise time and Fall time	10% to 90%	20	60	120	ns
tPWH, tPWL	Minimum input Pulse Width (High or Low)	Output reaches 67% VGS for tPWH and 1V for tPWL; C=1nF load			200	ns
$I_{UD\_\#}$	Leakage current with VGS and VCC = 0V	UD_#, SW_#, VFLT# wired together; $V_{SW\_\#}$ = 0V to 80V ref to MGND	-50		50	uA
$V_{UD\_\#}$	Upper drive voltage with 100% duty cycle	UD_IN# held High, UD_# loaded with 4 mA. Measured relative to VMPS	11.5		15	V
dV_{SW}/dt	Maximum SW# slew rate				10	kV/us
Internal bootstrap diodes						
V_{ON_B}	Forward voltage	IF = 100mA, Tj=25C	0.9		1.1	V
V_{ON_B}	Forward voltage	IF = 100mA, Tj=-55 and 125C	0.8		1.2	V
I_{Fmax_B}	Maximum DC current				100	mA
I_{PRmax_B}	Peak Repetitive maximum current	F = 100kHz, Duty cycle = 10%, square wave. Vr=-30V			1.5	A
t_{RR_B}	Reverse Recovery time	I_F=100mA, V_R=9V, dI_F/dt = TBD		300		ns
I_{RM_B}	Peak reverse recovery current	I_F=100mA, V_R=9V, dI_F/dt = TBD		90		mA
ADC Converters (with sinc3 filter and OSR = 256, input common mode = 2.1V unless otherwise specified)						
$FSR_{ADC\_\#}$	Max differential input	Extrapolated Clipping points of PDM output		+/-1400		mV

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
SLR $_{ADC\_\#}$	Specified linear range			+/-800		mV
V_{CMR_ADC}	Input common mode	With Vdiff = +/-800mV and THD < THD24/32$_{ADC}$(Max) - 3dB	0.5		VCC-2.1V	V
V_{CMR_ADC}	Common mode rejection	0.5V to 2.9V	45			dB
$BW_{ADC\_\#}$	Max frequency	With attenuation < 0.1dB	20			kHz
	Min frequency	By design			0	Hz
$AV_{ADC\_\#}$	Gain error	Tj=25C and 125C	-0.65		0.65	%
$AV_{ADC\_\#}$	Gain error	Tj=-55C	-0.8		0.8	%
V_{OS_ADC}	Offset error	Equivalent input for code measured to shorted inputs. Tj=25C	-0.05		0.05	%FSR
V_{OS_ADC}	Offset error	Equivalent input for code measured to shorted inputs. Tj=125C	-0.12		0.12	%FSR
V_{OS_ADC}	Offset error	Equivalent input for code measured to shorted inputs. Tj=-55C	-0.5		0.5	%FSR
$INL24_{ADC}$	Integral Non-Linearity	Gain error from straight line at 24MHz	-0.03	+/-0.01	0.03	%FSR
$INL32_{ADC}$	Integral Non-Linearity	Gain error from straight line at 32MHz	-0.06	+/-0.02	0.06	%FSR
$RES24_{ADC}$	No missing codes resolution at 24MHz	Histogram test using triangular wave	14	15		bits
$RES32_{ADC}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits
$SNR24_{ADC}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	93	100		dB
$THD24_{ADC}$	Total Harmonic Distortion at 24MHz clock	Input frequency = 1kHz, amplitude = 800mV		-79	-73	dB
$SNR32_{ADC}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	92	98		dB
$THD32_{ADC}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = 800mV		-78	-70	dB
tSWTO	ADC Timeout	ADC#_P= ADC#_N > **VSWTO** to cause ADC modulator sleep mode	225		325	us
VSWTO	ADC timeout threshold		VCC-0.25	VCC-0.1	VCC	V
CADC#	Diff input capacitance			10		pF
RADC#	Diff input resistance		50	250		kΩ
Floating Current Sense (with sinc3 filter and OSR = 256, input common mode = 0V unless otherwise specified)						
$FSR_{CS\_\#}$	Max differential input	Clipping points of PDM output		+/-350		mV
SLR $_{CS\_\#}$	Specified linear range			+/-200		mV
E_{CMR_CS}	Input common mode induced gain error	Input common mode from 0 to 50V	-0.15		0.15	%

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
V_{CMR_CS}	Input common mode rejection	CM = 50V	85			dB
$BW_{CS\_\#}$	Max frequency	With attenuation < 3dB	75			kHz
	Min frequency	With attenuation < 0.1dB			0	Hz
$AV_{CS\_\#}$	Gain error	Tj=25C	-0.5		0.5	%
$AV_{CS\_\#}$	Gain error	Tj=-55C and 125C	-1.3		1.3	%
V_{OS_CS}	Offset error	VCS_# = VRTN_#, Tj=25C	-0.2		0.2	%FSR
V_{OS_CS}	Offset error	VCS_# = VRTN_#, Tj=-55C and 125C	-1.1		1.1	%FSR
$RES24_{CS}$	No missing codes resolution at 24MHz	Histogram test using triangular wave	14	14		bits
$RES32_{CS}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits
$INL24_{CS}$	Integral Non-Linearity at 24MHz clock.	Gain error from straight line	-0.06	+/-0.03	0.06	%FSR
$INL32_{CS}$	Integral Non-Linearity at 32MHz clock.	Gain error from straight line	-0.06	+/-0.03	0.06	%FSR
$SNR24_{CS}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR=64	74	78		dB
$THD24_{CS}$	Total Harmonic Distortion at 24MHz clock	Input frequency = 1kHz, amplitude = 200mV, OSR=64		-75	-65	dB
$SNR32_{CS}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR=64	73	77		dB
$THD32_{CS}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = 200mV, OSR=64		-75	-65	dB
ZIN_CS	Differential Input Imped.	CS_# to RTN_#	0.1	2		MΩ
	Common mode	RTN# or CS# to MGND	50	150		kΩ
IBIAS_CS#	CS# bias current		-0.2		0.2	mA
IBIAS_RTN#	RTN# bias current		-1		1	mA
$V_{CS\_\#}$	Over Current Sense Threshold	Current flow into SW_# pin	260	320	380	mV
		Current flow out of SW_# pin	-380	-320	-260	
$V_{CS\_\#}$	Over Current Blanking	Spike filter pole	10		20	us
$I_{CS\_\#}$	Leakage current with VCPS_# and VCC = 0V	CPS_#, RTN_#, CS_# wired together; VCS= 0V to 80V referenced to MGND	-50		50	uA
Fixed Threshold Bi-Level Inputs						
$V_{BLI\#}$	Threshold (Rising Voltage)		2.4	2.5	2.6	V
$V_{BLI\#}$	Hysteresis	Only falling edge has hysteresis	80	150	200	mV
$V_{BLI\#}$	Voltage Clamp	Clamp Current = 1mA (into pin)	6.5	10	13	V

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
		Clamp Current = 1mA (out of pin)	-1.9	-1.4	-0.9	V
$I_{BLI\#}$	Bias Current	V_{BLI1}= 0V to 5V	-2	0	2	uA
$I_{BLI\#}$	Leakage Current	V_{BLI1}= 0V to 5V; IC powered off	-1	0	1.2	uA
$t_{BLI\#}$	Propagation Delay		10	40	80	ns
V_{BL_TH}	Ext Threshold Pin Range		0.5		4.5	V
I_{BL_TH}	Threshold Pin Leakage	V_{BL_TH}= 0V to 5V	-1	0	1.5	uA
Demodulator driver (differential load of 100Ω)						
$V_{DMOD\_OUT\_P,N}$	Voltage Range	Either output relative to MGND	10		18	V
$R_{DMOD\_OUT\_P,N}$	Source Impedance	WRT DMOD_PS; Sourcing current	0.8	2	4	Ω
		WRT MGND; Sinking current	0.8	2	4	
$R_{DMOD\_OUT\_P,N}$	High-Z state Leakage	DMOD_IN_P/N inactive; WRT DMOD_PS or MGND	-50		50	uA
tPHL	Propagation Delay H to L	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LOW	75		155	
tPLH	Propagation Delay L to H	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LO	75		155	
tPHL,PLH	Propagation Delay	Matching between DMOD_OUT_P and DMOD_OUT_N; HL to HL and LH to LH		7	20	ns
tR,F	Rise time	10% to 90%	4	17	30	ns
tR,F	Fall time	10% to 90%	6	33	60	ns
Logic Levels						
VLOG_IN VDD	Input Logic Threshold for VDD related inputs Pins 3-13, 17-18, 31, 117	VIH	70			%VDD
		VIL			30	%VDD
		Hysteresis at VDD=3.3V	100	160	220	mV
VLOG_IN other	Input Logic Threshold for other input pins	VIH pin 87 (EXT_VEE)	1.2			V
		VIL pin 87 (EXT_VEE)			0.25	
		VIH pin 114 (DMOD_BW)	1.8			
		VIL pin 114 (DMOD_BW)			0.4	
VLOG_OUT VDD	Logic Output Levels for VDD related outputs Pins 1-2, 14-16, 24-30, 33, 129, 132	High Logic Level (100µA source)	VDD-0.3			V
		Low Logic Level (100µA sink)			0.3	
ILOG_IN	Input currents for VDD related inputs	VLOG_IN = 3.3V (with pull down res)		4	7	µA
		VLOG_IN = 0V (with pull up res)	-7	-4		

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
ILOG_IN other	Input currents for other input pins	Pin 87 (EXT_VEE) V = 0V	-80	-38	-10	µA
		Pin 114, (DMOD_BW) V = 3.3V	10	37	80	
		Pin 114, (DMOD_BW) V = 0V	-1	0	1	
Thermal Shutdown						
OT_SDN	Thermal Shutdown threshold; SM_EN = 1	Threshold Temperature	135	150	165	°C
OTW_ FAULT	Over temperature warning threshold	Warning Temperature (T_{SD} - T_{OTW})	15	25	35	
		Hysteresis	10	15	25	

Typical Application

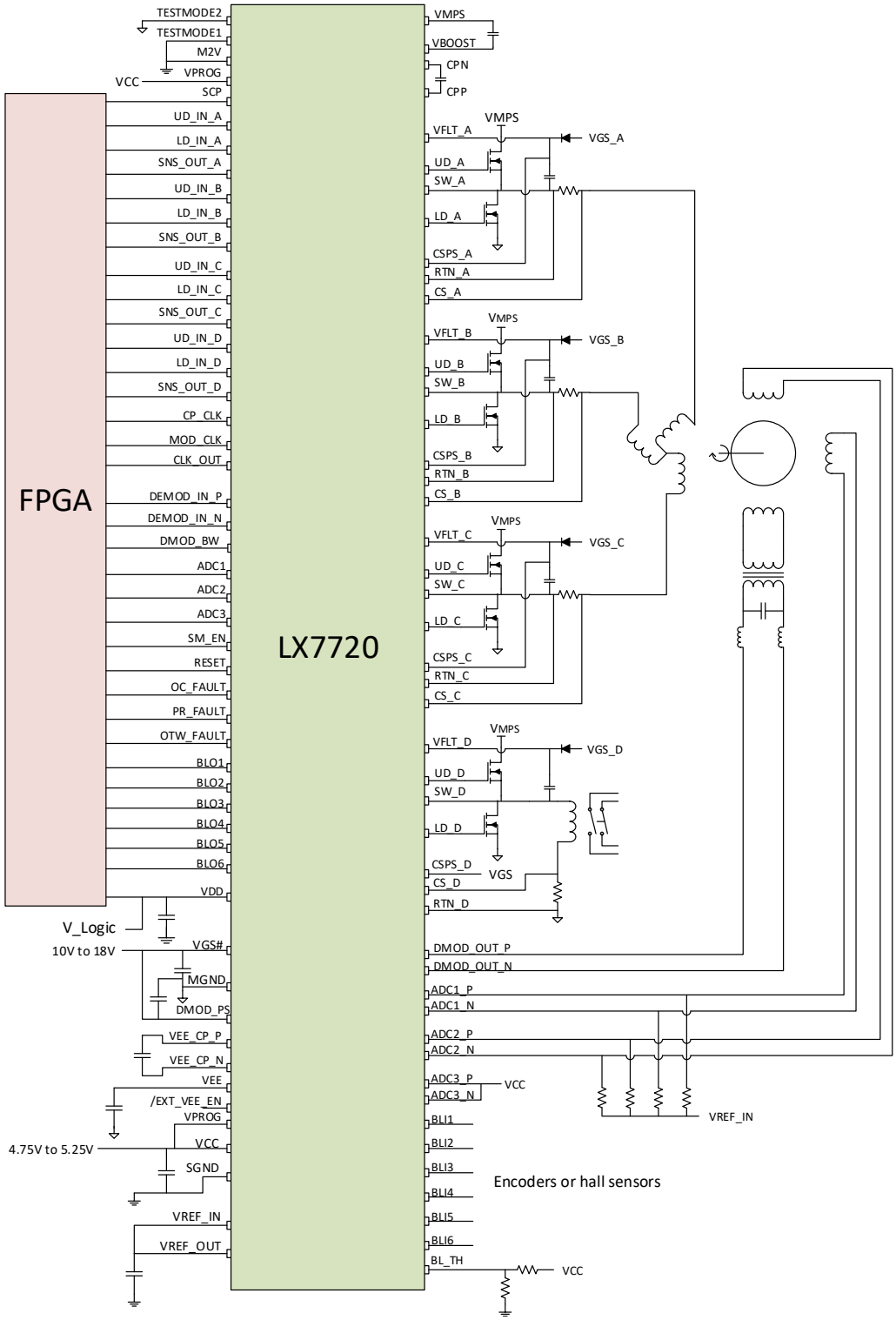


Figure 4 · **Typical Application**

Theory of Operation

MOSFET Driver

The LX7720 contains four high speed half bridge drivers with independent high and low side channels to drive all N channel MOSEFTs. Isolation is provided between the FPGA ground (SGND) and the motor ground (MGND). Both channels are powered from the VGS with the floating upper driver being powered from a bootstrap capacitor to the SW pin and/or the VBOOST charge pump to support long duration on times. The bootstrap capacitor is charged via a combination of internal diode and an external Schottky diode from VGS. The usage of the external diode is recommended to reduce the dissipated power on the internal diode during reverse recovery. The drivers are designed to have a pull-down impedance to bias the external MOSFETs in the off state if power is lost. The drivers continue to float relative to MGND if power is removed from the IC. There is simultaneous conduction protection that prevents the high side and low side switches from conducting simultaneously on a continuous basis; this can be disabled by grounding the SCP pin.

Floating Current Sense

The floating current sense is an isolated circuit that can be referenced to either the MGND or the SW_# pin to measure return currents (to MGND) or motor coil currents flowing from the SW_# node. The current sense is bi-directional and measures sense voltages in the +/-200mV linear range.

The sensed voltage is amplified and level shifted to an SGND referenced 2nd order sigma delta modulator designed to sample at 24 to 32MHz. The CS_# voltage relative to RTN_# of 0V is converted to a 50% full scale output. Positive amplitudes (flow CS# to RTN#) registered as >50% of full scale and negative differential amplitudes registered as <50% of full scale. The resultant bit stream is sent to the FPGA where it can be processed using a sinc3 filter and disseminator. A decimation ratio of 16 provides almost 9 bits of accuracy with a filter response time of 5us with a 32MHz sample rate. The sample rate is set by MOD_CLK and sampling is synchronized to CLK_OUT.

The # modulator will enter sleep mode after both UD_IN_# and LD_IN_# are simultaneously de-asserted for more than 8192 MOD_CLK cycles.

The floating current sense is powered from the CSPS_# pin. The current sense continues to float relative to MGND if power to the IC is removed.

Fixed Bi-Level Inputs

There are six fixed bi-level inputs with a common threshold setting at the BL_TH pin. A low pass filter and threshold hysteresis provides high frequency noise rejection. The Bi-Level inputs are cold spared.

Resolver / Synchro / LVDT to Digital Interface

The RTD interface consists of a differential driver output DMOD_OUT_P and DMOD_OUT_N to drive the resolver transformer primary and three differential inputs AD1,2 &3. ADC1 and ADC2 can be used to sense the two secondary output voltages. ADC 3 can be used to sense the primary voltage. If the DMOD_IN_N and DMOD_IN_P inputs remain low for more than 65536 MOD_CLK cycles, the DMOD_OUT_N and DMOD_OUT_P outputs both become a high impedance.

The resolver primary is driven with a sinusoidal carrier voltage with a frequency that ranges from 360Hz to 20kHz. The DMOD_OUT_P and DMOD_OUT_N differential outputs are driven with a pulse width modulated signal from DEMOD_IN_P and DEMOD_IN_N, respectively. The differential output can be filtered similar to a class-D audio signal. The DMOD_OUT_P and DMOD_OUT_N output drivers are powered from a separate higher voltage rail (DMOD_PS) so they can provide a

wide dynamic range; the DMOD_PS rail is referenced to the MGND. The driver bias current can be reduced by grounding the DMOD_BW pin; this reduces the effective pulse rate of the driver.

The ADC# differential inputs are referenced to VREF and may require an external attenuation voltage divider to be compatible with the voltage range of these inputs (SGND to VCC). A differential input voltage of 0V is converted to a 50% full scale output. Positive amplitudes registered as >50% of full scale and negative differential amplitudes registered as <50% of full scale. The 2nd order sigma delta modulator samples at the MOD_CLK rate or a sample range of 24 MHz to 32 MHz. The resultant bit stream is sent to the FPGA where it can be processed using a sinc3 filter and decimator. A decimation ratio of 64 to 256 provides accuracies from 10 to 14 bits. The sample rate is set by MOD_CLK and sampling is synchronized to CLK_OUT.

A modulator will enter sleep mode after both ADC#_P and ADC#_N are simultaneously held to VCC for more than 8192 MOD_CLK cycles.

FPGA Interface

The logic input pins have a 1MΩ pull down to ground and will assume a logic low level if open circuited. The logic level is determined by the voltage at the VDD pin which should also be connected to the FPGA VIO pin.

Over-current Detection

The Current sense detection circuitry will detect when the driven coil currents exceed the threshold levels indicated in the EC table and assert and latch the OC_FAULT logic output. A spike filter prevents very short duration spikes from triggering an OC detection.

Power Faults and Driver Overload

The MOSFET drivers and DMOD_OUT_# drivers are designed to deliver average currents up to those specified in the normal operating range table from the VGS and DMOD_PS power rails. The drivers will assert and latch the PR_FAULT pin if the average levels exceed the overcurrent thresholds. The VGS current is monitored for all the MOSFET drivers. The DMOD_PS current is monitored for the demodulator driver. A PR_FAULT is also asserted and latched if the monitored voltage rails fall below the UVLO threshold levels specified in the Electrical Characteristics table.

Over-temperature Warning

In the event that the die temperature exceeds the over temperature warning threshold, the OTW_FAULT output will be asserted. This warning allows a small operating window before the die temperature reaches the overtemperature shutdown threshold. The overtemperature shutdown is a latched fault state when safe mode is enabled.

RESET and SAFE MODE

Once a fault pin is latched, it can be reset by clearing the fault condition and then either toggling the RESET pin or cycling the power.

If safe mode is not enabled, the LX7720 will rely exclusively on the FPGA or system to use counter measures like shutting off the external MOSFETs or removing power in an attempt to correct faults. The SM_EN has a pull up to VDD and must be pulled low to disable.

In safe mode, the LX7720 will exert counter measures whenever a fault is latched. Safe mode is armed after power up by the power on reset and UVLO de-assertions.

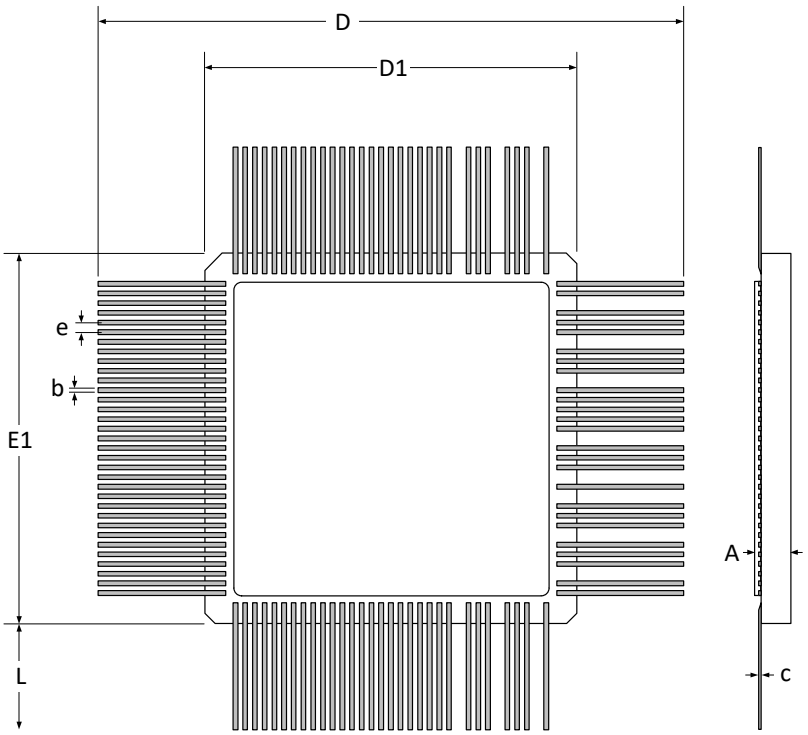
1) If an OC_FAULT is detected, the LX7720 will place all external MOSFET switches in the “off” state.
2) If a PR_FAULT is detected, the LX7720 will place all external MOSFET switches in the “off” state and place both DMOD_OUT_P and DMOD_OUT_N in the low state.

3) If the over-temperature shut down threshold is exceeded and latched or if MOD_CLK is stopped, the IC enters a low power state except for the FPGA control lines and the RESET function circuitry. All external MOSFETs default to the “off” state in low power mode. The MOD_CLK stopped fault is not a latched fault; operation resumes when MOD_CLK is restored.

Recommended external component values

Device name	Device connection	Recommended value/range
VBOOST capacitor	VBOOST to VMPS	1…10µF
VMPS decoupling near VBOOST	VMPS to ground	100nF
VBOOST charge pump capacitor	CPP to CPN	300nF…3.3µF
Bootstrap capacitor	VFLT# to SW#	100nF…1µF
External bootstrap diode	VGS# to VFLT#	Schottky diode to support most of the current during capacitor charging
VEE output capacitor	VEE to ground	1…10µF
VEE charge pump capacitor	VEE_CP_P to VEE_CP_N	300nF…3.3µF

Ceramic Quad Flat Pack Outline Dimensions



Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.93	2.39	0.076	0.094
b	0.23	0.33	0.009	0.013
c	0.125	0.20	0.0049	0.0079
D	39.37 typ		1.55 typ	
D1	24.00	24.26	0.945	0.955
e	0.635 BSC		0.025 BSC	
E	39.37 typ		1.55 typ	
E1	24.00	24.25	0.945	0.955
L	7.62 typ		0.30 typ	

Note:

1. Package will include a non-conductive ceramic tie-bar (not shown) mechanically connected to all pins.
2. Parts are shipped with untrimmed and unformed leads.

Figure 5 · **Package Dimensions**

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