DM2203/2213 EDRAM
512Kb x 8 Enhanced Dynamic RAM

Preliminary Datasheet

Features

- 8Kbit SRAM Cache Memory for 15ns Random Reads Within Four Active Pages
- Fast 4Mbit DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 5ns Output Enable Access Time Allows Fast Interleaving
- 256-byte Wide DRAM to SRAM Bus for 7.3 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency Without the Need for External Cache Control
- A Hit Pin Outputs Status of On-chip Page Hit/Miss Comparators to Simplify Control
- Output Latch Enable Allows Extended Data Output and Faster System Operation (Hyper Page Mode)
- Hidden Precharge Cycles
- Hidden Refresh Cycles
- Write-per-bit Option (DM2213) for Parity and Video Applications
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- Low Profile 300-Mil 44-Pin TSOP-II Package

Description

The Ramtron 4Mb enhanced DRAM (EDRAM) combines raw speed with innovative architecture to offer the optimum cost-performance solution for high performance local or main memory in computer and embedded control systems. In most high speed applications, zero-wait-state operation can be achieved without secondary SRAM cache for system clock speeds of up to 66MHz without interleaving or 132MHz with two-way interleaving. The EDRAM outperforms conventional SRAM cache plus DRAM or synchronous DRAM memory systems by minimizing wait states on initial reads (hit or miss) and by eliminating writeback delays. Architectural similarity with JEDEC DRAMs allows a single memory controller design to support either slow JEDEC DRAMs or high speed EDRAMs. A system designed in this manner can provide a simple upgrade path to higher system performance.

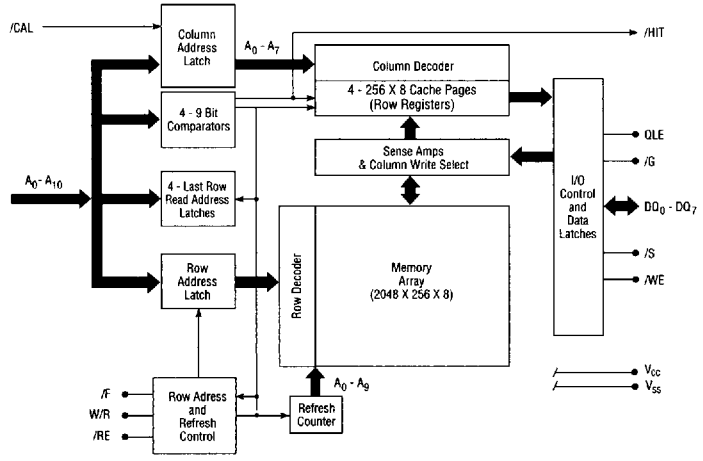
The 512K x 8 EDRAM has the same control and address interface as Ramtron's 4M x 1 and 1M x 4 EDRAM products so that EDRAMs of different organizations can be supported with the same controller design. The 512K x 8 EDRAM implements the following additional features which can be supported on new designs:

- A controllable output latch provides an enhanced "extended data out" or "hyper page mode."
- Cache size is increased from 2Kbits to 8Kbits. The 8Kbit cache is organized as four 256 x 8 direct mapped row registers.
- A hit pin is provided to tell the memory controller when a hit occurs to one of the on-chip cache row registers.

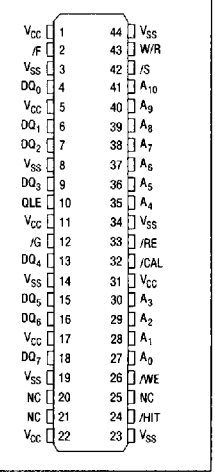
Architecture

The EDRAM architecture has a simple integrated SRAM cache which allows it to operate much like a page mode or static column DRAM.

Functional Diagram



Pin Configuration



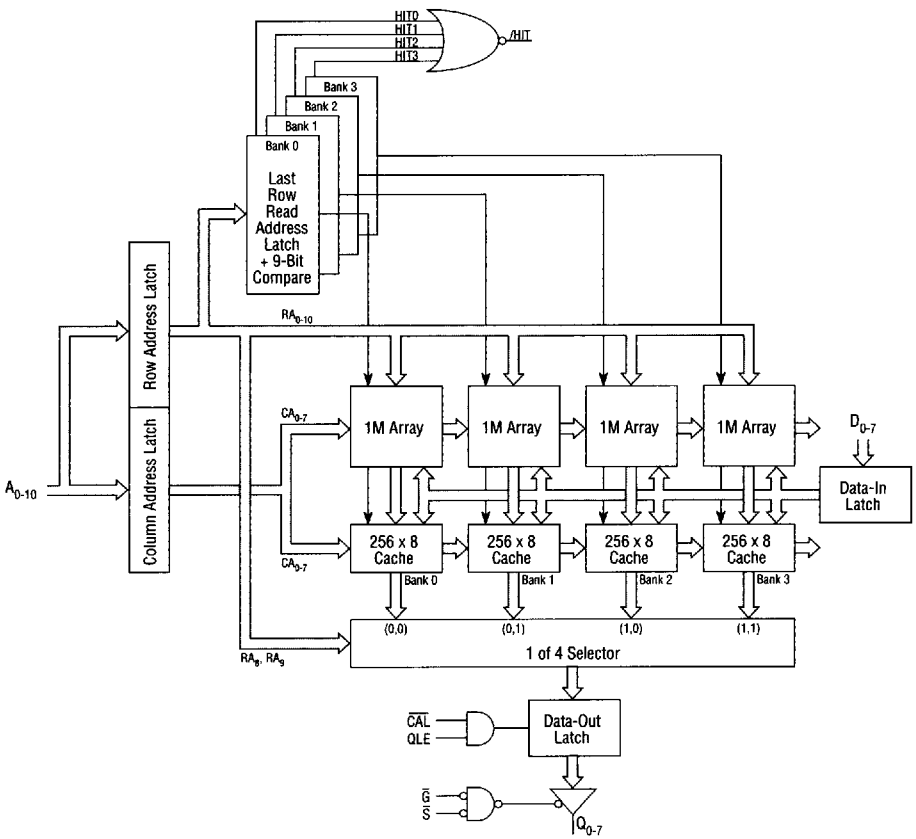
The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. The 512K x 8 EDRAM has a total of four independent DRAM memory banks each with its own 256 x 8 SRAM row register. Memory reads always occur from the cache row register of one of these banks as specified by row address bits A_8 and A_9 (bank select). When the internal comparator detects that the row address matches the last row read from any of the four DRAM banks (page hit), the SRAM is accessed and data is available on the output pins in 15ns from column address input. The /HIT pin is driven low during a page hit to signify to the DRAM control logic that data is available early. Subsequent reads within the page (burst reads or random reads) can continue at 15ns cycle time. When the row address does not match the last row read from any of the four DRAM banks (page miss), the new DRAM row is accessed and loaded into the appropriate SRAM row register and data is available on the output pins all within 35ns from row enable. In this case, the /HIT pin is driven high to signify to the control logic that data is available later. Subsequent reads within the page (burst reads or random reads) can continue at 15ns cycle time. During either read hit or read miss operations, a user controllable on-chip output data latch can be used to extend data output time to allow use of the full 66Mbyte/second bandwidth.

Since reads occur from the SRAM cache, the DRAM precharge can occur during burst reads. This eliminates the precharge time delay suffered by other DRAMs and SDRAMs when accessing a new page. The EDRAM has an independent on-chip refresh counter and dedicated refresh control pin to allow the DRAM array to be refreshed concurrently with cache read operations (hidden refresh).

During EDRAM read accesses, data can be accessed in either static column or page mode depending upon the operation of the /CAL input. If /CAL is held high, new data is accessed with each new column address (static column mode). If /CAL is brought low during a read access, the column address is latched and new data will not be accessed until both the column address is changed and /CAL is brought high (page mode). A separate /G with fast (5ns) access time is used to enable data to the output pins. It can be used to accommodate high speed interleaving without external muxing.

Memory writes are posted to the input data latch and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. Random or page mode writes can be posted 5ns after column address and data are available. The EDRAM allows 15ns page mode cycle time for both write hits and write misses. Memory writes do not affect the contents of the cache row

Four Bank Cache Architecture



register except during a cache hit. Since the DRAM array can be written to at SRAM speeds, there is no need for complex writeback schemes.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance without any significant increase in die size over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during reads and maximize hit rate by maintaining page cache contents during write operations even if data is written to another memory page. These capabilities, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select row address bits A_8 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F high(1). The EDRAM will compare the new row address to the last row read address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the row and column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. The /HIT output is driven low at time t_{HV} after /RE to indicate the shorter access time to the external control logic. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. Additional locations within the currently active page may be accessed concurrently with precharge by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F high(1). The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row is fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. The /HIT output is driven high at time t_{HV} after /RE to indicate the longer access time to the external control logic. /RE may be brought high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. Additional locations within the currently active page may be accessed by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high(1). The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the appropriate bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched

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EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	$A_{0\text{-}10}$	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	L	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, read operations may be performed while /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 15ns cycle times. During a write hit sequence, the /HIT output is driven low. At the end of any write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high(1). The EDRAM will compare the new row address to the LRR address latch for the bank specified for row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match any of the LRRs, the EDRAM will write data to the DRAM page in the appropriate bank and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, the /HIT output is driven high, cache reads are inhibited, and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with the precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems.

/RE Inactive Operation

Data may be read from the SRAM cache without clocking /RE. This capability allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. In this mode of operation, the cache reads will occur from the page accessed during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. When /RE is inactive, the hit pin is not driven and is in a high impedance state.

This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles.

Function	/S	/G	/CAL	A_{0-7}
Cache Read (Static Column)	L	L	H	Col Adr
Cache Read (Page Mode)	L	L	↕	Col Adr

Output Latch Enable Operation

The 512K x 8 EDRAM has an output latch enable (QLE) that can be used to extend data output valid time. The output latch enable operates as shown in the following table.

When QLE is low, the latch is transparent and the EDRAM operates identically to the standard 4M x 1 and 1M x 4 EDRAMs. When /CAL is high during a static column mode read, the QLE input can be used to latch the output to extend the data output valid time. QLE can be held high during page mode reads. In this case, the data outputs are latched while /CAL is high and open when /CAL is not high.

QLE	/CAL	Comments
L	X	Output Transparent
↕	H	Output Latched When QLE=H (Static Column)
H	↕	Ouput Latched When /CAL=H (Page Mode)

Write-Per-Bit Operation

The DM2213 version of the 512Kb x 8 EDRAM offers a write-per-bit capability which allows single bits of the memory to be selectively written without altering other bits in the same word. This capability may be useful for implementing parity or masking data in video graphics applications. The bits to be written are determined by a bit mask data word which is placed on the I/O data pins DQ_{0-7} prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles where /S can be disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, an /RE only refresh may be performed using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R, /G, and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of eight /RE active initialization cycles (read, write, or refresh) are required before normal operation is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_8 and A_9 define the four internal DRAM banks.

Unallowed Mode

Read, write, or /RE only refresh operations must not be performed to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, the interface to the EDRAM may be simplified to reduce the number of control lines by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The QLE input can be tied low if output latching is not required, or it can be tied high if "extended data out" (hyper page mode) is required. The /HIT output pin is not necessary for device operation. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. The W/R and /G inputs can be tied together if reads are not required during a write hit cycle. If these techniques are used, the EDRAM will require only three control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], and W/R [combined W/R and /G]). The simplified control interface still allows the fast page read/write cycle times, fast random read/ write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the most currently read SRAM row register. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL transitions low, it latches the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles. If QLE is high during a read, /CAL will hold data output until it transitions low.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when /F is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /RE should never be clocked when /S is inactive.

DQ_{0-7} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2213 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 8-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

QLE — Output Latch Enable

This input enables the output latch. When QLE is low, the output latch is transparent. Data is latched when both /CAL and QLE are high. This allows output data to be extended during either static column or page mode read cycles.

/HIT — Hit Pin

This output pin will be driven during /RE active read or write cycles to indicate the hit/miss status of the cycle.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Pin Names

Pin Names	Function
A_{0-10}	Address Inputs
/RE	Row Enable
DQ_{0-7}	Data In/Data Out
/CAL	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)
V_{SS}	Ground

Pin Names	Function
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select
/HIT	Hit Output
QLE	Output Latch Enable
NC	Not Connected

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ V_{CC}+1
Output Voltage (V_{OUT})	- 1 ~ V_{CC}+1
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

*One output at a time; short duration.

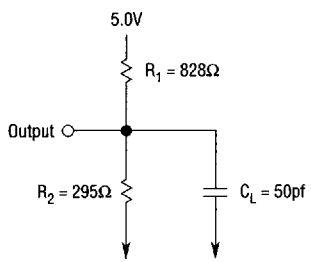
Capacitance

Description	Max	Pins
Input Capacitance	7pf	A_{0-10}, /WE, /S
Input Capacitance	10pf	/RE, /CAL
Input Capacitance	3pf	/G, /F, QLE, W/R
Output Capacitance	6pf	/HIT
I/O Capacitance	6pf	DQ_{0-7}

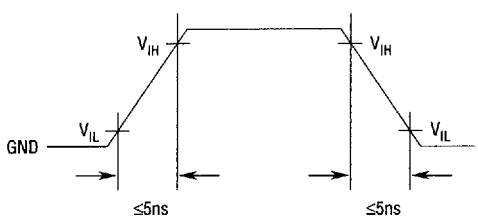
AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}

V_{OUT} Timing Referenced to 1.5 Volts



Load Circuit



Input Waveforms

Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	V_{CC}+1	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$V_{I(L)}$	Input Leakage Current	-10µA	10µA	0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V
$V_{O(L)}$	Output Leakage Current	-10µA	10µA	0V ≤ V_{IN}, 0V ≤ V_{OUT} ≤ 5.5V

Symbol	Operating Current	33MHz Typ(1)	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	110mA	225mA	180mA	/RE, /CAL, /G and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC2}	Fast Page Mode Read	65mA	145mA	115mA	/CAL, /G and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC3}	Static Column Read	55mA	110mA	90mA	/G and Addresses Cycling: t_{AC} = t_{AC} Minimum	2, 4
I_{CC4}	Random Write	135mA	190mA	150mA	/RE, /CAL, /WE and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC5}	Fast Page Mode Write	50mA	135mA	105mA	/CAL, /WE and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC6}	Standby	1mA	1mA	1mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	30mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}

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Switching Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}(1)	Column Address Access Time		15		20	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{ACI}	Address Valid to /CAL Inactive (QLE High)	15		20		ns
t_{AHQ}	Column Address Hold From QLE High (/CAL=H)	0		0		ns
t_{AQH}	Address Valid to QLE High	15		20		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CLV}	Column Address Latch Low to Data Valid (QLE High)		7		10	ns
t_{CQH}	Data Hold From /CAL ↓ Transaction (QLE High)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		15		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1.5		2		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		6		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}(1)	Output Enable Access Time		5		6	ns
t_{GQX}(2,3)	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}(4,5)	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{HV}	Hit Valid From Row Enable		5		6	ns
t_{HZ}	Hit Turn-Off From Row Enable Going High	0		0		ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{QCI}	QLE High to /CAL Inactive	0		0		ns
t_{QH}	QLE High Time	5		6		ns

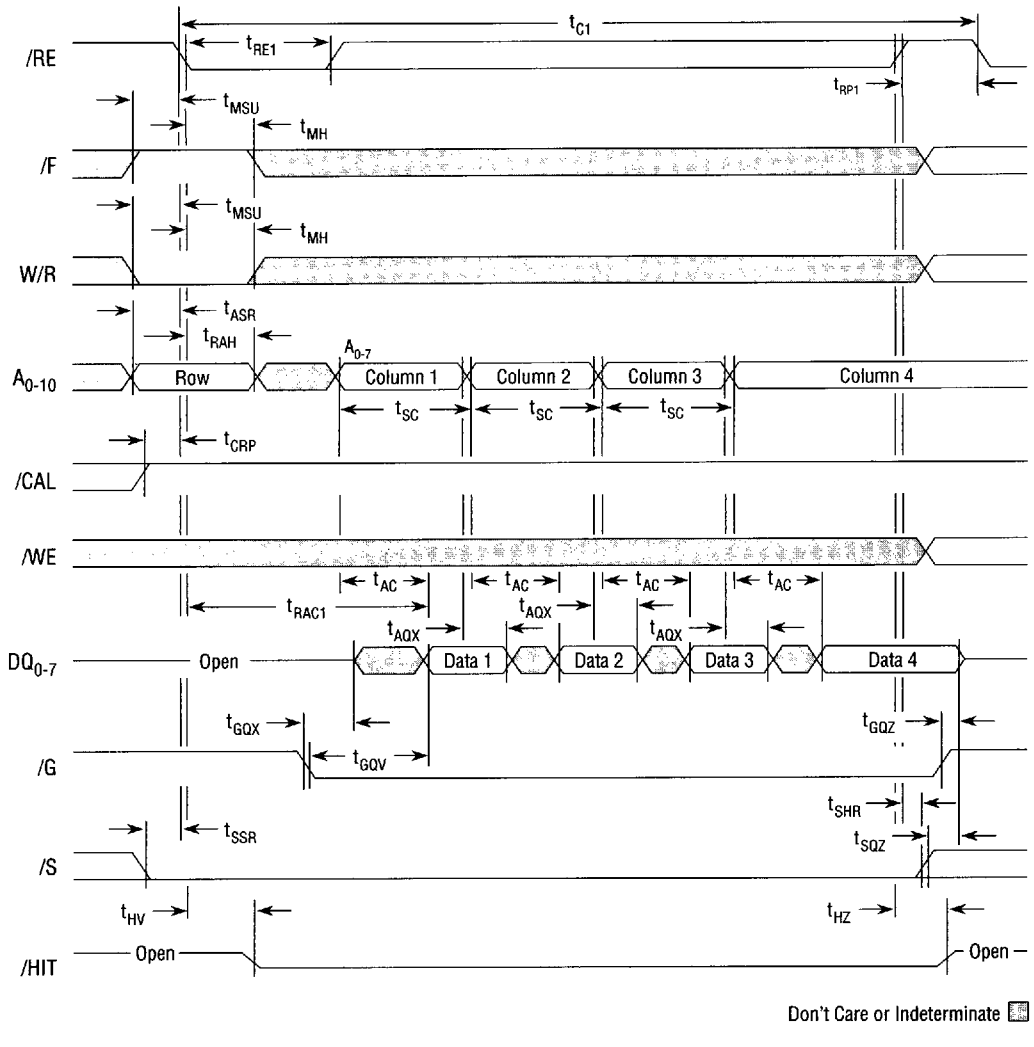
Switching Characteristics (continued)

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

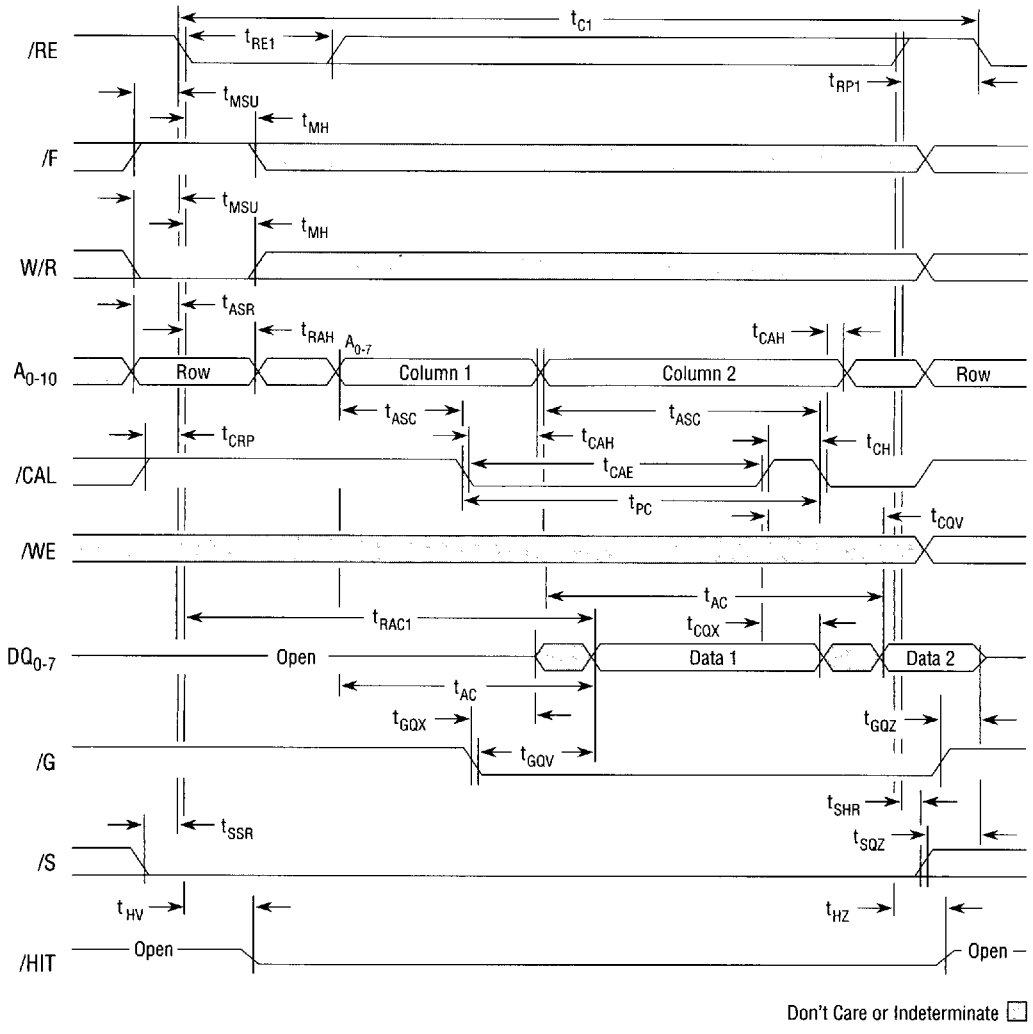
Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{QL}	QLE Low Time	5		6		ns
t_{QQH}	Data Hold From QLE Inactive	2		3		ns
t_{QQV}	Data Valid From QLE Low		7.5		10	ns
t_{RAC}(1)	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}(1)	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), DQ = Hi-Z	10		13		ns
t_{RP}	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Write Enable Don't Care From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}(6)	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		15		20	ns

(1) V_{OUT} Timing Reference Point at 1.5V
(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}
(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal
(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}
(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal
(6) On DM2213, t_{WHR} Minimum is t_{DS}

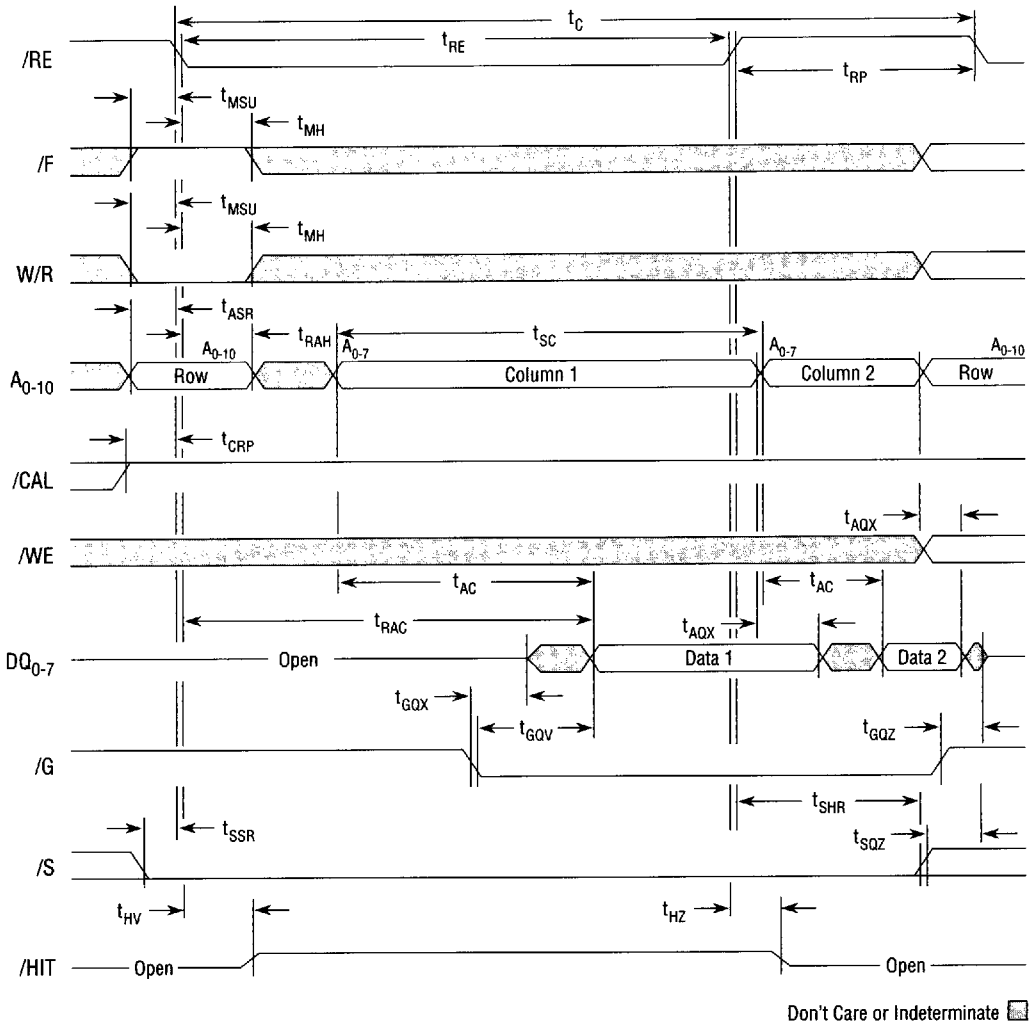
/RE Active Cache Read Hit (Static Column Mode)



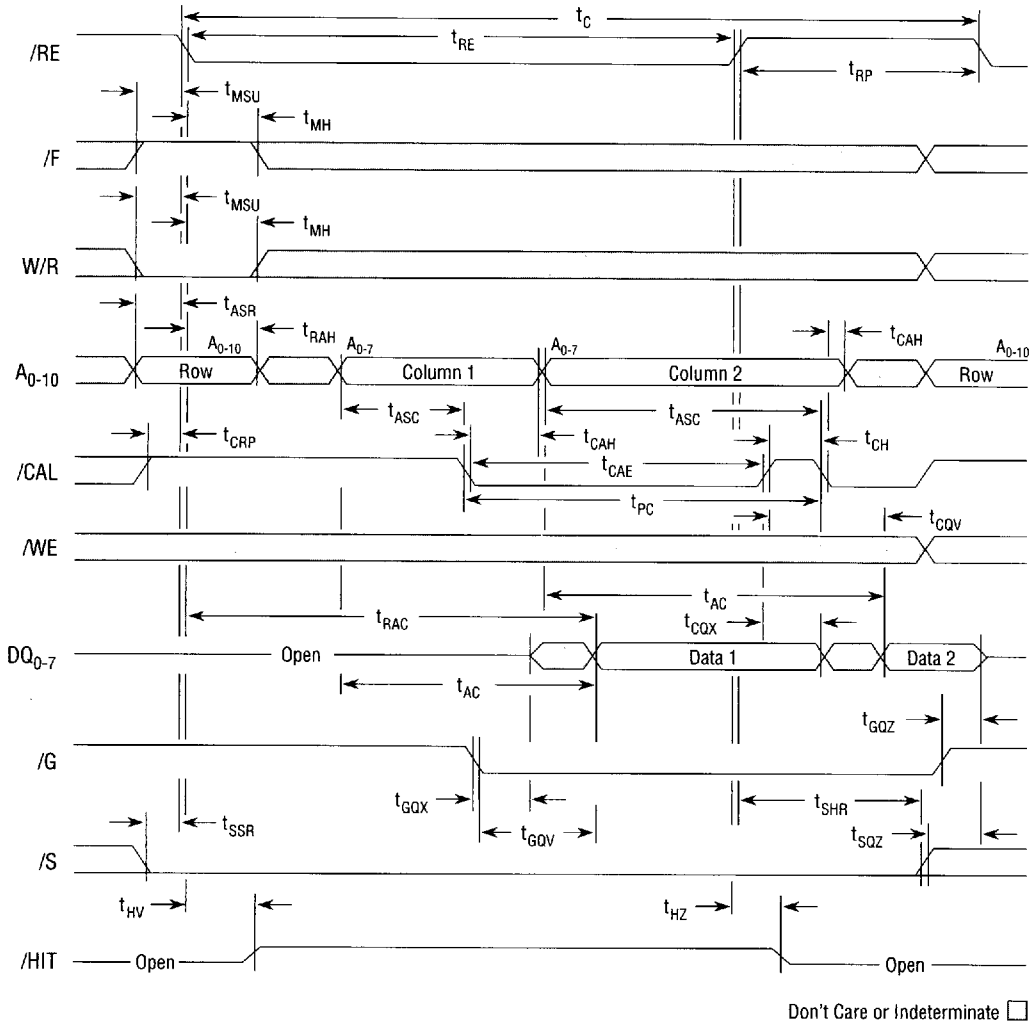
/RE Active Cache Read Hit (Page Mode)



/RE Active Cache Read Miss (Static Column Mode)

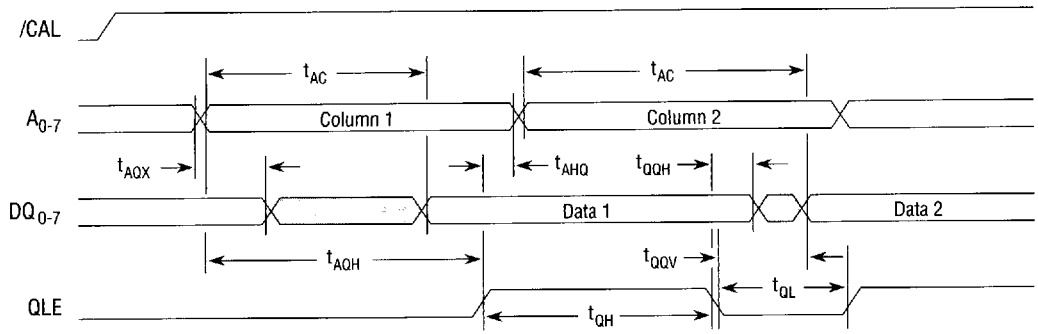


/RE Active Cache Read Miss (Page Mode)

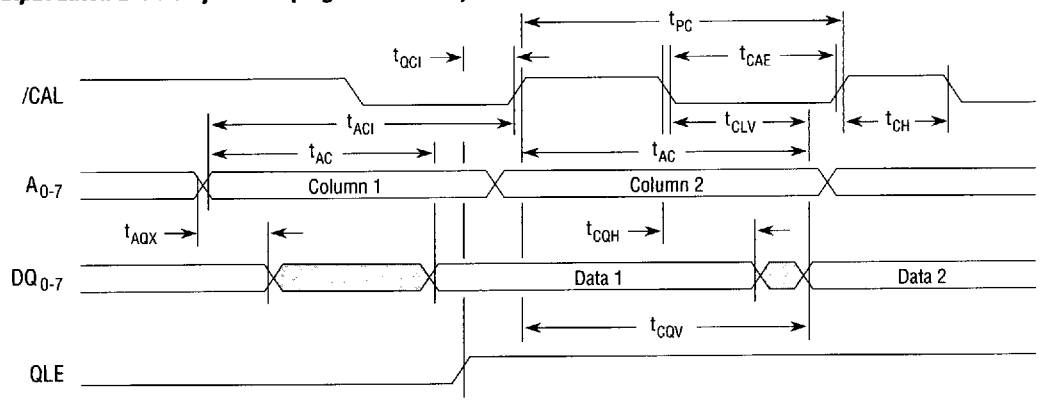


2

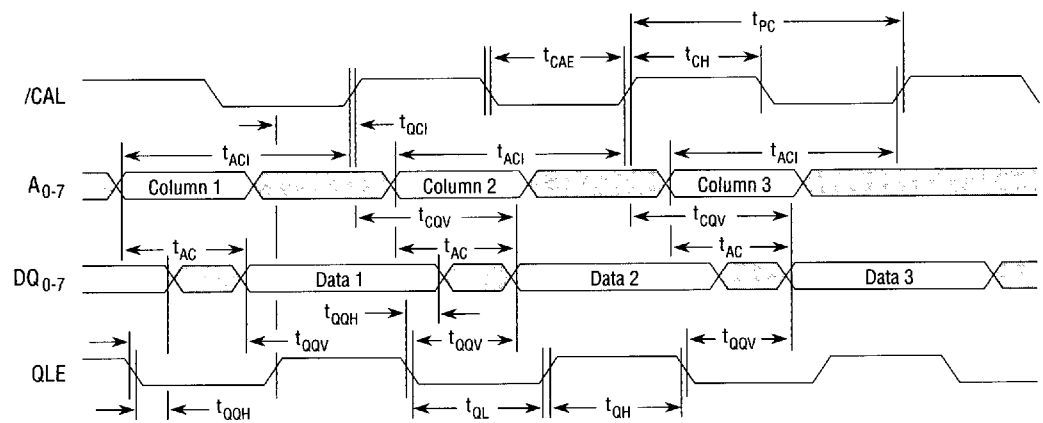
Output Latch Enable Operation (Static Column Mode Read)



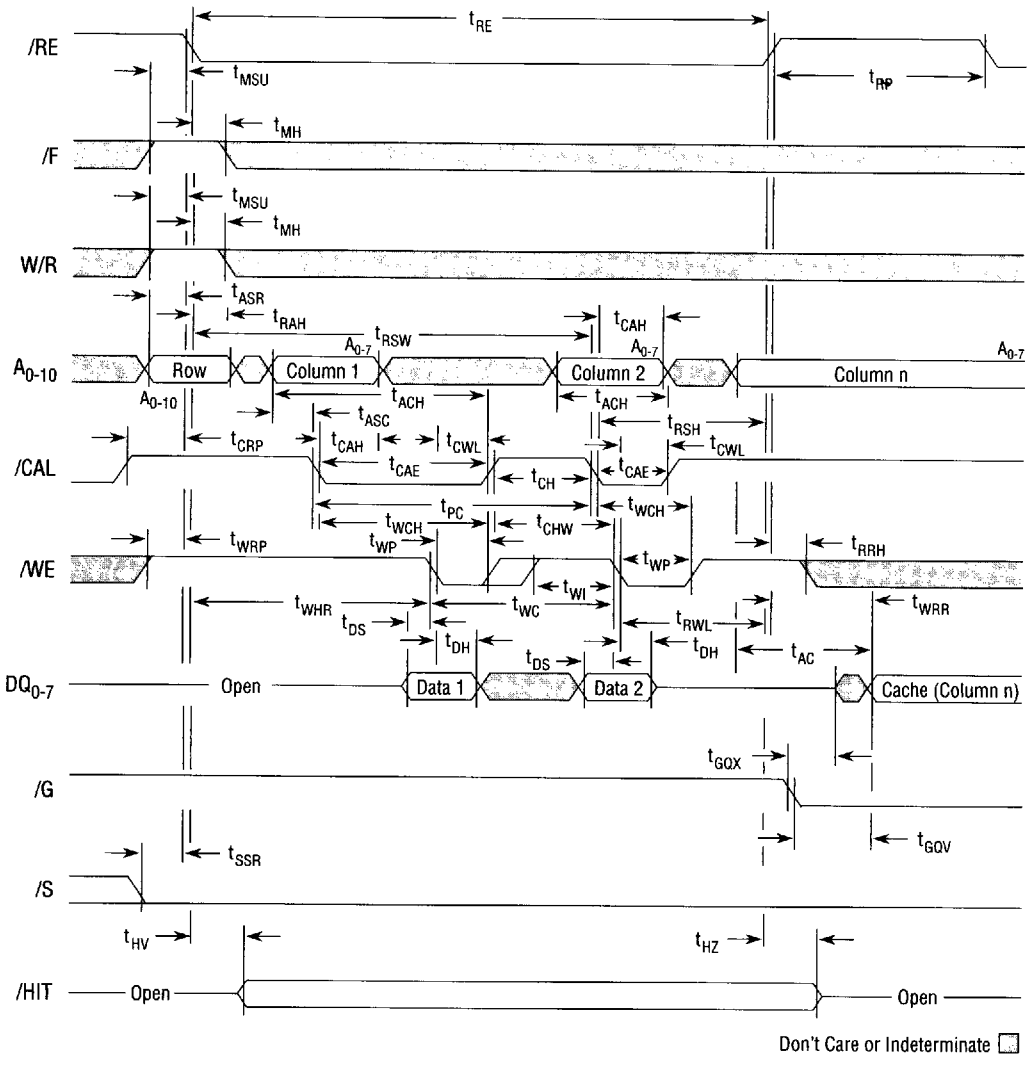
Output Latch Enable Operation (Page Mode Read)



Output Latch Enable Operation (Asynchronous Access)

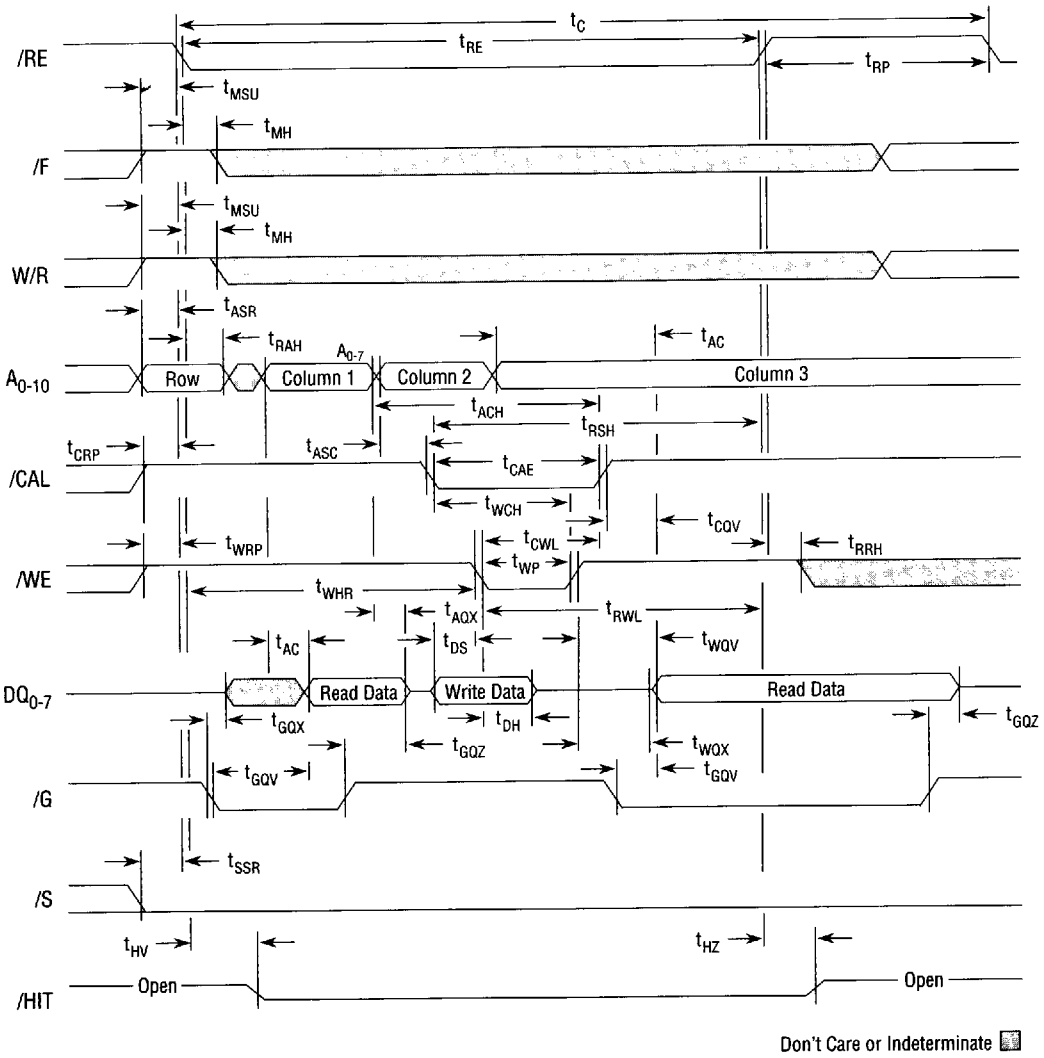


Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



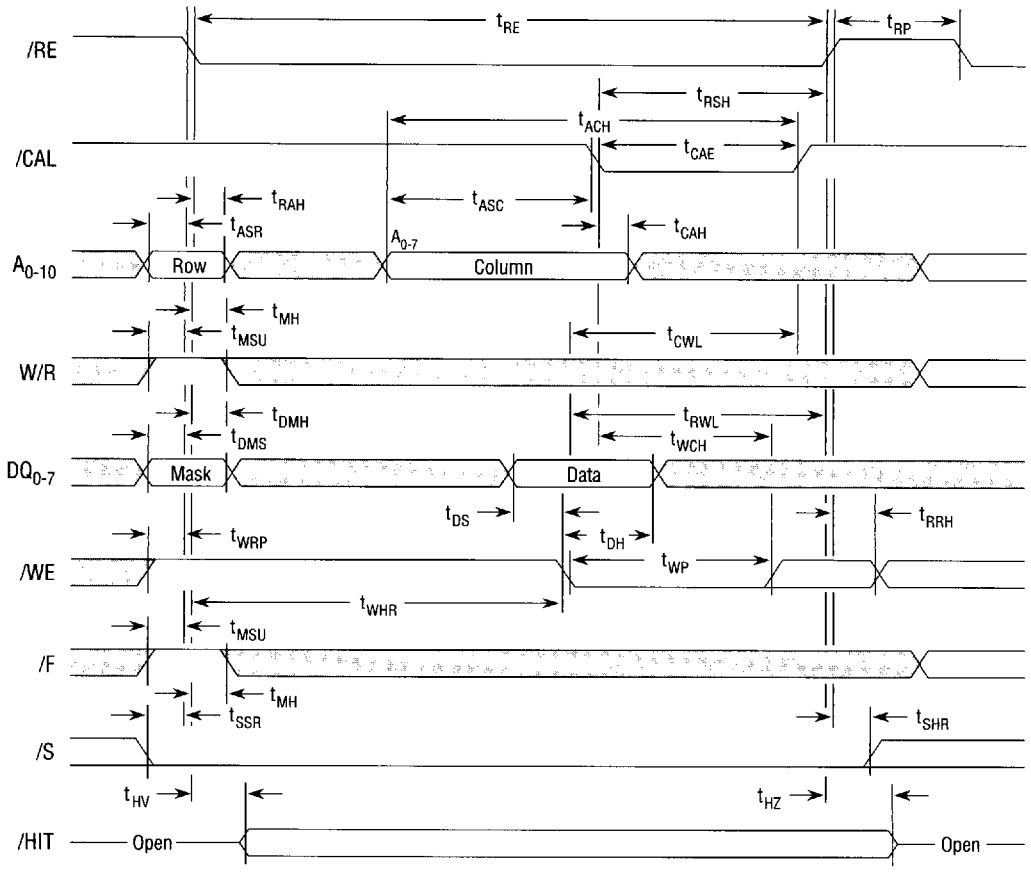
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.

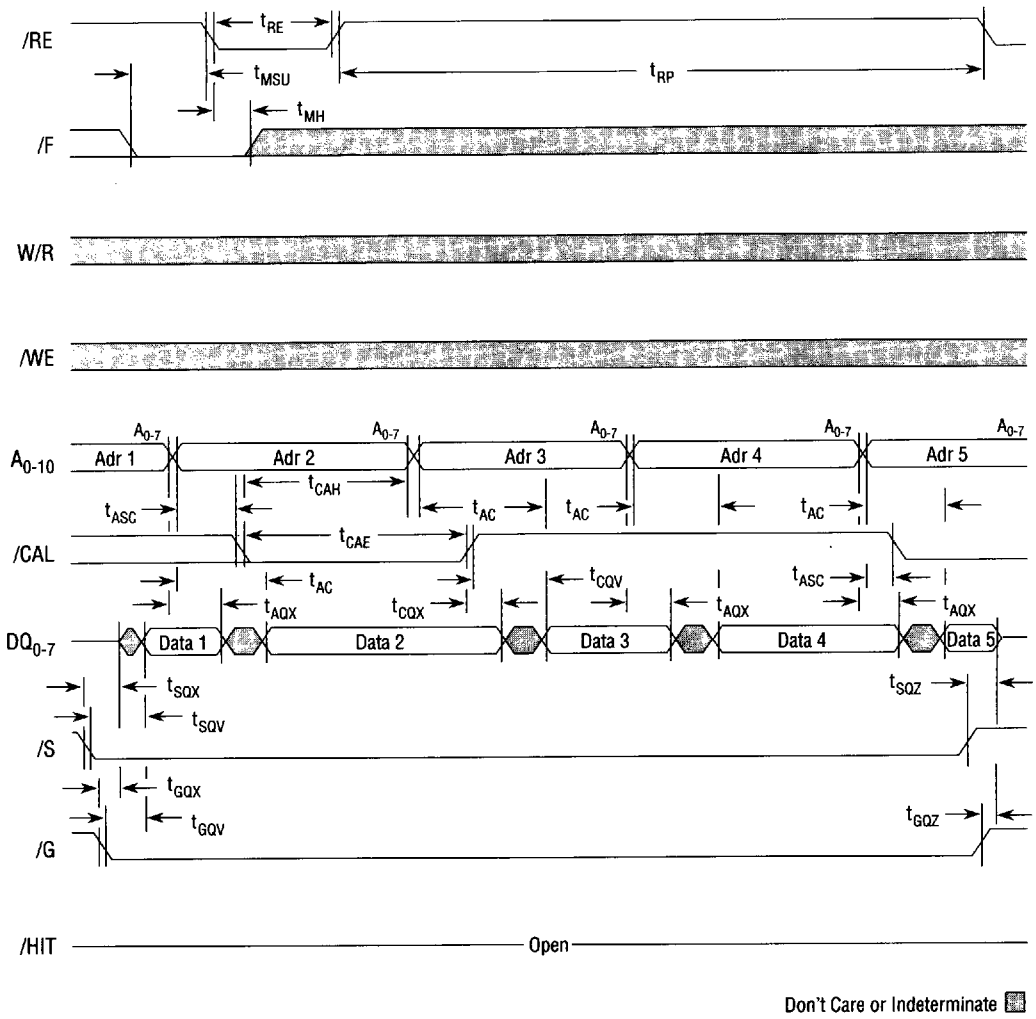
Write-Per-Bit Cycle (/G=High)



NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.
2. Write-per-bit cycle valid only for DM2213.

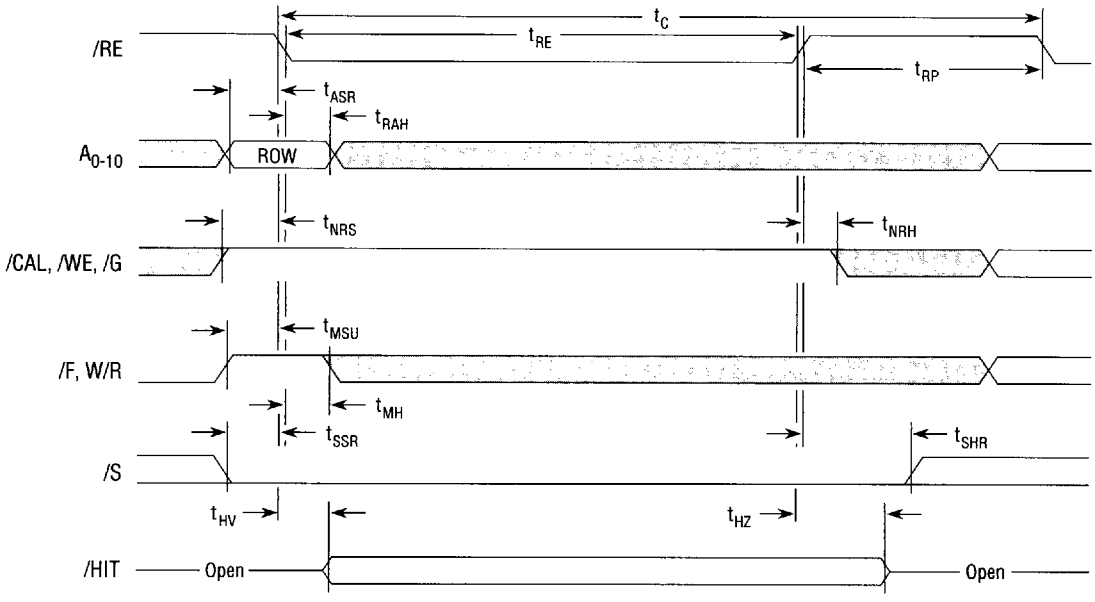
2

Hidden /F Refresh Cycle During Page Mode and Static Column Cache Reads



NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

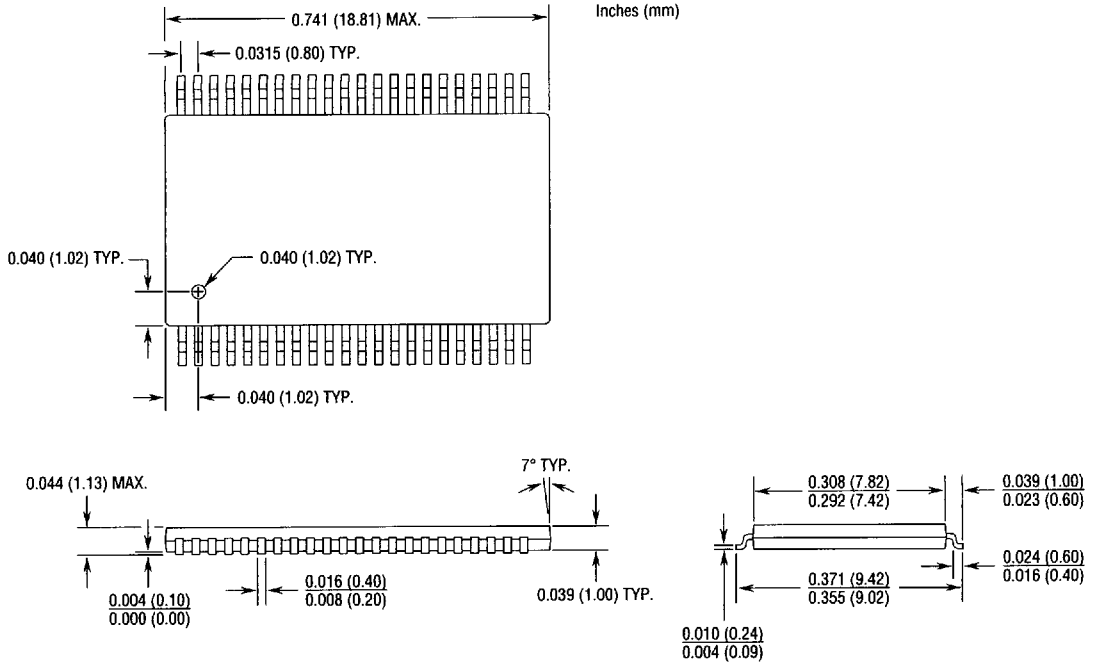
/RE-Only Refresh



NOTES: 1. All binary combinations of A_{0-9} must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.
2. /RE refresh is write cycle with no /CAL active cycle.

2

Mechanical Data
44 Pin 300 Mil Plastic TSOP Package



Part Numbering System

DM2203T - 15

Access Time from Cache in Nanoseconds
15ns
20ns

Packaging System
T = 300 Mil, TSOP

I/O Width
i.e., Power to Which 2 is Raised for I/O Width

Special Features Field
0 = No Write Per Bit
1 = Write Per Bit

Capacity in Bits
i.e., Power to Which 2 is Raised for Total Capacity

Dynamic Memory