Integrated Device Technology, Inc.

# FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

**ADVANCE INFORMATION**
**IDT54/74FCT16245T/AT/CT/ET**
**IDT54/74FCT162245T/AT/CT/ET**
**IDT54/74FCT166245T/AT/CT**
**IDT54/74FCT162H245T/AT/CT/ET**

## FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16245T/AT/CT/ET:**
  - High drive outputs (-32mA $I_{OH}$, 64mA $I_{OL}$)
  - Power off disable outputs permit "live insertion"
  - Typical $V_{OLP}$ (Output Ground Bounce) < 1.0V at $V_{CC}$ = 5V, $T_A$ = 25°C
- **Features for FCT162245T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical $V_{OLP}$ (Output Ground Bounce) < 0.6V at $V_{CC}$ = 5V, $T_A$ = 25°C

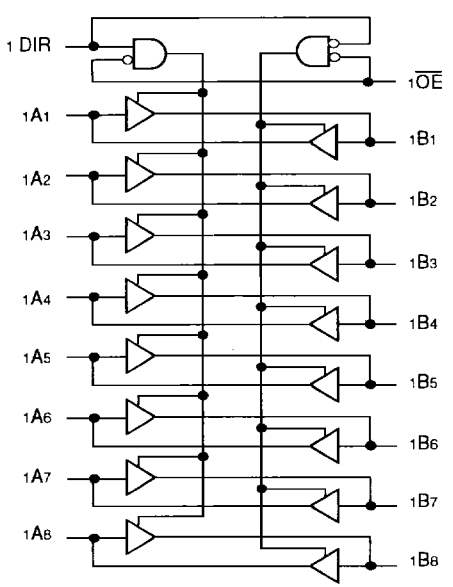
## DESCRIPTION:

The 16-bit transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($x\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

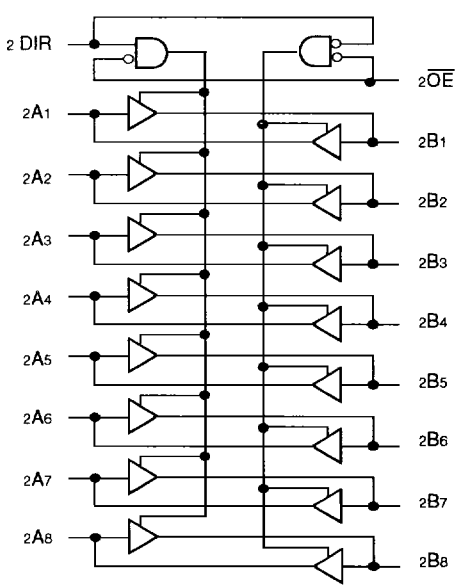
The IDT54/74FCT16245T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162245T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162245T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16245T/AT/CT/ET and 54/74ABT16245 for on-board interface applications.

## FUNCTIONAL BLOCK DIAGRAM




2545 drw 01




2545 drw 02

## FEATURES: (Cont'd.)

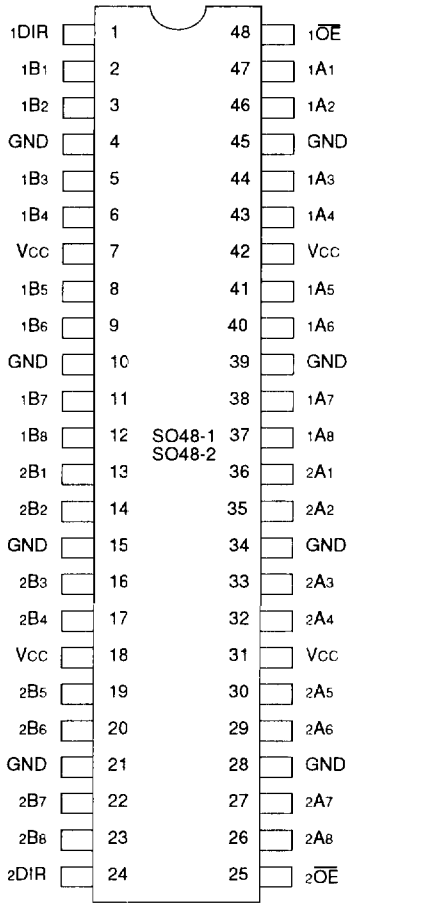
- **Features for FCT166245T/AT/CT:**
  - Light Drive Balanced Output: ±8mA (commercial), ±6mA (military)
  - Minimal system switching noise
  - Typical $V_{OLP}$ (Output Ground Bounce) < 0.4V at $V_{CC}$ = 5V, $T_A$ = 25°C
- **Features for FCT162H245T/AT/CT/ET:**
  - Bus Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

## DESCRIPTION: (Cont'd.)

The IDT54/74FCT166245T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<50pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

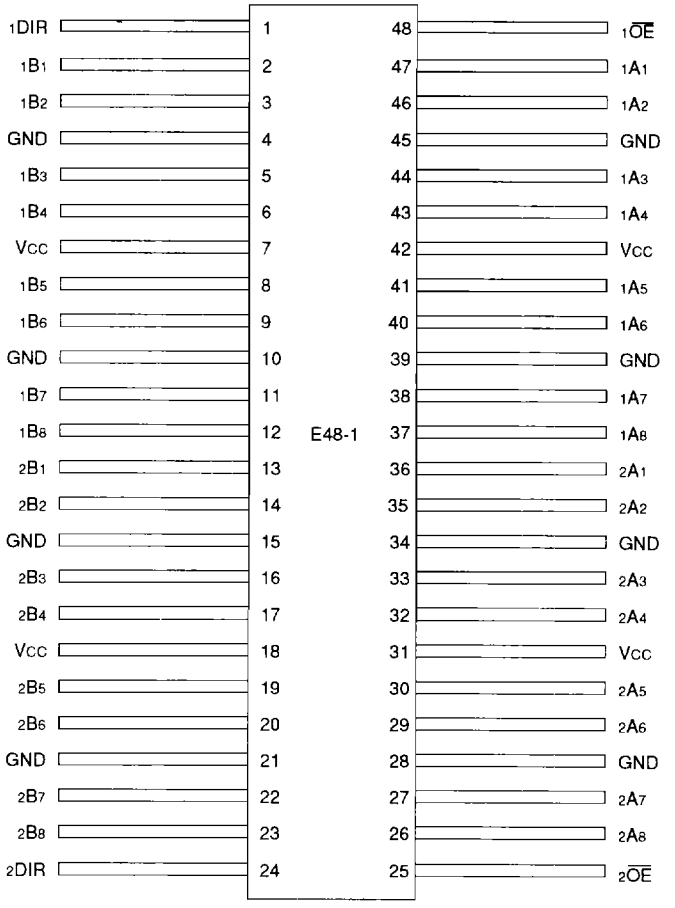
The IDT54/74FCT162H245T/AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

## PIN CONFIGURATIONS




2545 drw 03

**SSOP**
**TSSOP**
**TOP VIEW**




2545 drw 04

**CERPACK**
**TOP VIEW**

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## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| x$\overline{OE}$ | Output Enable Input (Active LOW) |
| xDIR | Direction Control Input |
| xAx | Side A Inputs or 3-State Outputs(1) |
| xBx | Side B Inputs or 3-State Outputs(1) |

**NOTE:** 2545 tbl 01
1. On FCT162H245T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

## FUNCTION TABLE(1)

| Inputs | | Outputs |
|---|---|---|
| x$\overline{OE}$ | xDIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

**NOTE:** 2545 tbl 02
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –40 to +85 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | 1.0 | W |
| $I_{OUT}$ | DC Output Current | –60 to +120 | –60 to +120 | mA |

**NOTES:** 2545 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT and FCT166XXXT.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 3.5 | 6.0 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 0V | 3.5 | 8.0 | pF |

**NOTE:** 2545 lnk 04
1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ± 10%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current (Input pins)[5] | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| | Input HIGH Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{IL}$ | Input LOW Current (Input pins)[5] | | $V_I$ = GND | — | — | ±1 | |
| | Input LOW Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[5] | | $V_O$ = 0.5V | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –80 | –140 | –225 | mA |
| $I_O$ | Output Drive Current | $V_{CC}$ = Max., $V_O$ = 2.5V[3] | | –50 | — | –180 | mA |
| $V_H$ | Input Hysteresis | — | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

2545 lnk 05

## OUTPUT DRIVE CHARACTERISTICS FOR FCT16245T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –3mA | 2.5 | 3.5 | — | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –12mA MIL.<br>$I_{OH}$ = –15mA COM'L. | 2.4 | 3.5 | — | V |
| | | | $I_{OH}$ = –24mA MIL.<br>$I_{OH}$ = –32mA COM'L.[4] | 2.0 | 3.0 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 48mA MIL.<br>$I_{OL}$ = 64mA COM'L. | — | 0.2 | 0.55 | V |
| $I_{OFF}$ | Input/Output Power Off Leakage[5] | $V_{CC}$ = 0V, $V_{IN}$ or $V_O$ ≤ 4.5V | | — | — | ±1 | µA |

2545 lnk 06

## OUTPUT DRIVE CHARACTERISTICS FOR FCT162245T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{ODL}$ | Output LOW Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | 60 | 115 | 150 | mA |
| $I_{ODH}$ | Output HIGH Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | –60 | –115 | –150 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –16mA MIL.<br>$I_{OH}$ = –24mA COM'L. | 2.4 | 3.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA MIL.<br>$I_{OL}$ = 24mA COM'L. | — | 0.3 | 0.55 | V |

2545 lnk 07

## OUTPUT DRIVE CHARACTERISTICS FOR FCT166245T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{ODL}$ | Output LOW Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | 16 | 48 | 96 | mA |
| $I_{ODH}$ | Output HIGH Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | –16 | –48 | –96 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –6mA MIL.<br>$I_{OH}$ = –8mA COM'L. | 2.4 | 3.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 6mA MIL.<br>$I_{OL}$ = 8mA COM'L. | — | 0.3 | 0.55 | V |

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**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at $T_A$ = –55°C.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ± 10%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[4] | Standard Input[5] | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| | | Standard I/O[5] | | | — | — | ±1 | |
| | | Bus Hold Input | | | — | — | ±100 | |
| | | Bus Hold I/O | | | — | — | ±100 | |
| $I_{IL}$ | Input LOW Current[4] | Standard Input[5] | | $V_I$ = GND | — | — | ±1 | |
| | | Standard I/O[5] | | | — | — | ±1 | |
| | | Bus Hold Input | | | — | — | ±100 | |
| | | Bus Hold I/O | | | — | — | ±100 | |
| $I_{BHH}$ | Bus Hold | Bus Hold Input | $V_{CC}$ = Min. | $V_I$ = 2.0V | –50 | — | — | µA |
| $I_{BHL}$ | Sustain Current[4] | | | $V_I$ = 0.8V | +50 | — | — | |
| $I_{BHHO}$ | Bus Hold | Bus Hold Input | $V_{CC}$ = Max. | $V_I$ = 1.5V | — | — | TBD | mA |
| $I_{BHLO}$ | Overdrive Current[4] | | | | — | — | TBD | |
| $I_{OZH}$ | High Impedance Output Current | | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[5] | | | $V_O$ = 0.5V | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | | $V_{CC}$ = Max., $V_O$ = GND[3] | | –80 | –140 | –225 | mA |
| $I_O$ | Output Drive Current | | $V_{CC}$ = Max., $V_O$ = 2.5V[3] | | –50 | — | –180 | mA |
| $V_H$ | Input Hysteresis | | — | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ $I_{CCZ}$ | Quiescent Power Supply Current | | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

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**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at $T_A$ = –55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$x\overline{OE}$ = xDIR = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 60 | 100 | µA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>$f_i$ = 10MHz<br>50% Duty Cycle<br>$x\overline{OE}$ = xDIR = GND<br>One Bit Toggling | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.6 | 1.5 | mA |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 0.9 | 2.3 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_i$ = 2.5MHz<br>50% Duty Cycle<br>$x\overline{OE}$ = xDIR = GND<br>Sixteen Bits Toggling | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 2.4 | 4.5[5] | |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 6.4 | 16.5[5] | |

2545 tbl 10

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

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## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | FCT16245T/162245T[5] | | | | FCT16245AT/162245AT[5] | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| tPLH<br>tPHL | Propagation Delay<br>A to B, B to A | CL = 50pF<br>RL = 500Ω | 1.5 | 7.0 | 1.5 | 7.5 | 1.5 | 4.6 | 1.5 | 4.9 | ns |
| tPZH<br>tPZL | Output Enable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 9.5 | 1.5 | 10.0 | 1.5 | 6.2 | 1.5 | 6.5 | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 7.5 | 1.5 | 10.0 | 1.5 | 5.0 | 1.5 | 6.0 | ns |
| tPZH<br>tPZL | Output Enable Time<br>xDIR to A or B[4] | | 1.5 | 9.5 | 1.5 | 10.0 | 1.5 | 6.2 | 1.5 | 6.5 | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>xDIR to A or B[4] | | 1.5 | 7.5 | 1.5 | 10.0 | 1.5 | 5.0 | 1.5 | 6.0 | ns |
| tSK(o) | Output Skew[3] | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |

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| Symbol | Parameter | Condition[1] | FCT16245CT/162245CT[5] | | | | FCT16245ET/162245ET[5] | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| tPLH<br>tPHL | Propagation Delay<br>A to B, B to A | CL = 50pF<br>RL = 500Ω | 1.5 | 4.1 | 1.5 | 4.5 | 1.5 | 3.2 | — | — | ns |
| tPZH<br>tPZL | Output Enable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 5.8 | 1.5 | 6.2 | 1.5 | 4.4 | — | — | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 4.8 | 1.5 | 5.2 | 1.5 | 4.0 | — | — | ns |
| tPZH<br>tPZL | Output Enable Time<br>xDIR to A or B[4] | | 1.5 | 5.8 | 1.5 | 6.2 | 1.5 | 4.8 | — | — | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>xDIR to A or B[4] | | 1.5 | 4.8 | 1.5 | 5.2 | 1.5 | 4.0 | — | — | ns |
| tSK(o) | Output Skew[3] | | — | 0.5 | — | 0.5 | — | 0.5 | — | — | ns |

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| Symbol | Parameter | Condition[1] | FCT166245T | | | | FCT166245AT | | | | FCT166245CT | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| tPLH<br>tPHL | Propagation Delay<br>A to B, B to A | CL = 50pF<br>RL = 500Ω | 1.5 | 7.0 | 1.5 | 7.5 | 1.5 | 4.6 | 1.5 | 4.9 | 1.5 | 4.1 | 1.5 | 4.5 | ns |
| tPZH<br>tPZL | Output Enable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 9.5 | 1.5 | 10.0 | 1.5 | 6.2 | 1.5 | 6.5 | 1.5 | 5.8 | 1.5 | 6.2 | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>x$\overline{OE}$ to A or B | | 1.5 | 7.5 | 1.5 | 10.0 | 1.5 | 5.0 | 1.5 | 6.0 | 1.5 | 4.8 | 1.5 | 5.2 | ns |
| tPZH<br>tPZL | Output Enable Time<br>xDIR to A or B[4] | | 1.5 | 9.5 | 1.5 | 10.0 | 1.5 | 6.2 | 1.5 | 6.5 | 1.5 | 5.8 | 1.5 | 6.2 | ns |
| tPHZ<br>tPLZ | Output Disable Time<br>xDIR to A or B[4] | | 1.5 | 7.5 | 1.5 | 10.0 | 1.5 | 5.0 | 1.5 | 6.0 | 1.5 | 4.8 | 1.5 | 5.2 | ns |
| tSK(o) | Output Skew[3] | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |

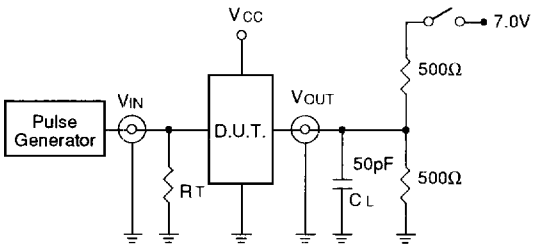
2545 tbl 13

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.
5. Including parts with Bus Hold

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




2545 drw 05

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

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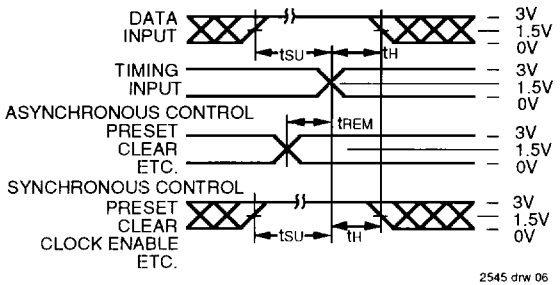
**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES

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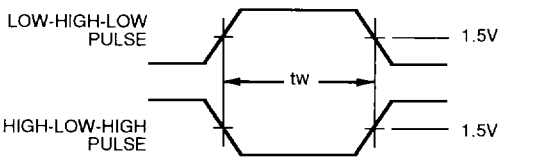
## PULSE WIDTH

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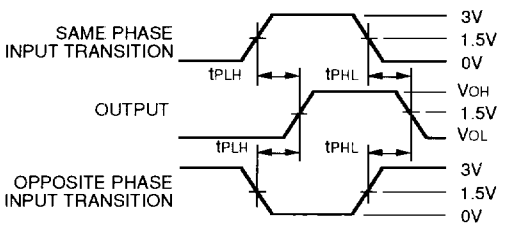
## PROPAGATION DELAY

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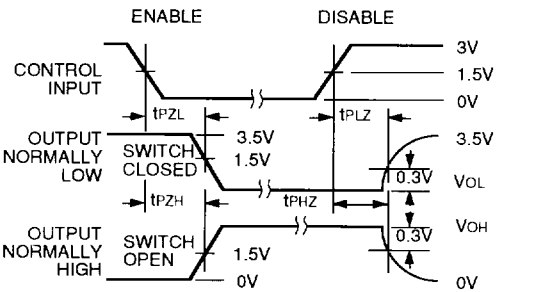
## ENABLE AND DISABLE TIMES

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**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

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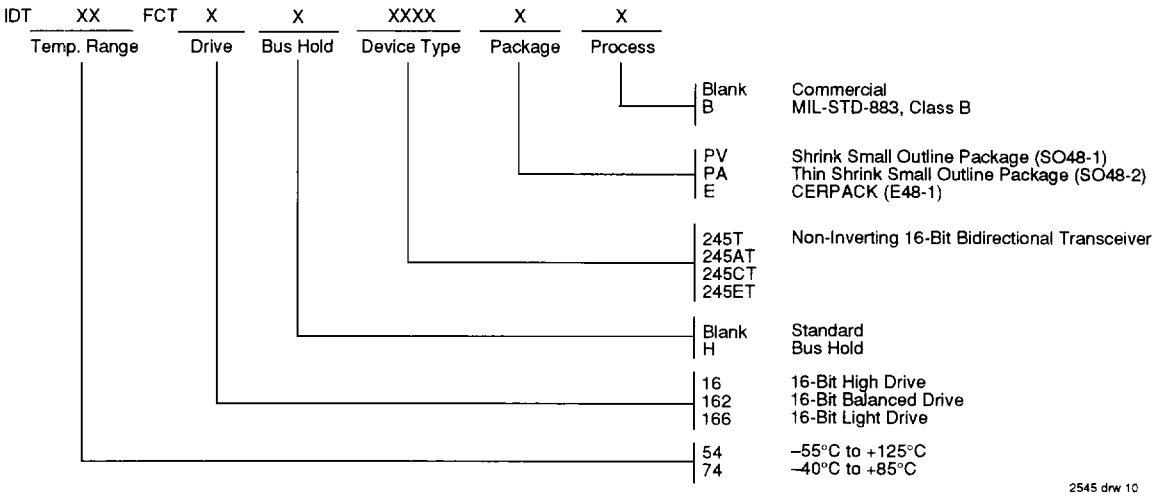
## ORDERING INFORMATION




2545 drw 10