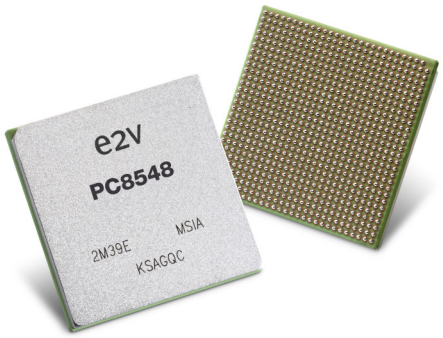
PC8548E
PowerQUICC III Integrated Processor

Datasheet - *Preliminary Specification*

Features



- Embedded e500 Core, Initial Offerings up to 1.2 GHz
  - Dual Dispatch Superscalar, 7-stage Pipeline Design with out-of-order Issue and Execution
  - 3065 MIPS at 1333 MHz (Estimated Dhrystone 2.1)
- 36-bit Physical Addressing
- Enhanced Hardware and Software Debug Support
- Double-precision Embedded Scalar and Vector Floating-point APUs
- Memory Management Unit (MMU)
- Integrated L1/L2 Cache
  - L1 Cache-32 KB Data and 32 KB Instruction Cache with Line-locking Support
  - L2 Cache-512 KB (8-Way Set Associative); 512 KB/256 KB/128 KB/64 KB Can Be Used As SRAM
  - L1 and L2 Hardware Coherency
  - L2 Configurable As SRAM, Cache and I/O Transactions Can Be Stashed Into L2 Cache Regions
- Integrated DDR Memory Controller With Full ECC Support, Supporting:
  - 200 MHz Clock Rate (400 MHz Data Rate), 64-bit, 2.5V/2.6V I/O, DDR SDRAM
- Integrated Security Engine Supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 Encryption Algorithms
- Four On-chip Triple-speed Ethernet Controllers (GMACs) Supporting 10- and 100-Mbps, and 1-Gbps Ethernet/IEEE*802.3 Networks with MII, RMII, GMII, RGMII, RTBI and TBI Physical Interfaces
  - TCP/IP Checksum Acceleration
  - Advanced QoS Features
- General-purpose I/O (GPIO)
- Serial RapidIO and PCI Express High-speed Interconnect Interfaces, Supporting
  - Single x8 PCI Express, or Single x4 PCI Express and Single 4x Serial RapidIO
- On-chip Network (OCeaN) Switch Fabric
- Multiple PCI Interface Support
  - 64-bit PCI 2.2 Bus Controller (Up to 66 MHz, 3.3V I/O)
  - 64-bit PCI-X Bus Controller (Up to 133 MHz, 3.3V I/O), or Flexibility to Configure Two 32-bit PCI Controllers
- 166 MHz, 32-bit, 3.3V I/O, Local Bus with Memory Controller
- Integrated Four-channel DMA Controller
- Dual I2C and Dual Universal Asynchronous Receiver/Transmitter (DUAR) Support
- Programmable Interrupt Controller (PIC), IEEE 1149.1 JTAG Test Access Port
- 1.1V Core Voltage with 3.3V and 2.5V I/O, 783-pin HITCE Package

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0831C–HIREL–04/08

Description

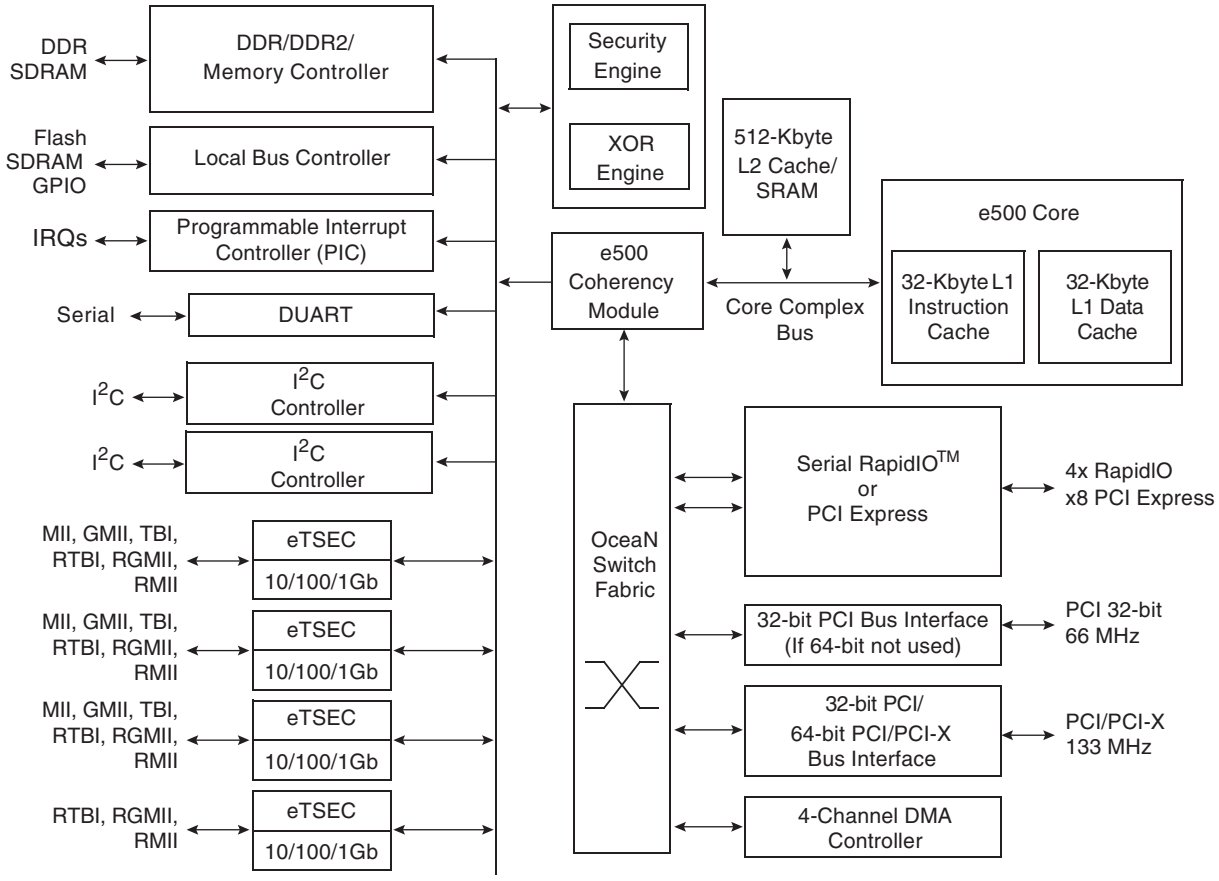
The PC8548E contains a PowerPC® processor core. The PC8548E integrates a processor that implements the PowerPC architecture with system logic required for networking, storage, and general-purpose embedded applications. For functional characteristics of the processor, refer to the PC8548E Integrated Processor Preliminary Reference Manual.

Screening

- **Full Military Temperature Range (T_C = -55°C, T_J = +125°C)**
- **Industrial Temperature Range (T_C = -40°C, T_J = +110°C)**

1. PC8548E Architecture General Overview

Figure 1-1. PC8548E Block Diagram



2. Features Overview

The following list provides an overview of the PC8548E feature set:

- High-performance 32-bit Book E–enhanced core that implements the PowerPC® architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
  - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - 36-bit real addressing
  - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
  - Enhanced hardware and software debug support
  - Performance monitor facility that is similar to, but separate from, the PC8548E performance monitor

  The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.
- 512-Kbyte L2 cache/SRAM
  - Flexible configuration.
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
  - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
  - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express

  - Four inbound windows plus a default window on RapidIO
  - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
  - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface
  - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Full ECC support
  - Page mode support
    - Up to 16 simultaneous open pages for DDR
    - Up to 32 simultaneous open pages for DDR2
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support when using DDR2
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5V SSTL_2 compatible I/O (1.8V SSTL_1.8 for DDR2)
  - Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller

  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- PKEU: public key execution unit
  - RSA and Diffie-Hellman; programmable field size up to 2048 bits
  - Elliptic curve cryptography with F_2m and F(p) modes and programmable field size up to 511 bits
- DEU: Data Encryption Standard execution unit
  - DES, 3DES
  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU: Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU: ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU: message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU: Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG: random number generator
- XOR engine for parity checking in RAID storage applications

• Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
• Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
• DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{RTS}$, $\overline{CTS}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
• Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz

  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMI
  - Flexible configuration for multiple PHY interface configurations.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - EEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses

  - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

• OCeaN switch fabric
- Full crossbar packet switch
- Reorders packets from a source based on priorities
- Reorders packets to bypass blocked packets
- Implements starvation avoidance algorithms
- Supports packets with payloads of up to 256 bytes

• Integrated DMA controller
- Four-channel controller
- All channels accessible by both the local and remote masters
- Extended DMA functions (advanced chaining and striding capability)
- Support for scatter and gather transfers
- Misaligned transfer capability
- Interrupt on completed segment, link, list, and error
- Supports transfers to or from any local memory or I/O port
- Selectable hardware-enforced coherency (snoop/no snoop)
- Ability to start and flow control each DMA channel from external 3-pin interface
- Ability to launch DMA from single write transaction

• Two PCI/PCI-X controllers
- PCI 2.2 and PCI-X 1.0 compatible
- One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
- One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
- Host and agent mode support
- 64-bit dual address cycle (DAC) support
- PCI-X supports multiple split transactions
- Supports PCI-to-memory and memory-to-PCI streaming
- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes

  - PCI 3.3V compatible
  - Selectable hardware-enforced coherency
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification, Revision 1.2*
  - Both 1x and 4x LP-serial link interfaces
  - Long- and short-haul electricals with selectable pre-compensation
  - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
  - Auto detection of 1x- and 4x-mode operation during port initialization
  - Link initialization and synchronization
  - Large and small size transport information field support selectable at initialization time
  - 34-bit addressing
  - Up to 256 bytes data payload
  - All transaction flows and priorities
  - Atomic set/clr/inc/dec for read-modify-write operations
  - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
  - Receiver-controlled flow control
  - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
  - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
  - Hardware recovery only
  - Register support is not required for software-mediated error recovery.
  - Accept-all mode of operation for fail-over support
  - Support for RapidIO error injection
  - Internal LP-serial and application interface-level loopback modes
  - Memory and PHY BIST for at-speed production test
- RapidIO–compliant message unit
  - 4 Kbytes of payload per message
  - Up to sixteen 256-byte segments per message
  - Two inbound data message structures within the inbox
  - Capable of receiving three letters at any mailbox
  - Two outbound data message structures within the outbox
  - Capable of sending three letters simultaneously
  - Single segment multicast to up to 32 devIDs
  - Chaining and direct modes in the outbox
  - Single inbound doorbell message structure
  - Facility to accept port-write messages
- PCI Express interface
  - PCI Express 1.0a compatible

  - Supports x8, x4, x2, and x1 link widths
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high speed I/O interfaces supports one of the following configurations:
  - x8 PCI Express
  - x4 PCI Express and 4x serial RapidIO
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the eight counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1 compliant, JTAG boundary scan
- 783 HITCE package

3. Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PC8548E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

3.2 Detailed Specification

This specification describes the specific requirements for the microprocessor PC8548E in compliance with e2v standard screening.

3.3 Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

3.3.1 Absolute Maximum Ratings

Table 3-1 provides the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings(1)

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.21	V	
PLL supply voltage		AV_{DD}	-0.3 to 1.21	V	
Core power supply for SerDes transceivers		SV_{DD}	-0.3 to 1.21	V	
Pad power supply for SerDes transceivers		XV_{DD}	-0.3 to 1.21	V	
DDR and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD} (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	
		TV_{DD} (for eTSEC3 and eTSEC4)	-0.3 to 3.63 -0.3 to 2.75		
PCI/PCI-X, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.63	V	(3)
Local bus I/O voltage		BV_{DD}	-0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98	V	(3)
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	-0.3 to (GV_{DD} + 0.3)	V	(2)(5)
	DDR/DDR2 DRAM reference	MV_{REF}	-0.3 to (GV_{DD}/2 + 0.3)	V	(2)(5)
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	-0.3 to (LV_{DD} + 0.3) -0.3 to (TV_{DD} + 0.3)	V	(4)(5)
	Local bus signals	BV_{IN}	-0.3 to (BV_{DD} + 0.3)		
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	-0.3 to (OV_{DD} + 0.3)	V	(5)
	PCI/PCI-X	OV_{IN}	-0.3 to (OV_{DD} + 0.3)	V	(6)
Storage temperature range		T_{STG}	-55 to 150	°C	

Notes: 1. Functional and tested operating conditions are given in Table 3-2 on page 11. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3-1 on page 12.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3V operation, as shown in Figure 7-1 on page 22.

3.3.2 Recommended Operating Conditions

Table 3-2 provides the recommended operating conditions for this device. Note that the values in Table 3-2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3-2. Recommended Operating Conditions

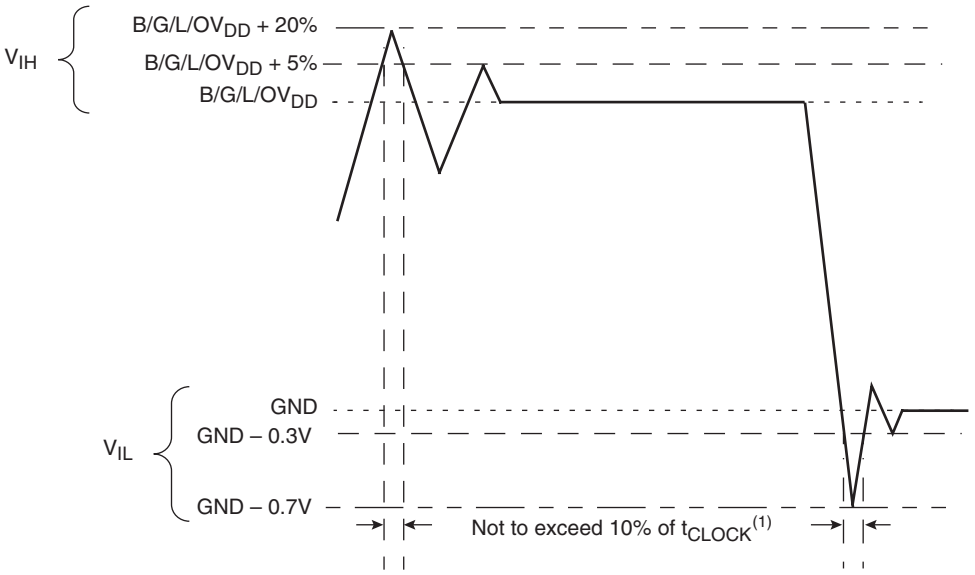
Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.1V ± 55 mV	V	
PLL supply voltage		AV_{DD}	1.1V ± 55 mV	V	(1)
Core power supply for SerDes transceivers		SV_{DD}	1.1V ± 55 mV	V	
Pad power supply for SerDes transceivers		XV_{DD}	1.1V ± 55 mV	V	
DDR and DDR2 DRAM I/O voltage		GV_{DD}	2.5V ± 125 mV 1.8V ± 90 mV	V	
Three-speed Ethernet I/O voltage		LV_{DD}	3.3V ± 165 mV 2.5V ± 125 mV	V	(4)
		TV_{DD}	3.3V ± 165 mV 2.5V ± 125 mV		(4)
PCI/PCI-X, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3V ± 165 mV	V	(3)
Local bus I/O voltage		BV_{DD}	3.3V ± 165 mV 2.5V ± 125 mV	V	
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	(2)
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	(2)
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	(4)
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	(3)
Operating Temperature range		T_C,T_J	T_C = -55°C to T_J = 125°C	°C	

Notes:
1. This voltage is the input to the filter discussed in Section 22.2.1 "PLL Power Supply Filtering" on page 89 and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 3-1 shows the undershoot and overshoot voltages at the interfaces of the PC8548E.

Figure 3-1. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}$



Note: 1. t_{CLOCK} refers to the clock period associated with the respective interface:
For I^2C and JTAG, t_{CLOCK} references SYSCLK.
For DDR, t_{CLOCK} references MCLK.
For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
For LBIU, t_{CLOCK} references LCLK.
For PCI, t_{CLOCK} references PCI*n*_CLK or SYSCLK.
For SerDes, t_{CLOCK} references SD_REF_CLK.

2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

The core voltage must always be provided at nominal 1.1V. (See Table 3-2 on page 11 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3-2 on page 11. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

3.3.3 Output Driver Characteristics

Table 3-3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3-3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV_{DD} = 3.3V BV_{DD} = 2.5V	(1)
	45 (default) 45 (default)	BV_{DD} = 3.3V BV_{DD} = 2.5V	
PCI signals	25	OV_{DD} = 3.3V	(2)
	45 (default)		
DDR signal	18 36 (half strength mode)	GV_{DD} = 2.5V	(3)
DDR2 signal	18 36 (half strength mode)	GV_{DD} = 1.8V	(3)
TSEC/10/100 signals	45	L/TV_{DD} = 2.5/3.3V	
DUART, system control, JTAG	45	OV_{DD} = 3.3V	
I^2C	150	OV_{DD} = 3.3V	

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT1}}$ signal at reset.
3. The drive strength of the DDR interface in half-strength mode is at T_C = 105°C and at GV_{DD} (min).

3.4 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

1. V_{DD}, AV_{DD_n}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Notes:
1. Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.
2. In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

4. Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4-1.

Table 4-1. PC8548E Power Dissipation[1]

CCB Frequency[1]	Core Frequency	SLEEP[2]	Typical-65[3]	Typical-105[4]	Maximum[5]	Unit
400	800	2.7	4.6	7.5	11	W
	1000	2.7	5.0	7.9	11.6	
	1200	2.7	5.4	8.3	11.9	
533	1333	6.2	7.9	10.8	12.8	W

Notes:
1. CCB Frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on V_{DD} = 1.1 V, T_J = 65°C.
3. Typical-65 is based on V_{DD} = 1.1 V, T_J = 65°C, running Dhrystone.
4. Typical-105 is based on V_{DD} = 1.1 V, T_J = 105°C, running Dhrystone.
5. Maximum is based on V_{DD} = 1.1 V, T_J = 125°C, running a smoke test.

At allowable voltage levels, the estimated power dissipation on the 1.1V AV_{DD} supplies for the PC8548E PLLs is shown in Table 4-2.

Because I/O usage varies from design to design, for power dissipation estimates on the G/L/OV_{DD} power rails, refer to the PowerQUICC III I/O power calculator.

Table 4-2. PC8548E Estimated I/O Power Dissipation

Interface	Parameters	1.1V (XV_{DD})	1.8V (GV_{DD})	2.5V ($B/G/L/TV_{DD}$)	3.3V ($B/L/O/TV_{DD}$)	Comments
DDR	266 MHz data		0.31 W	0.59 W		
	333 MHz data		0.38 W	0.73 W		
	400 MHz data		0.46 W			
	533 MHz data		0.60 W			
PCI-Express	x8, 2.5 G-baud	0.71 W				
Serial RapidIO	x4, 3.125 G-baud	0.49 W				
PCI-X	64-bit, 133 MHz				0.25 W	
PCI	64-bit, 66 MHz				0.14 W	
	64-bit, 33 MHz				0.08 W	
	32-bit, 66 MHz				0.07 W	Power per PCI port
	32-bit, 33 MHz				0.04 W	
Local Bus	32-bit, 133 MHz			0.14 W	0.24 W	
	32-bit, 66MHz			0.07 W	0.13 W	
	32-bit, 33 MHz			0.04 W	0.07 W	

Table 4-2. PC8548E Estimated I/O Power Dissipation (Continued)

Interface	Parameters	1.1V (XV_{DD})	1.8V (GV_{DD})	2.5V ($B/G/L/TV_{DD}$)	3.3V ($B/L/O/TV_{DD}$)	Comments
eTSEC (10/100/1000 Ethernet)	MII				0.01 W	Power per eTSEC used
	GMII				0.07 W	
	TBI				0.07 W	
	RGMII			0.04 W		
	RTBI			0.04 W		
eTSEC (packet FIFO)	16-bit, 200 MHz			0.20 W		Power per FIFO interface used
	16-bit, 155 MHz			0.16 W		
	8-bit, 200 MHz			0.11 W		
	8-bit, 155 MHz			0.08 W		

5. Input Clocks

5.1 System Clock Timing

Table 5-1 provides the system clock (SYSCLK) AC timing specifications for the PC8548E.

Table 5-1. SYSCLK AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} = 3.3V ± 165 mV (see Table 3-2 on page 11)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	16	–	133	MHz	(1)(6)
SYSCLK cycle time	t_{SYSCLK}	7.5	–	60	ns	(6)
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	(2)
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	–	60	%	(3)
SYSCLK jitter	–	–	–	± 150	ps	(4)(5)

Notes:
1. Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum operating frequencies. Refer to Section 20.2 ”CCB/SYSCLK PLL Ratio” on page 85” and Section 20.3 ”e500 Core PLL Ratio” on page 86, for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6V and 2.7V
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter – short term and long term – and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. This parameter has been adjusted slower according to the workaround for device erratum GEN-13.

5.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

5.3 eTSEC Gigabit Reference Clock Timing

Table 5-2 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the PC8548E.

Table 5-2. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	–	125	–	MHz	
EC_GTX_CLK125 cycle time	t_{G125}	–	8	–	ns	
EC_GTX_CLK125 rise and fall time - L/TV_{DD} = 2.5V - L/TV_{DD} = 3.3V	t_{G125R}/t_{G125F}		–	0.75 1.0	ns	(1)
EC_GTX_CLK125 duty cycle - GMII, TBI - 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	45 47	–	55 53	%	(2)(3)

Note: 1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for L/TV_{DD} = 2.5V, and from 0.6 and 2.7V for L/TV_{DD} = 3.3V.

2. Timing is guaranteed by design and characterization.

3. EC_GTX_CLK125 is used to generate the GTX clock TSEC*n*_GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSECn_ GTX_CLK. See Section 9.2.6 "RGMII and RTBI AC Timing Specifications" on page 33 for duty cycle for 10Base-T and 100Base-T reference clock.

5.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCI*n*_CLK. Table 5-3 provides the PCI/PCI-X reference clock AC timing specifications for the PC8548E.

Table 5-3. PCI*n*_CLK AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} = 3.3V ± 165 mV (see Table 3-2 on page 11)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI*n*_CLK frequency	f_{PCICLK}	16	–	133	MHz	
PCI*n*_CLK cycle time	t_{PCICLK}	7.5	–	60	ns	
PCI*n*_CLK rise and fall time	t_{PCIKH}, t_{PCIKL}	0.6	1.0	2.1	ns	(1)(2)
PCI*n*_CLK duty cycle	$t_{PCIKHKL}/t_{PCICLK}$	40	–	60	%	(2)

Notes: 1. Rise and fall times for SYSCLK are measured at 0.6V and 2.7V.

2. Timing is guaranteed by design and characterization.

5.5 Platform to FIFO restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:
FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz

For FIFO encoded mode:
FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz.

5.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{500\ \text{MHz} \times (\text{PCI-Express link width})}{8}$$

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

5.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

6. RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the PC8548E. Table 6-1 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 6-1. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	–	µs	
Minimum assertion time for $\overline{\text{SRESET}}$	3	–	SYSCLKs	(1)
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	–	µs	
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	–	SYSCLKs	(1)
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	–	SYSCLKs	(1)
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	–	5	SYSCLKs	(1)

Note: 1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the PC8548E.

Table 6-2 provides the PLL lock times.

Table 6-2. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	–	100	µs
Local bus PLL lock time	–	50	µs
PCI/PCI-X bus PLL lock time	–	50	µs

7. DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the PC8548E. Note that GV_{DD}(typ) = 2.5V for DDR SDRAM, and GV_{DD}(typ) = 1.8V for DDR2 SDRAM.

7.1 DDR SDRAM DC Electrical Characteristics

Table 7-1 provides the recommended operating conditions for the DDR2 SDRAM controller of the PC8548E when GV_{DD}(typ) = 1.8V.

Table 7-1. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	(1)
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	(2)
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	(3)
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	MV_{REF} - 0.125	V	
Output leakage current	I_{OZ}	-50	50	µA	(4)
Output high current (V_{OUT} = 1.420V)	I_{OH}	-13.4	–	mA	
Output low current (V_{OUT} = 0.280V)	I_{OL}	13.4	–	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0V ≤ V_{OUT} ≤ GV_{DD}.

Table 7-2 provides the DDR capacitance when GV_{DD}(typ) = 1.8V.

Table 7-2. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	(1)
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	–	0.5	pF	(1)

Note: 1. This parameter is sampled. GV_{DD} = 1.8V ± 0.090V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2V.

Table 7-3 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5V.

Table 7-3. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	(1)
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	(2)
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	(3)
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	MV_{REF} – 0.15	V	
Output leakage current	I_{OZ}	-50	50	µA	(4)
Output high current (V_{OUT} = 1.95V)	I_{OH}	-16.2	–	mA	
Output low current (V_{OUT} = 0.35V)	I_{OL}	16.2	–	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0V ≤ V_{OUT} ≤ GV_{DD}.

Table 7-4 provides the DDR capacitance when GV_{DD} (typ) = 2.5V.

Table 7-4. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	(1)
Delta input/output capacitance: DQ, DQS	C_{DIO}	–	0.5	pF	(1)

Notes:
1. This parameter is sampled. GV_{DD} = 2.5V ± 0.125V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2V.

Table 7-5 provides the current draw characteristics for MV_{REF}.

Table 7-5. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	–	500	µA	(1)

Notes:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 µA current.

7.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

7.2.1 DDR SDRAM Input AC Timing Specifications

Table 7-6 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 1.8V.

Table 7-6. DDR2 SDRAM Input AC Timing Specifications for 1.8V Interface (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	–	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25		V

Table 7-7 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5V.

Table 7-7. DDR SDRAM Input AC Timing Specifications for 2.5V Interface (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	–	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31		V

Table 7-8 provides the input AC timing specifications for the DDR SDRAM interface.

Table 7-8. DDR SDRAM Input AC Timing Specifications (At Recommended Operating Conditions)

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS–MDQ/MECC/MDM	t_{CISKEW}			ps	(1)(2)
533 MHz		-300	300		
400 MHz		-365	365		
333 MHz		-390	390		

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

7.2.2 DDR SDRAM Output AC Timing Specifications

Table 7-9. DDR SDRAM Output AC Timing Specifications (At Recommended Operating Conditions)

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, $\overline{\text{MCK}}$[n]/MCK[n] crossing	t_{MCK}	3.75	10	ns	(2)
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	 1.48 1.95 2.40	 – – –	ns	(3)
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	 1.48 1.95 2.40	 – – –	ns	(3)
$\overline{\text{MCS}}$[n] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	 1.48 1.95 2.40	 – – –	ns	(3)
$\overline{\text{MCS}}$[n] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCX}	 1.48 1.95 2.40	 – – –	ns	(3)
MCK to MDQS Skew	t_{DDKHMH}	-0.6	0.6	ns	(4)
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDS}, t_{DDKLDS}	 538 700 900	 – – –	ps	(5)
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDX}, t_{DDKLDX}	 538 700 900	 – – –	ps	(5)
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	(6)
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	(6)

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note (1). For example, tDDKHMH describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the PC8548E PowerQUICC III Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.

5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note [(1)].

Note: For the ADDR/CMD setup and hold specifications in Table 7-9 on page 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 7-1 on page 22 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

Figure 7-1. Timing Diagram for t_{DDKHMH}

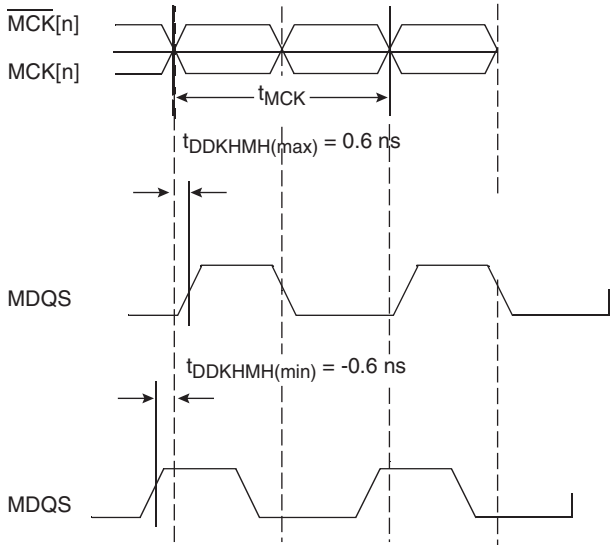


Figure 7-2 shows the DDR SDRAM output timing diagram.

Figure 7-2. DDR SDRAM Output Timing Diagram

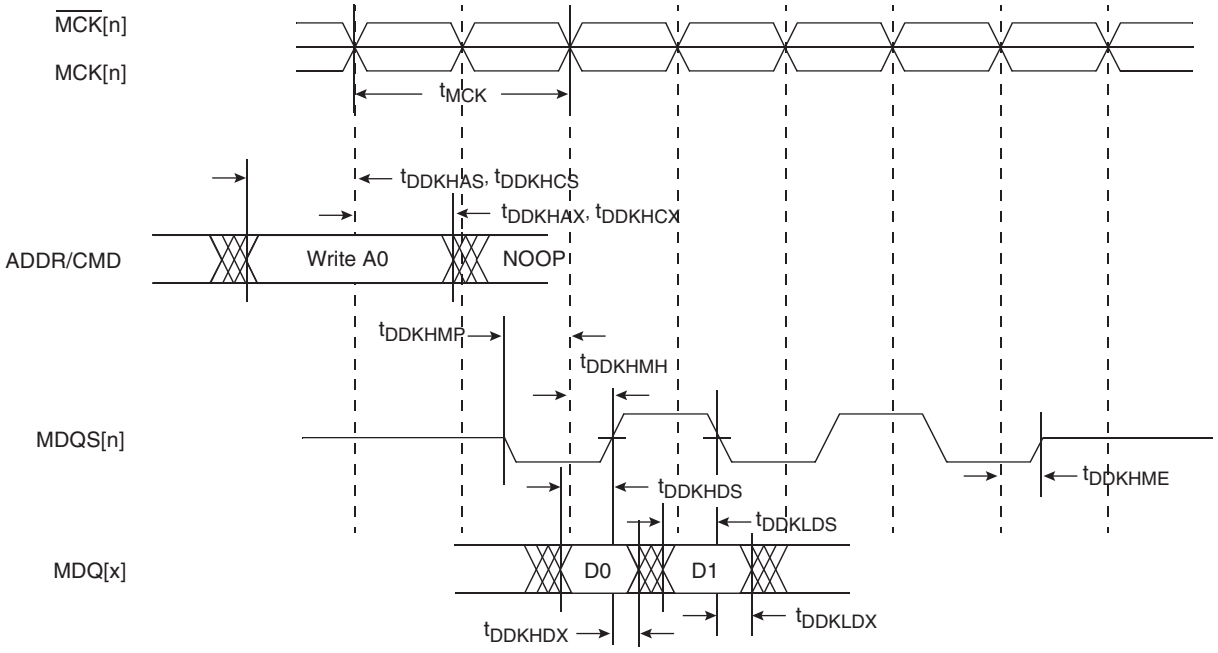
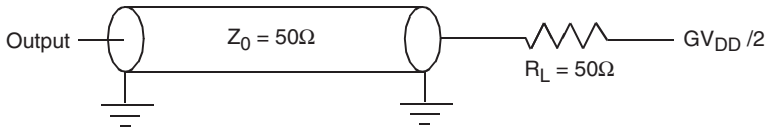


Figure 7-3 provides the AC test load for the DDR bus.

Figure 7-3. DDR AC Test Load



8. DUART

This section describes the DC and AC electrical specifications for the DUART interface of the PC8548E.

8.1 DUART DC Electrical Characteristics

Table 8-1 provides the DC electrical characteristics for the DUART interface.

Table 8-1. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN} [(1)] = 0V or V_{IN} = V_{DD})	I_{IN}	–	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = -100 μA)	V_{OH}	OV_{DD}– 0.2	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	–	0.2	V

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

8.2 DUART AC Electrical Specifications

Table 8-2 provides the AC timing parameters for the DUART interface.

Table 8-2. DUART AC Timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	(1)(2)
Maximum baud rate	f_{CCB} clock/16	baud	(1)(2)(3)
Oversample rate	16	–	(1)(4)

Notes: 1. Guaranteed by design
2. f_{CCB} refers to the internal platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

9. Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

9.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps) – GMII/MII/TBI/ RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5V, while the GMII and TBI interfaces can be operated at 3.3V. The GMII, MII, or TBI interface timing is compliant with the IEEE Std. 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 10. ”Ethernet Management Interface Electrical Characteristics” on page 36.

9.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 9-1 and Table 9-2. The RGMII and RTBI signals are based on a 2.5V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 9-1. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3V	LV_{DD} TV_{DD}	3.13	3.47	V	(1)(2)
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = -4.0 mA)	V_{OH}	2.40	LV_{DD}/TV_{DD} + 0.3	V	
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	
Input high voltage	V_{IH}	2.0	LV_{DD}/TV_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	0.90	V	
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	–	40	µA	(1)(2)(3)
Input low current (V_{IN} = GND)	I_{IL}	-600	–	µA	(3)

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3-1 on page 10 and Table 3-2 on page 11

.

Table 9-2. RGMII, RTBI and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5V	LV_{DD} TV_{DD}	2.37	2.63	V	(1)(2)
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = -1.0 mA)	V_{OH}	2	LV_{DD}/TV_{DD} + 0.3	V	
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	0.90	V	
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	–	10	µA	(1)(2)(3)
Input low current (V_{IN} = GND)	I_{IL}	-15	–	µA	(3)

Notes: 1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

9.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

9.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSECn's TSECn_TX_CLK, while the receive clock must be applied to pin TSECn_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSECn_GTX_CLK pin (while transmit data appears on TSECn_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSECn_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 5.5 "Platform to FIFO restrictions" on page 17.

A summary of the FIFO AC specifications appears in Table 3-2 and Table 9-4 on page 26.

Table 9-3. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	t_{FIT}	5.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	–	–	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	–	–	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	–	–	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	–	–	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5()	–	3.0	ns

Table 9-4. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{FIR}	5.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	–	–	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	–	–	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	–	–	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	–	–	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	–	–	ns

Timing diagrams for FIFO appear in Figure 9-1 and Figure 9-2 on page 27.

Figure 9-1. FIFO Transmit AC Timing Diagram

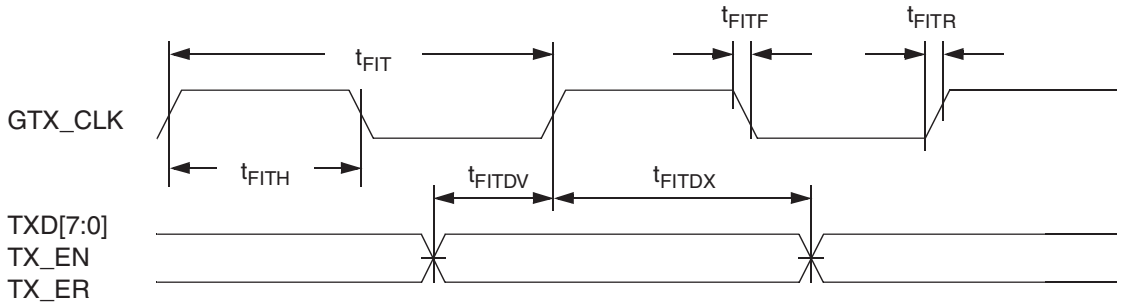
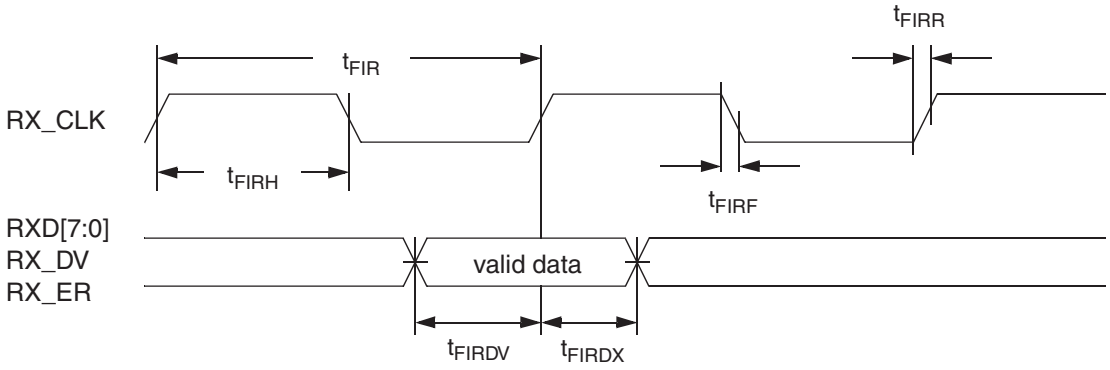


Figure 9-2. FIFO Receive AC Timing Diagram



9.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

9.2.2.1 GMII Transmit AC Timing Specifications

Table 9-5 provides the GMII transmit AC timing specifications.

Table 9-5. GMII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

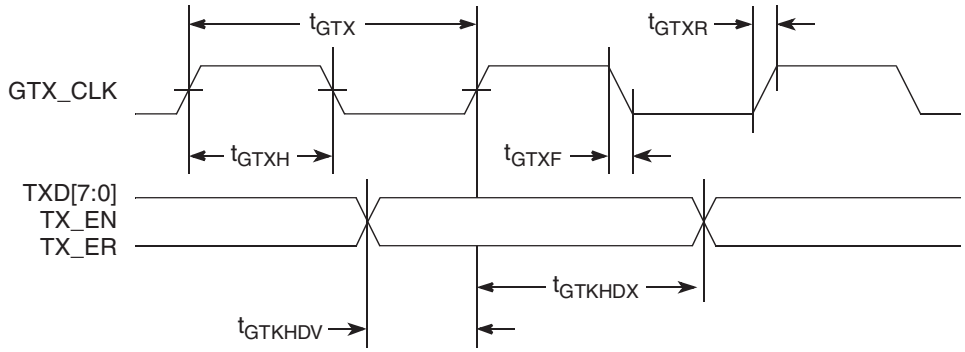
Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	–	–	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	–	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}[2]	–	–	1.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	–	–	1.0	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 9-3 shows the GMII transmit AC timing diagram.

Figure 9-3. GMII Transmit AC Timing Diagram



9.2.2.2 GMII Receive AC Timing Specifications

Table 9-6 provides the GMII receive AC timing specifications..

Table 9-6. GMII Receive AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	–	8.0	–	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	–	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	–	–	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	–	–	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}[2]	–	–	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]			1.0	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the tRX clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9-4 provides the AC test load for eTSEC.

Figure 9-4. eTSEC AC Test Load

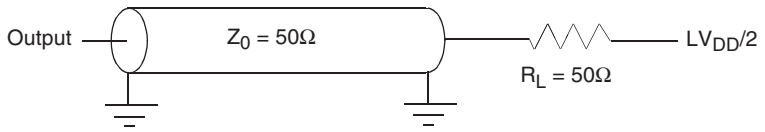
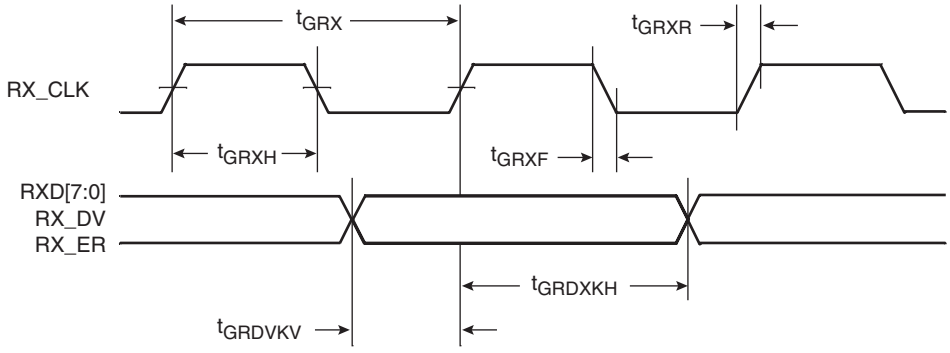


Figure 9-5 shows the GMII receive AC timing diagram.

Figure 9-5. GMII Receive AC Timing Diagram



9.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

9.2.3.1 MII Receive AC Timing Specifications

Table 9-7 provides the MII transmit AC timing specifications.

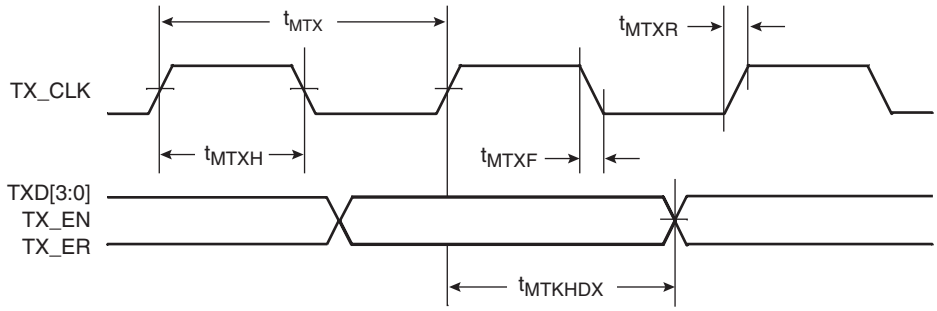
Table 9-7. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	–	400	–	ns
TX_CLK clock period 100 Mbps	t_{MTX}	–	40	–	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	–	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1.0	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	–	4	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	–	4	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9-6 shows the MII transmit AC timing diagram.

Figure 9-6. MII Transmit AC Timing Diagram



9.2.3.2 MII Receive AC Timing Specifications

Table 9-8 provides the MII receive AC timing specifications.

Table 9-8. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	–	400	–	ns
RX_CLK clock period 100 Mbps	t_{MRX}	–	40	–	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	–	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10	–	–	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10	–	–	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	–	4	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	–	4	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional.
For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with
2. Guaranteed by design.

Figure 9-7 provides the AC test load for eTSEC.

Figure 9-7. eTSEC AC Test Load

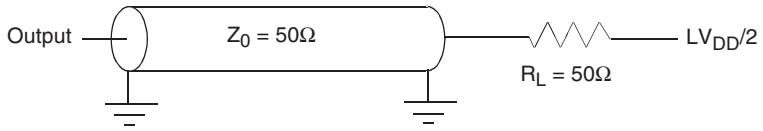
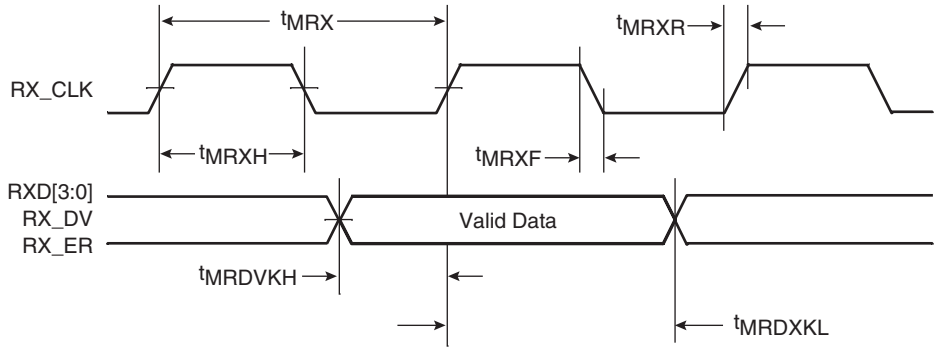


Figure 9-8 shows the MII receive AC timing diagram.

Figure 9-8. MII Receive AC Timing Diagram



9.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

9.2.4.1 TBI Transmit AC Timing Specifications

Table 9-9 provides the TBI transmit AC timing specifications.

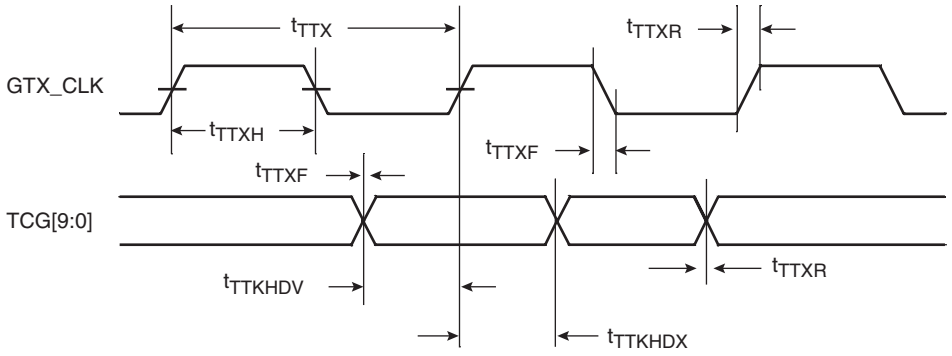
Table 9-9. TBI Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	–	–	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	–	–	ns
GTX_CLK rise (20%–80%)	t_{TTXR}[2]	–	–	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	–	–	1.0	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 9-9 shows the TBI transmit AC timing diagram.

Figure 9-9. TBI Transmit AC Timing Diagram



9.2.4.2 TBI Receive AC Timing Specifications

Table 9-10 provides the TBI receive AC timing specifications.

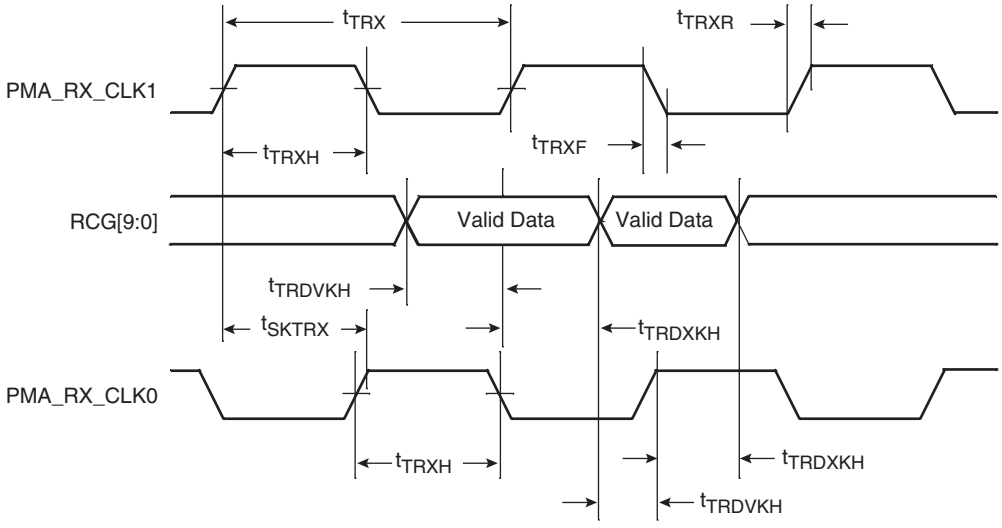
Table 9-10. TBI Receive AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}	–	16.0	–	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	–	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	–	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	–	–	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	–	–	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	–	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	–	2.4	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.

Figure 9-10 shows the TBI receive AC timing diagram.

Figure 9-10. TBI Receive AC Timing Diagram



9.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when a 125-MHz TBI receive clock is supplied on TSECn pin (no receive clock is used on in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the in all TBI modes.

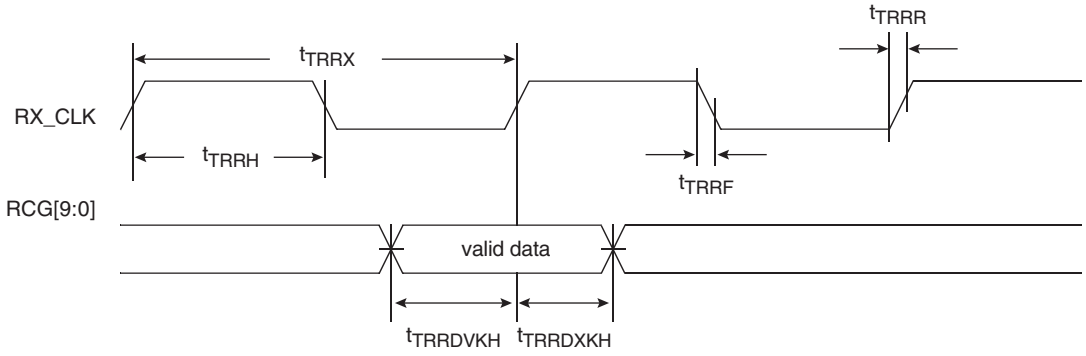
A summary of the single-clock TBI mode AC specifications for receive appears in Table 9-11.

Table 9-11. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	$t_{TRRH/TRRX}$	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	–	–	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	–	–	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	–	–	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	–	–	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	–	–	ns

A timing diagram for TBI receive appears in Figure 9-11 on page 33.

Figure 9-11. TBI Single-Clock Mode Receive AC Timing Diagram



9.2.6 RGMII and RTBI AC Timing Specifications

Table 9-12 presents the RGMII and RTBI AC timing specifications.

Table 9-12. RGMII and RTBI AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 2.5V ± 5%)

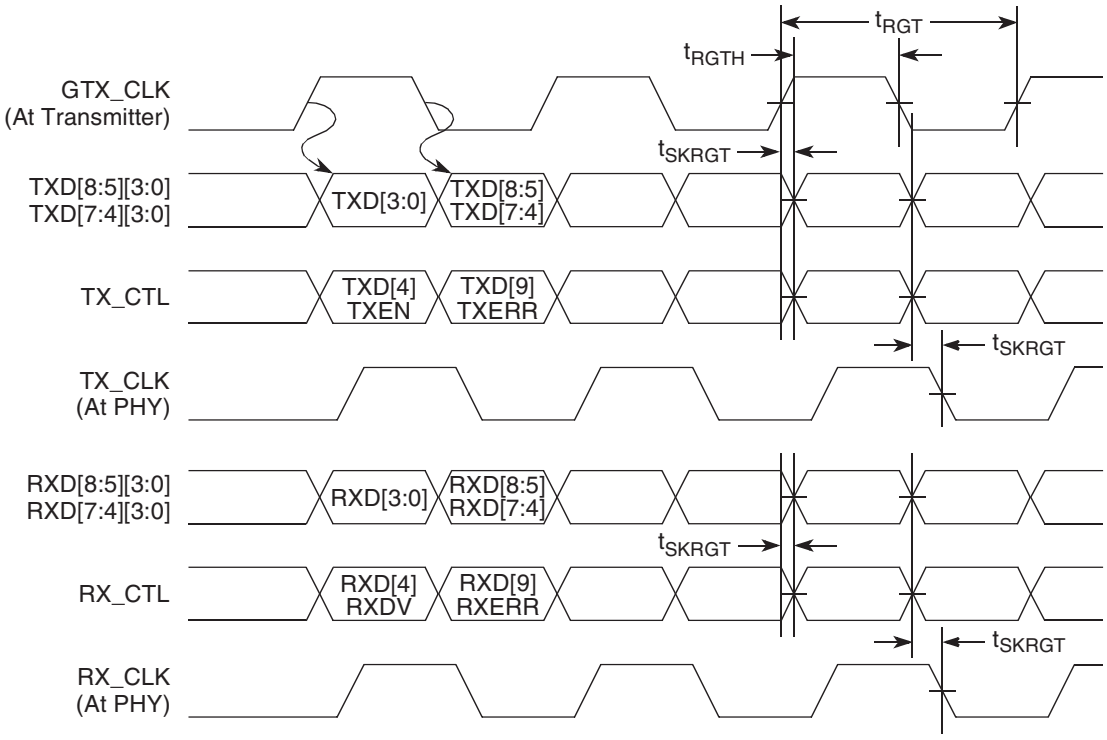
Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	-500[6]	0	500[6]	ps
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	–	2.8	ns
Clock period[3]	t_{RGT}[5]	7.2	8	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX[3][4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%-80%)	t_{RGTR}[5]	–	–	0.75	ns
Fall time (20%-80%)	t_{RGTF}[5]	–	–	0.75	ns

Notes:
1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. In rev 1.0 silicon, due to errata, t_{SKRGT} is -650 ps (Min) and 650 ps (Max). Please refer to “eTSEC 10” in the device errata document.

Figure 9-12 on page 34 shows the RGMII and RTBI AC timing and multiplexing diagrams.

Figure 9-12. RGMII and RTBI AC Timing and Multiplexing Diagrams



9.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 9-13.

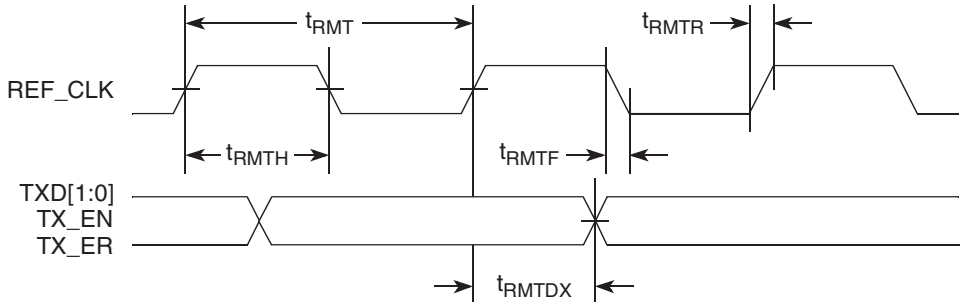
Table 9-13. RMII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	–	–	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	–	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	–	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	–	10	ns

Note: 1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9-13 shows the RMII transmit AC timing diagram.

Figure 9-13. RMII Transmit AC Timing Diagram



9.2.7.2 RMII Receive AC Timing Specifications

Table 9-14. RMII Receive AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	–	–	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	–	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	–	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	–	–	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	–	–	ns

Note: 1. The symbols used for timing specificationsherein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9-14 provides the AC test load for eTSEC.

Figure 9-14. eTSEC AC Test Load

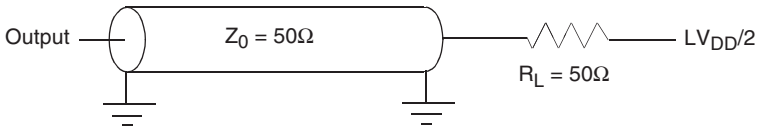
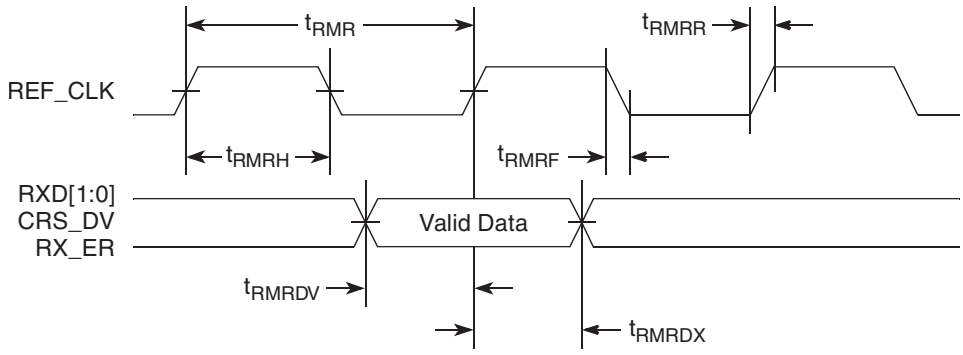


Figure 9-15 shows the RMII receive AC timing diagram.

Figure 9-15. RMII Receive AC Timing Diagram



10. Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in Section 9. "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management" on page 24.

10.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3V. The DC electrical characteristics for MDIO and MDC are provided in Table 10-1.

Table 10-1. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = -1 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	–	V
Input low voltage	V_{IL}	–	0.90	V
Input high current (OV_{DD} = Max, V_{IN}[1] = 2.1V)	I_{IH}	–	40	µA
Input low current (OV_{DD} = Max, V_{IN} = 0.5V)	I_{IL}	-600	–	µA

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

10.2 MII Management AC Electrical Specifications

Table 10-2 provides the MII management AC timing specifications.

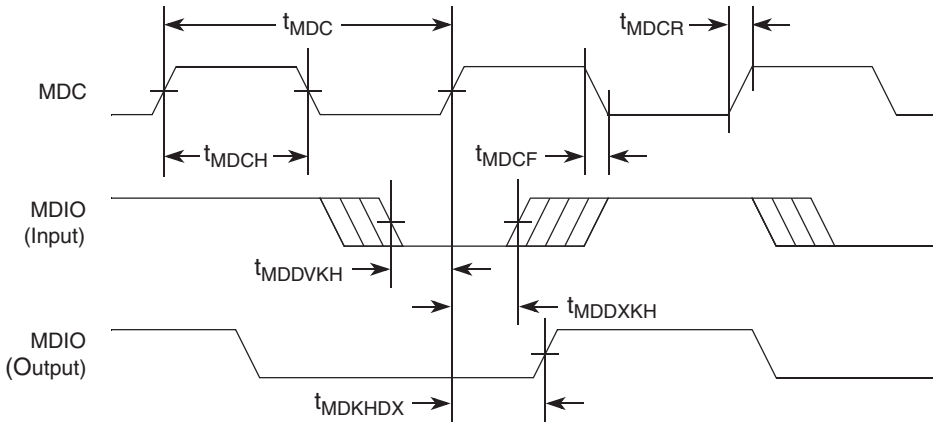
Table 10-2. MII Management AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} is 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	5.2	8.3	MHz	(2)(4)
MDC period	t_{MDC}	120	192	ns	
MDC clock pulse width high	t_{MDCH}	32	–	ns	
MDC to MDIO valid	t_{MDKHDV}	16*t_{CCB}		ns	(5)
MDC to MDIO delay	t_{MDKHDX}	10	16*t_{CCB}	ns	(3)(5)
MDIO to MDC setup time	t_{MDDVKH}	5	–	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	–	ns	
MDC rise time	t_{MDCR}	–	10	ns	(4)
MDC fall time	t_{MDHF}	–	10	ns	(4)

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. t_{plb_clk} is the platform (CCB) clock.

Figure 10-1 shows the MII management AC timing diagram.

Figure 10-1. MII Management Interface Timing Diagram



11. Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the PC8548.

11.1 Local Bus DC Electrical Characteristics

Table 11-1 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3V DC

Table 11-1. Local Bus DC Electrical Characteristics (3.3V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[(1)] = 0V or V_{IN} = BV_{DD})	I_{IN}	–	± 5	µA
High-level output voltage (BV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	BV_{DD} - 0.2	–	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.2	V

Note: 1. Note that the symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

Table 11-2 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5V DC.

Table 11-2. Local Bus DC Electrical Characteristics (2.5V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	1.70	BV_{DD}+ 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.7	V
Input current (V_{IN}[(1)] = 0V or V_{IN} = BV_{DD})	I_{IH}	–	10	µA
	I_{IL}		-15	
High-level output voltage (BV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	BV_{DD}+ 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note: 1. Note that the symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

11.2 Local Bus AC Electrical Specifications

Table 11-3 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3V DC. For information about the frequency range of local bus see Section 20.1 "Clock Ranges" on page 85.

Table 11-3. Local Bus General Timing Parameters (BV_{DD} = 3.3V DC) – PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	(2)
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$		150	ps	(7)(8)
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	–	ns	(3)(4)
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	–	ns	(3)(4)
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	–	ns	(3)(4)
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	–	ns	(3)(4)
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	–	ns	(6)
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	–	2.0	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	–	2.2	ns	(3)
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	–	2.3	ns	(3)
Local bus clock to LALE assertion	$t_{LBKHOV4}$		2.3	ns	(3)
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	–	ns	(3)
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	–	ns	(3)
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	–	2.5	ns	(5)
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	–	2.5	ns	(5)

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \cdot BV_{DD}$ of the signal in question for 3.3V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 11-4 describes the general timing parameters of the local bus interface at BV_{DD} = 2.5V DC.

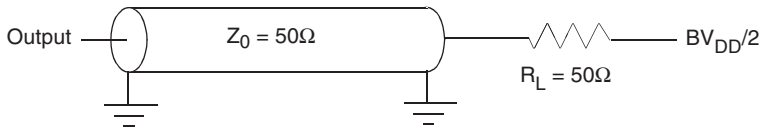
Table 11-4. Local Bus Timing Parameters (BV_{DD} = 2.5V): PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	(2)
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	–	150	ps	(7)(8)
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.9	–	ns	(3)(4)
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	–	ns	(3)(4)
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	–	ns	(3)(4)
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	–	ns	(3)(4)
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	–	ns	(6)
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	–	2.1	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	–	2.3	ns	(3)
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	–	2.4	ns	(3)
Local bus clock to LALE assertion	$t_{LBKHOV4}$	–	2.4	ns	(3)
Output hold from local bus clock (except LAD/LDP and LALE)	**$t_{LBKHOX1}$**	0.8	–	ns	(3)
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	–	ns	(3)
Local bus clock to output high Impedance (except LAD/LDP and LALE)	**$t_{LBKHOZ1}$**	–	2.6	ns	(5)
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	–	2.6	ns	(5)

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \cdot BV_{DD}$ of the signal in question for 3.3V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. Figure 9-1 on page 26 provides the AC test load for the local bus.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 11-1 provides the AC test load for the local bus.

Figure 11-1. Local Bus AC Test Load



Note: PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 Mhz, LBIU PLL is recommended to be enabled.

Figure 11-2 to Figure 11-7 on page 47 show the local bus signals.

Figure 11-2. Local Bus Signals, (PLL Enabled)

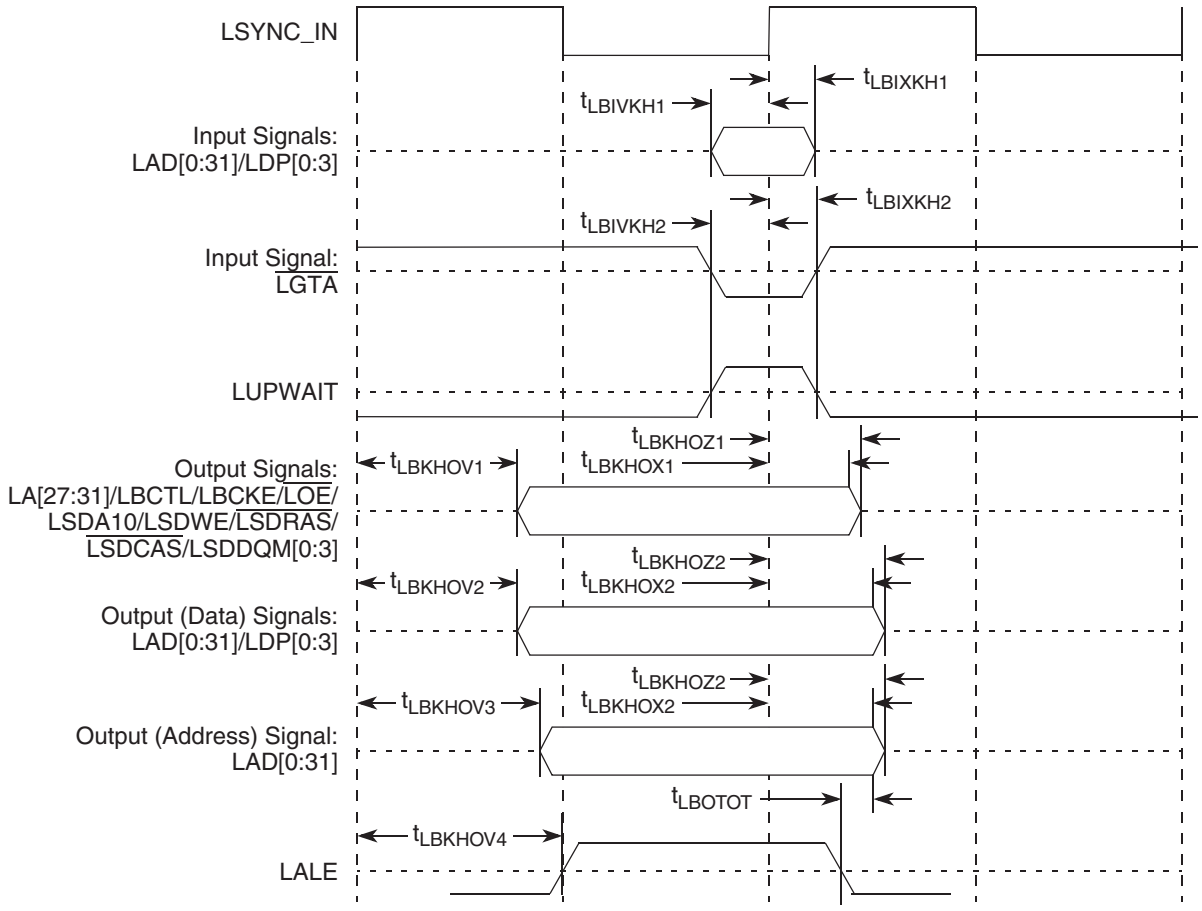


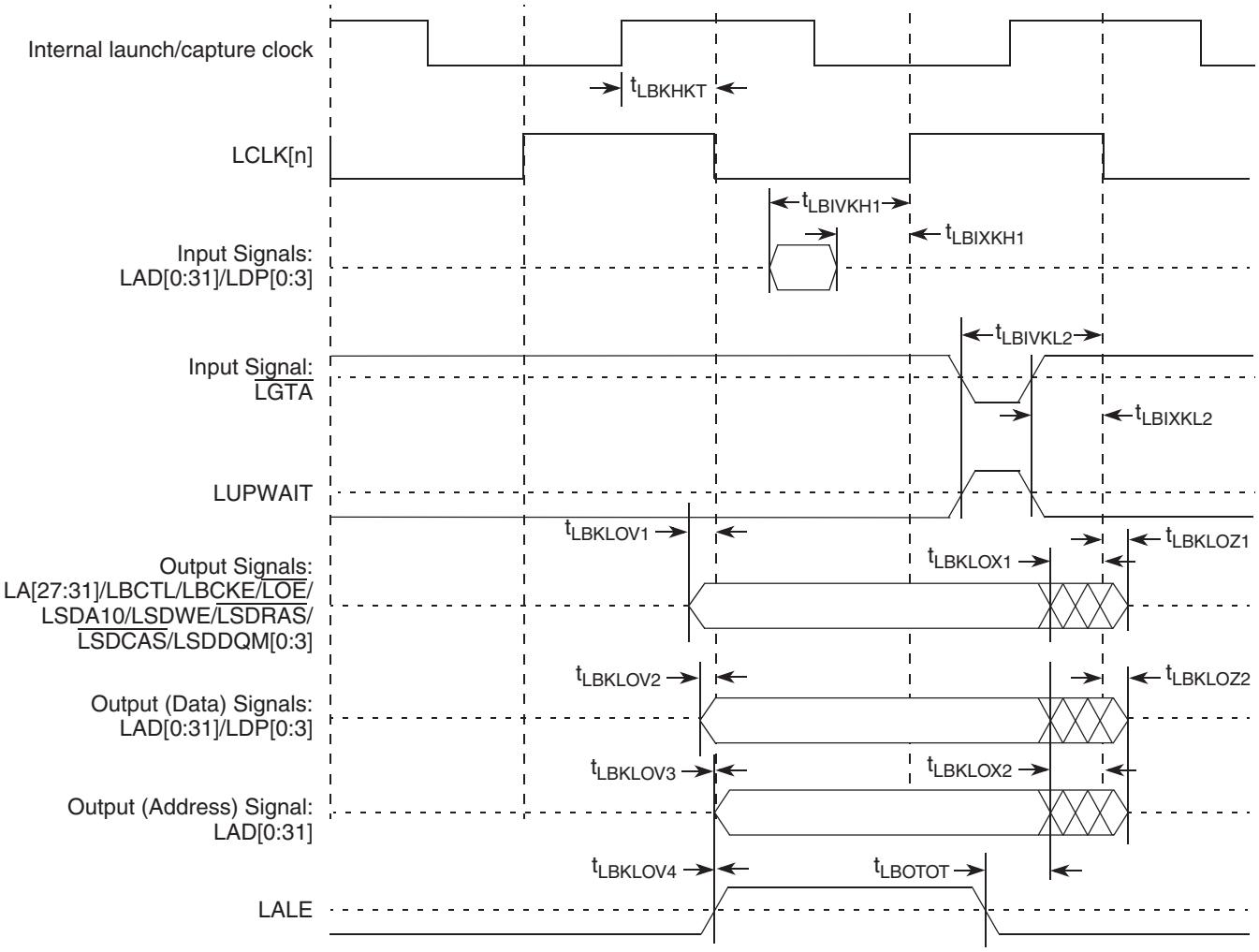
Table 11-5 describes the timing parameters of the local bus interface at BV_{DD} = 3.3V with PLL disabled.

Table 11-5. Local Bus Timing Parameters: PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	–	ns	(2)
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.4	ns	(8)
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	6.2	–	ns	(4)(5)
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.1	–	ns	(4)(5)
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	-1.8	–	ns	(4)(5)
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	-1.3	–	ns	(4)(5)
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	–	ns	(6)
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	–	-0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	–	-0.1	ns	(4)
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	–	0	ns	(4)
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-3.7	–	ns	(4)
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-3.7	–	ns	(4)
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	–	0.2	ns	(7)
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	–	0.2	ns	(7)

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which preceeds LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

Figure 11-3. Local Bus Signals (PLL Bypass Mode)



Note: In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock withe the exception of LGTA/LUPWAIT (which is captured on on the rising edge of the internal clock).

Figure 11-4. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

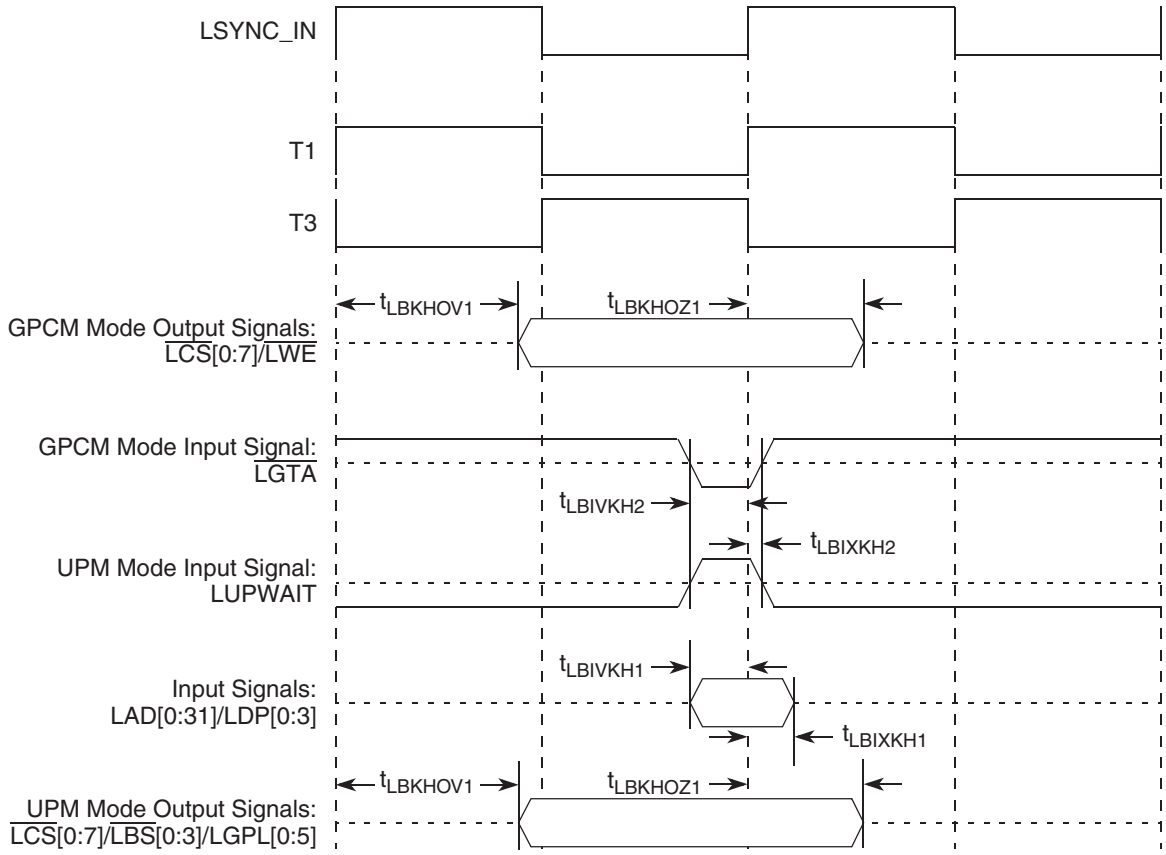


Figure 11-5. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

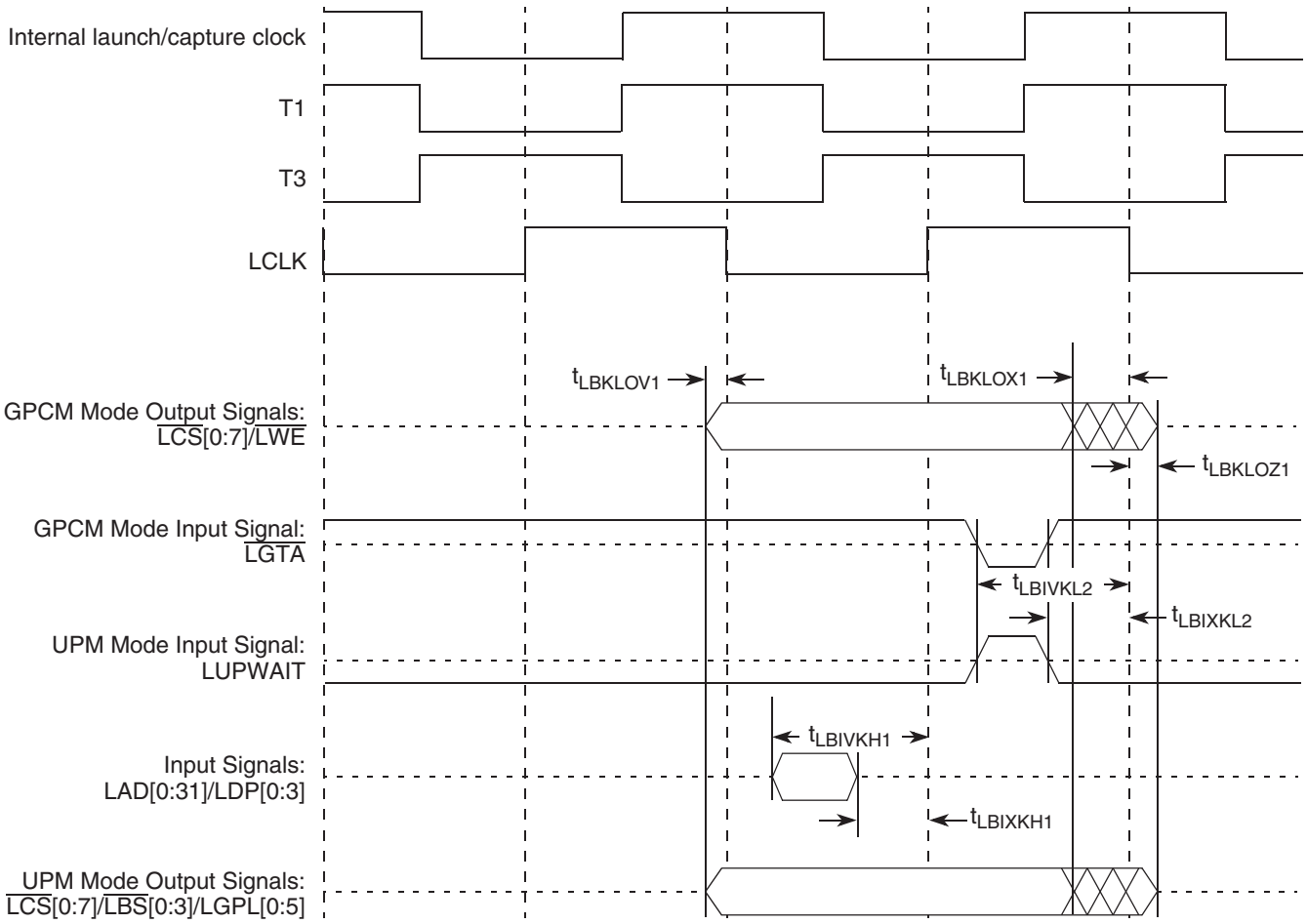


Figure 11-6. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

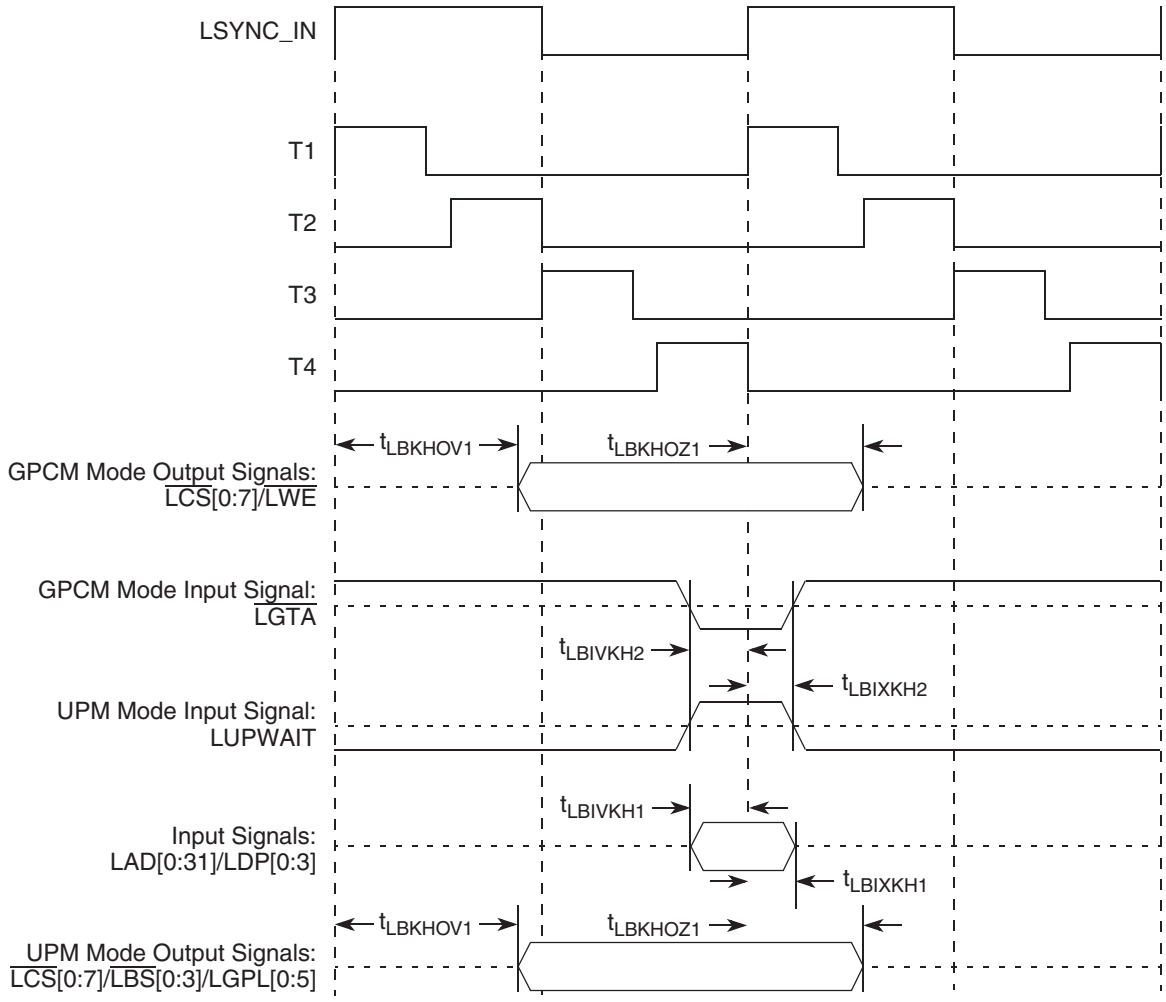
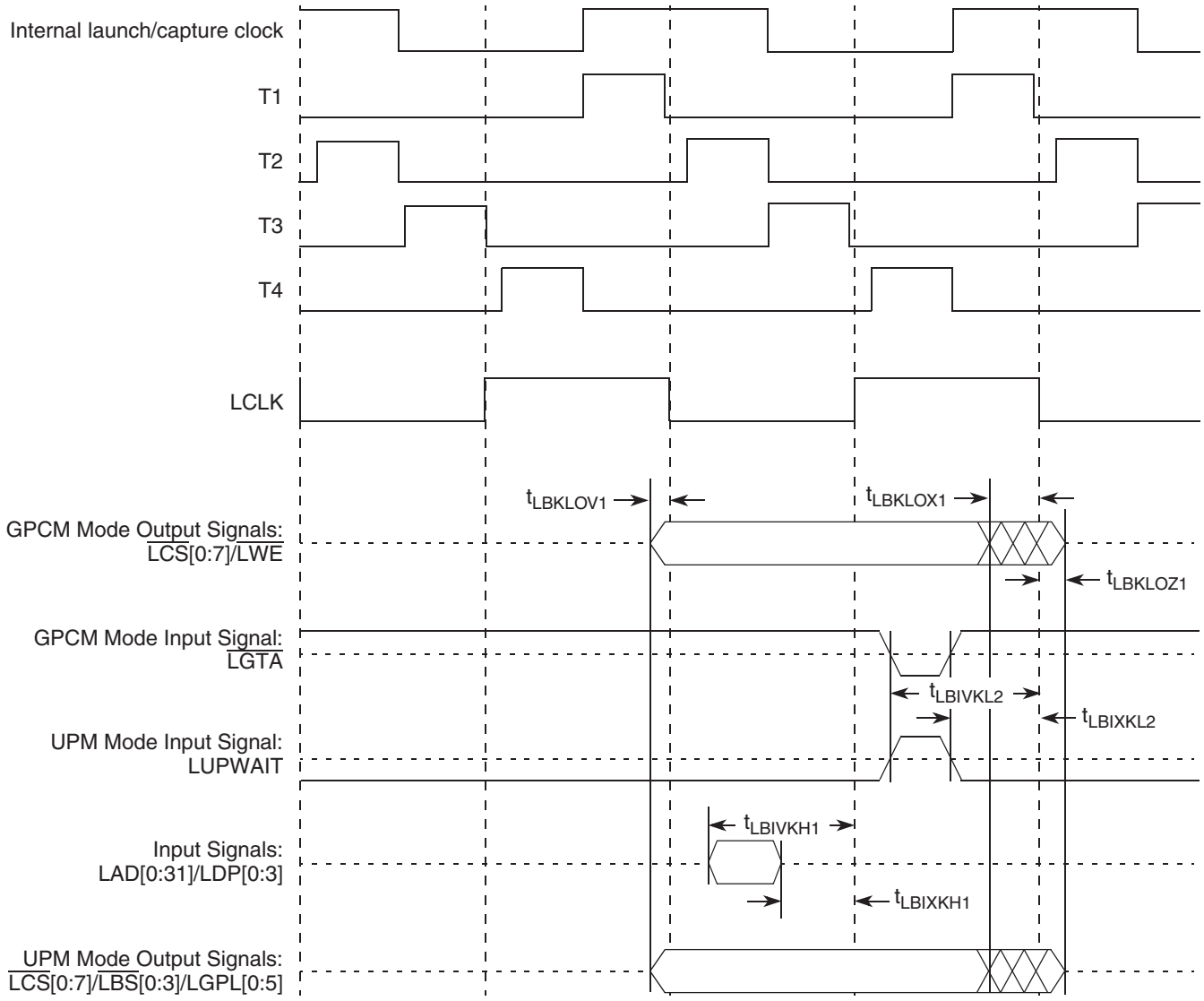


Figure 11-7. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)



12. Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at lest 3 system clocks (SYSCLK periods).

13. JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the PC8548E.

13.1 JTAG DC Electrical Characteristics

Table 13-1 provides the DC electrical characteristics for the JTAG interface.

Table 13-1. JTAG DC Electrical Characteristics

Parameter	Symbol[2]	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	–	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

13.2 JTAG AC Electrical Specifications

Table 13-2 provides the JTAG AC timing specifications as defined in Figure 13-2 through Figure 13-4 on page 50.

Table 13-2. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	–	ns	
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	–	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2.0	ns	(6)
$\overline{TRST}$ assert time	t_{TRST}	25	–	ns	(3)
Input setup times: - Boundary-scan data - TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 – –	ns	(4)
Input hold times: - Boundary-scan data - TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 – –	ns	(4)

Table 13-2. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (Continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Valid times: - Boundary-scan data - TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	(5)
Output hold times: - Boundary-scan data - TDO	t_{JTKLDX} t_{JTKLOX}	30 30		ns	(5)
JTAG external clock to output high impedance: - Boundary-scan data - TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	(5)(6)

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 13-1 on page 49). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 13-1 provides the AC test load for TDO and the boundary-scan outputs.

Figure 13-1. AC Test Load for the JTAG Interface

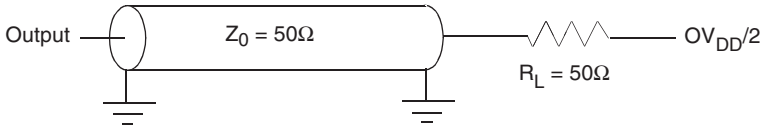
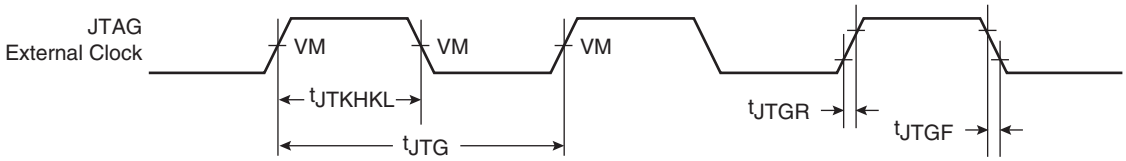


Figure 13-2 provides the JTAG clock input timing diagram.

Figure 13-2. JTAG Clock Input Timing Diagram



Note: VM = Midpoint Voltage (OV_{DD}/2).

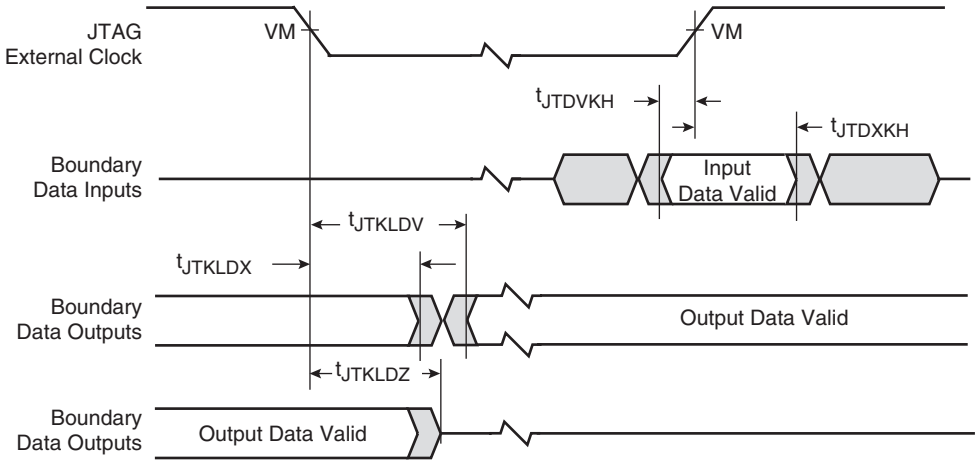
Figure 13-3 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 13-3. $\overline{\text{TRST}}$ Timing Diagram

Note: VM = Midpoint Voltage (OV_{DD}/2).

Figure 13-4 provides the boundary-scan timing diagram.

Figure 13-4. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage (OV_{DD}/2).

14. I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the PC8548E.

14.1 I^2C DC Electrical Characteristics

Table 14-1 provides the DC electrical characteristics for the I^2C interface.

Table 14-1. I^2C DC Electrical Characteristics (At Recommended Operating Conditions with OV_{DD} of 3.3V ± 5%)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	0.7 × OV_{DD}	OV_{DD} + 0.3	V	
Input low voltage level	V_{IL}	-0.3	0.3 × OV_{DD}	V	
Low level output voltage	V_{OL}	0	0.2 × OV_{DD}	V	(1)
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	(2)
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD} (max)	I_I	-10	10	µA	(3)
Capacitance for each I/O pin	C_I	–	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the PC8548E PowerQUICC III Integrated Host Processor Reference Manual for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

14.2 I^2C AC Electrical Specifications

Table 14-2 provides the AC timing parameters for the I^2C interfaces.

Table 14-2. I^2C AC Electrical Specifications (All Values Refer to V_{IH} (min) and V_{IL} (max) Levels (see Table 14-1)

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}[5]	1.3	–	µs
High period of the SCL clock	t_{I2CH}[5]	0.6	–	µs
Setup time for a repeated START condition	t_{I2SVKH}[5]	0.6	–	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}[5]	0.6	–	µs
Data setup time	t_{I2DVKH}[5]	100	–	ns
Data hold time: - CBUS[4] compatible masters - I^2C bus devices	t_{I2DXKL}	– 0[2]	– 0.9[3]	µs
Set-up time for STOP condition	t_{I2PVKH}	0.6	–	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3		µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$		V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$		V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. PC8548E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL. As a transmitter, the PC8548E provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When PC8548Eacts as the I^2C bus master while transmitting, PC8548E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, PC8548E would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for PC8548E as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I^2C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I^2C SCL clock frequency is 400 KHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I^2C Source Clock Frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR Bit Setting	0x2A	0x05	0x26	0x00
Actual FDR Divider Selected	896	704	512	384
Actual I^2C SCL Frequency Generated	371 KHz	378 KHz	390 KHz	346 KHz

For the detail of I^2C frequency calculation, refer to the application note AN2919 “Determining the I^2C Frequency Divider Ratio for SCL”. Note that the I^2C Source Clock Frequency is half of the CCB clock frequency for MPC8548E.

3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. Guaranteed by design.

Figure 14-1 provides the AC test load for the I^2C.

Figure 14-1. I^2C AC Test Load

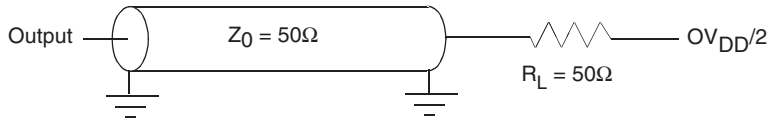
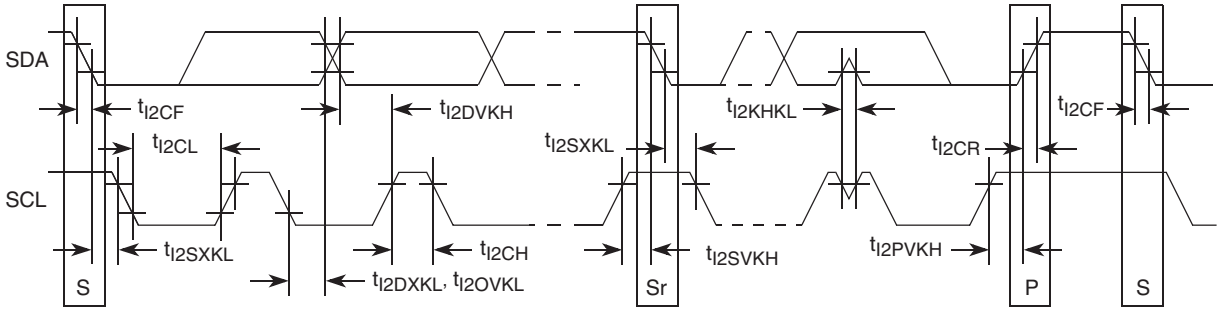


Figure 14-2 shows the AC timing diagram for the I^2C bus.

Figure 14-2. I^2C Bus AC Timing Diagram



15. PCI/PCI-X

Table 15-1 on page 52 describes the DC and AC electrical specifications for the PCI/PCI-X bus of the PC8548E. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

Table 15-1 provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 15-1. PCI/PCI-X DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[2] = 0V or V_{IN} = V_{DD})	I_{IN}	–	± 5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -100 μA)	V_{OH}	OV_{DD} – 0.2	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	–	0.2	V

Notes: 1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3-1 on page 10 and Table 3-2 on page 11.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for asynchronous mode and by PCI*n*_CLK when it is configured for asynchronous mode.

Table 15-2 provides the PCI AC timing specifications at 66 MHz.

Table 15-2. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	–	6	ns	(2)(3)
Output hold from SYSCLK	t_{PCKHOX}	2	–	ns	(2)(10)
SYSCLK to output high impedance	t_{PCKHOZ}	–	14	ns	(2)(4)(11)
Input setup to SYSCLK	t_{PCIVKH}	3	–	ns	(2)(5)(10)
Input hold from SYSCLK	t_{PCIXKH}	0	–	ns	(2)(5)(10)
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$[9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	–	clocks	(6)(7)(11)
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	(7)(11)
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	–	clocks	(8)(11)

Notes:
1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \cdot OV_{DD}$ of the signal in question for 3.3V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 20. ”Clocking” on page 85.
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI 2.2 Local Bus Specifications.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 ⌈s.
10. Guaranteed by characterization.
11. Guaranteed by design.

Figure 15-1 provides the AC test load for PCI and PCI-X.

Figure 15-1. PCI/PCI-X AC Test Load

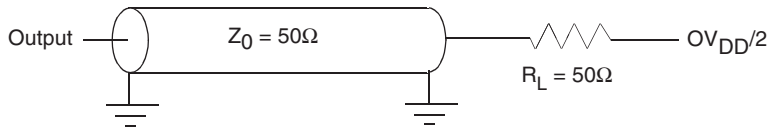


Figure 15-2 shows the PCI/PCI-X input AC timing conditions.

Figure 15-2. PCI/PCI-X Input AC Timing Measurement Conditions

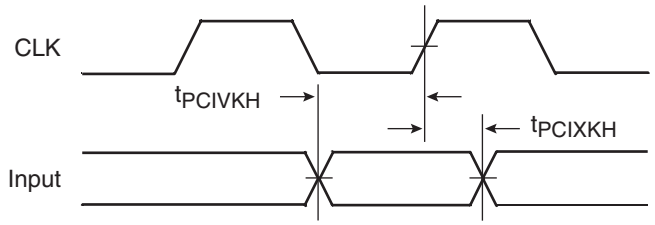


Figure 15-3 shows the PCI/PCI-X output AC timing conditions.

Figure 15-3. PCI/PCI-X Output AC Timing Measurement Condition

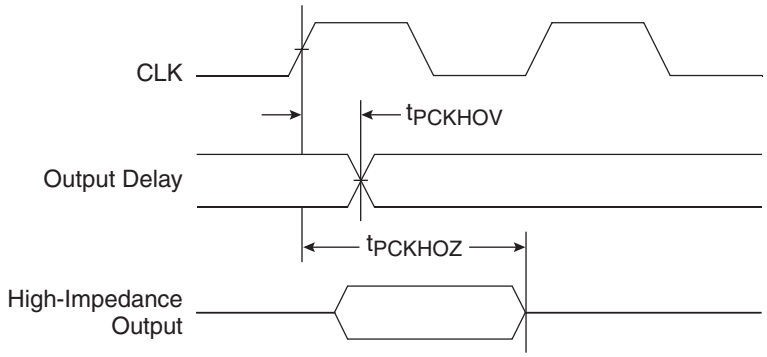


Table 15-3 provides the PCI-X AC timing specifications at 66 MHz.

Table 15-3. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	–	3.8	ns	(1)(2)(3)(7)(8)
Output hold from SYSCLK	t_{PCKHOX}	0.7	–	ns	(1)(10)
SYSCLK to output high impedance	t_{PCKHOZ}	–	7	ns	(1)(4)(8)(11)
Input setup time to SYSCLK	t_{PCIVKH}	1.7	–	ns	(3)(5)
Input hold time from SYSCLK	t_{PCIXKH}	0.5	–	ns	(10)
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$setup time	t_{PCRVRH}	10	–	clocks	(11)
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	(11)
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	–	clocks	(9)(11)
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	–	clocks	(11)
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	(6)(11)

Notes:
1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.

4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
10. Guaranteed by characterization.
11. Guaranteed by design.

Table 15-4 provides the PCI-X AC timing specifications at 133 MHz.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Table 15-4. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	–	3.8	ns	(1)(2)(3)(7)(8)
Output hold from SYSCLK	t_{PCKHOX}	0.7	–	ns	(1)(11)
SYSCLK to output high impedance	t_{PCKHOZ}	–	7	ns	(1)(4)(8)(12)
Input setup time to SYSCLK	t_{PCIVKH}	1.2	–	ns	(3)(5)(9)(11)
Input hold time from SYSCLK	t_{PCIXKH}	0.5	–	ns	(11)
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	–	clocks	(12)
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	(12)
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	–	clocks	(10)(12)
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	–	clocks	(12)
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	(6)(12)

Notes:
1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*
10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*
11. Guaranteed by characterization.
12. Guaranteed by design.

16. High-Speed Interfaces

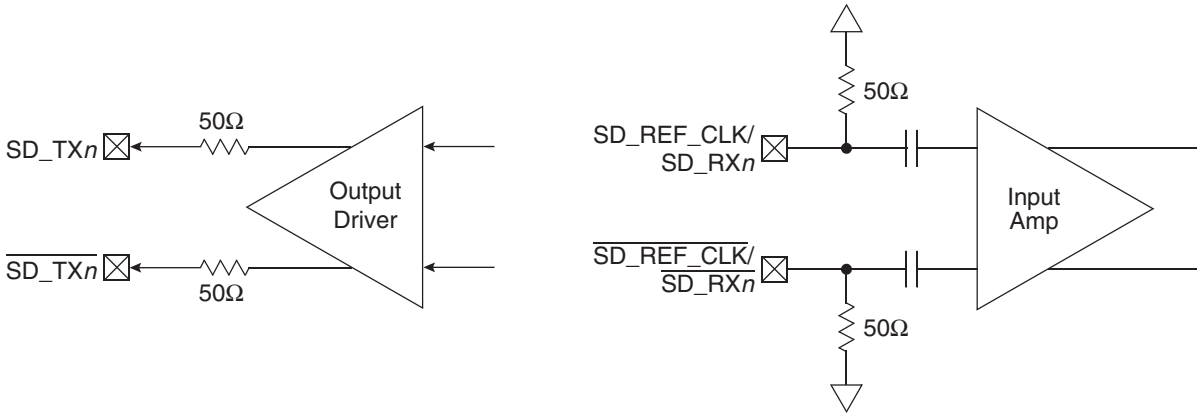
This section describes the common DC electrical specifications for the high-speed interconnect interfaces (Serial RapidIO and PCI Express) of the PC8548E.

16.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$.

- Recommended minimum operating voltage is -0.4V; recommended maximum operating voltage is 1.32V; Maximum absolute voltage is 1.72V.
- Each differential clock input has an internal 50Ω termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled on chip following the termination.
- The amplitude of the clock must be at least a 400 mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive ±100 mV around common mode voltage.
- The differential reference clock (SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$) input is HCSL compatible DC coupled or LVDS compatible with AC coupling.

Figure 16-1. Driver and Receiver of SerDes (PCI Express, Serial RapidIO, and SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$



16.2 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK_B was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

17. PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the PC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 16.1 ”DC Requirements for SerDes Reference Clocks” on page 56.

17.2 AC Requirements for PCI Express SerDes Clocks

Table 17-1 lists AC requirements.

Table 17-1. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	-	10	-	ns	(1)
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	–	–	100	ps	–
t_{REFPJ}	Phase jitter. Deviation edge location in edge location with respect to mean	-50	–	50	ps	–

Note: 1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million 15 (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

17.4.1 Differential Transmitter (TX) Output

Table 17-2 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 17-2. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note (1).
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note (2).
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. See Note (2).
T_{TX-EYE}	Minimum TX Eye Width	0.70			UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes (2) and (3).
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0V$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes (2) and (3).

Table 17-2. Differential Transmitter (TX) Output Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX-RISE, TTX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes (2) and (4)
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20	mV	$V_{TX-CM-ACp}$ = RMS($\|V_{TXD+}$- V_{TXD}-$\|$/2 -$V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+}$- $V_{TX-D-}\|$/2 See Note (2)
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During LO and Electrical Idle	0		100	mV	$\|V_{TX-CM-DC (during LO)}$ - $V_{TX-CM-Idle-DC (During Electrical Idle)}\|$<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+}$- $V_{TX-D-}\|$/2 [LO] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+}$ - $V_{TX-D-}\|$/2 [Electrical Idle] See Note (2).
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0		25	mV	$\|V_{TX-CM-DC-D+}$ - $V_{TX-CM-DC-D-}\|$ <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note (2).
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0		20	mV	$V_{TX-IDLE-DIFFp}$ = $\|V_{TX-IDLE-D+}$ -$V_{TX-IDLE-D-}\|$ <= 20 mV See Note (2).
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note (5).
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0		3.6	V	The allowed DC Common Mode voltage under any conditions. See Note (5).
$I_{TX-SHORT}$	TX Short Circuit Current Limit			90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50			UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set			20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from LO.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note (3)
RL_{TX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note (3)
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance

Table 17-2. Differential Transmitter (TX) Output Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
Z_{TX-DC}	Transmitter DC Impedance	40			Ω	Required TX D+ as wellall states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew			500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75		200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$T_{crosslink}$	Crosslink Random Timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note (6).

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 17-3 on page 63 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 17-1 on page 60.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes; see Figure 17-3 on page 63). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 17-3 on page 63 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a.
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 17-1 on page 60 is specified using the passive compliance/test measurement load (see Figure 17-3 on page 63) in place of any real PCI Express interconnect + RX component.

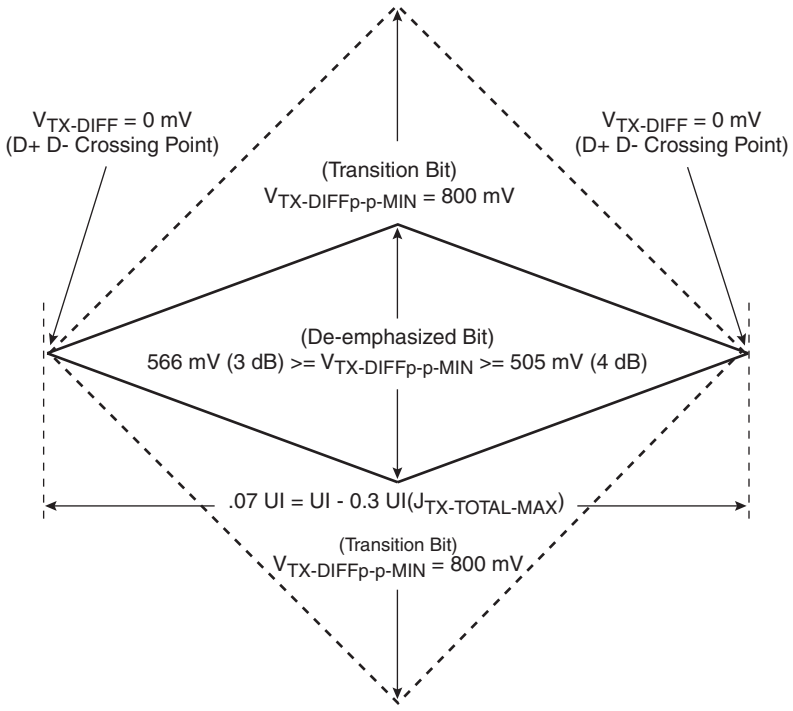
There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Note: It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

Figure 17-1. Minimum Transmitter Timing and Voltage Output Compliance Specifications



17.4.3 Differential Receiver (RX) Input Specifications

Table 17-3 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 17-3. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note (1).
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175		1.200	V	$V_{RX-DIFFp-p}$= 2*|V_{RX-D+} - V_{RX-D-}| See Note (2).
T_{RX-EYE}	Minimum Receiver Eye Width	0.4			UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE} = 0.6 UI. See Notes (2) and (3).
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes (2)(3)(7).

Table 17-3. Differential Receiver (RX) Input Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage			150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note (2)
$RL_{RX-DIFF}$	Differential Return Loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at +300 mV and -300 mV, respectively. See Note (4)
RL_{RX-CM}	Common Mode Return Loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at 0V. See Note (4)
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential (5)
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D-DC Impedance (50 ± 20% tolerance). See Notes (2) and (5)
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k			Ω	Required RX D+ as well as D-DC Impedance when the Receiver terminations do not have power. See Note (6)
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
$L_{TX-SKEW}$	Total	Skew		20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 17-3 on page 63 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 17-2 on page 62). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes - see Figure 17-3 on page 63). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 17-2 on page 62 is specified using the passive compliance/test measurement load (see Figure 17-3 on page 63) in place of any real PCI Express RX component.

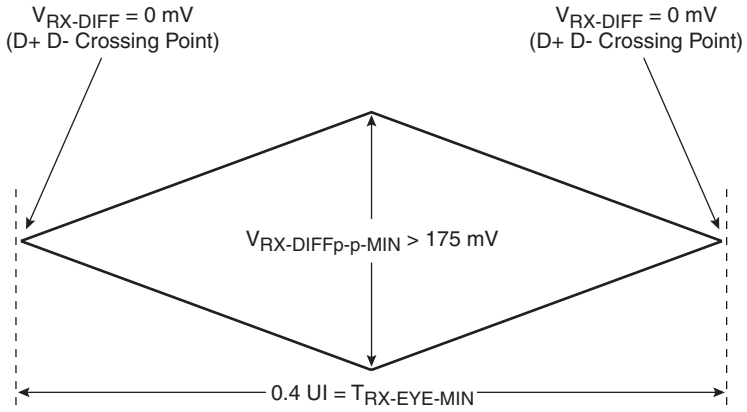
Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 17-3 on page 63) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 17-2) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Note: The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (i.e., as measured by a Vector Network Analyzer with 50. probes; see Figure 17-3 on page 63). Note that the series capacitors, CTX, are optional for the return loss measurement.

Figure 17-2. Minimum Receiver Eye Timing and Voltage Compliance Specification

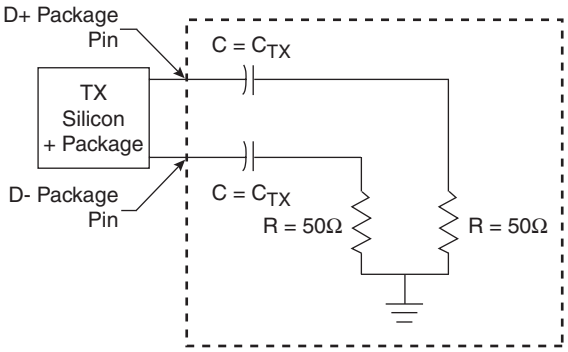


17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 17-3 on page 63.

Note: The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

Figure 17-3. Compliance Test/Measurement Load



18. Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the PC8548E, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

18.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 16.1 ”DC Requirements for SerDes Reference Clocks” on page 56.

18.2 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Table 18-1 lists AC requirements.

Table 18-1. SD n_REF_CLK and $\overline{\text{SDn\_REF\_CLK}}$ AC Requirements

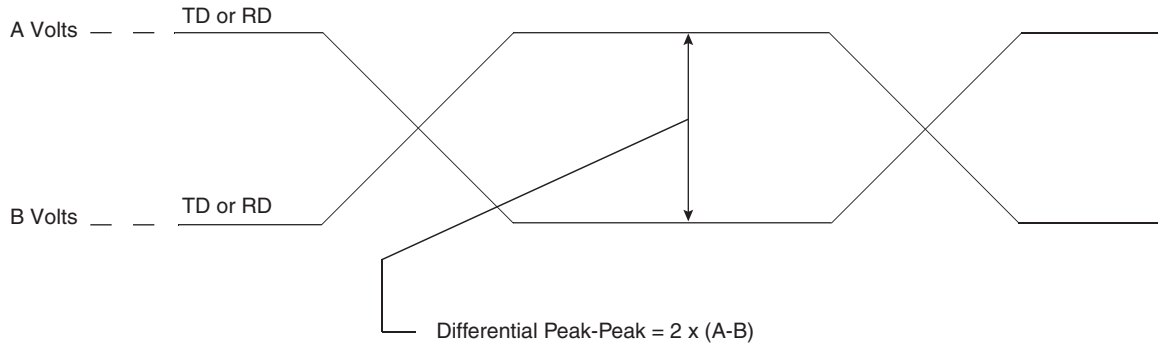
Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	–	10(8)	–	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	–	–	80	ps	–
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	-40	–	40	ps	

18.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 18-1 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A - B Volts
2. The differential output signal of the transmitter, V_{OD}, is defined as V_{TD}-$V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID}, is defined as V_{RD}-$V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A - B Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A - B) Volts

Figure 18-1. Differential Peak-Peak Voltage of Transmitter or Receiver



To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

18.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification.

To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 9.1 ”Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps) – GMII/MII/TBI/ RGMII/RTBI/RMII Electrical Characteristics” on page 24. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- -10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- -10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20% - 80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 18-2. Short Run Transmitter AC Timing Specifications: 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 18-3. Short Run Transmitter AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	± 100 ppm

Table 18-4. Short Run Transmitter AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	± 100 ppm

Table 18-5. Long Run Transmitter AC Timing Specifications: 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 18-6. Long Run Transmitter AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	± 100 ppm

Table 18-7. Long Run Transmitter AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	± 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 18-2 with the parameters specified in Table 18-8 when measured at the output pins of the device and the device is driving a 100Ω ±5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

Figure 18-2. Transmitter Output Compliance Mask

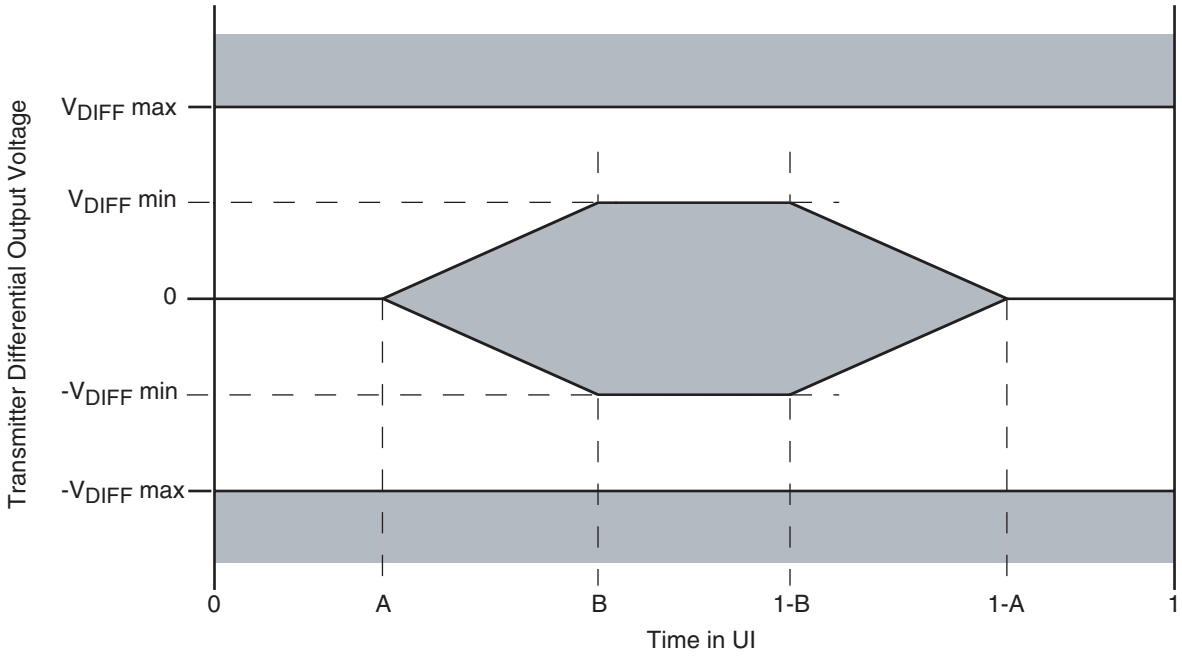


Table 18-8. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

18.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω resistive for differential return loss and 25Ω resistive for common mode.

Table 18-9. Receiver AC Timing Specifications – 1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance(1)	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	800	800	ps	± 100 ppm

Note: 1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18-3 on page 70. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 18-10. Receiver AC Timing Specifications: 2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance(1)	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	± 100 ppm

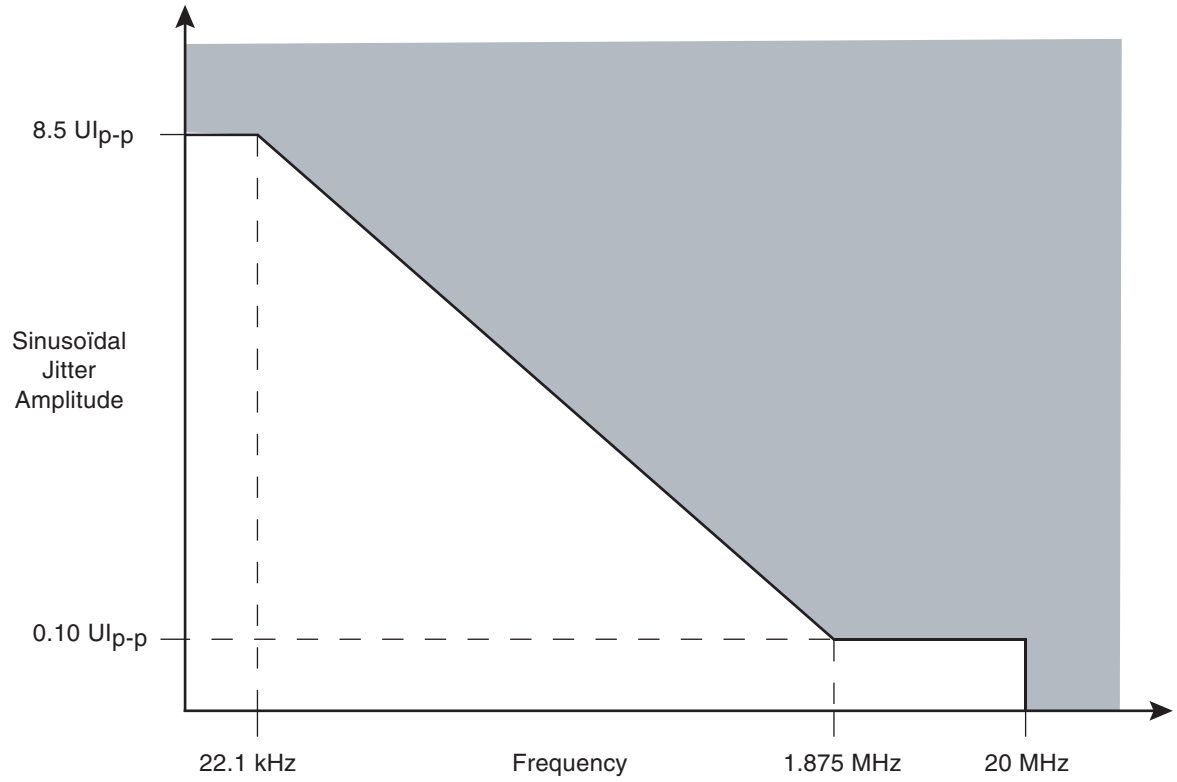
Note: Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18-3 on page 70. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 18-11. Receiver AC Timing Specifications: 3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Total Jitter Tolerance(1)	J_T	0.65		UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	± 100 ppm

Note: 1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18-3. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects

Figure 18-3. Single Frequency Sinusoidal Jitter Limits



18.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 18-9 on page 69, Table 18-10 on page 69, Table 18-11 on page 70) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 18-4 with the parameters specified in Table 18-12 on page 71. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ohm ± 5% differential resistive load.

Figure 18-4. Receiver Input Compliance Mask

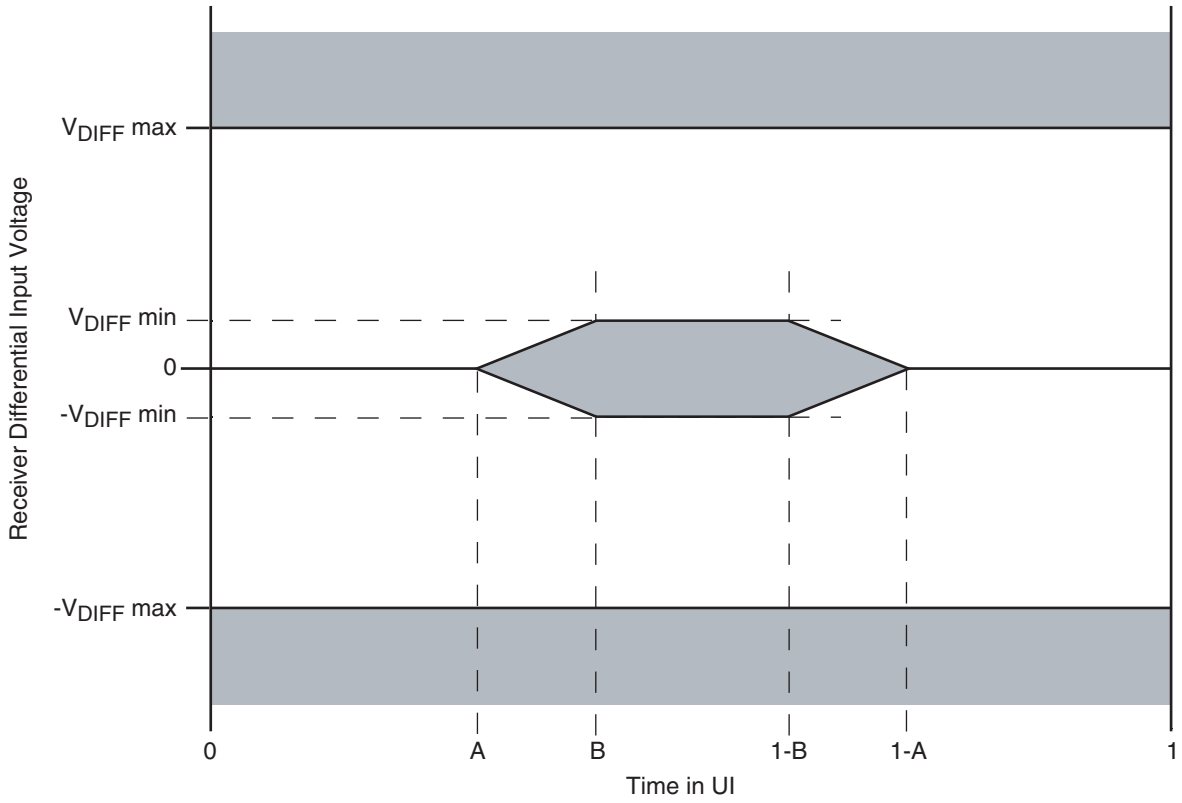


Table 18-12. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF} min (mV)	V_{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

18.9 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive ±5% differential to 2.5 GHz.

18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE802.3ae.

18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive ± 5% differential to 2.5 GHz.

18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

19. Package Description

This section details package parameters, pin assignments, and dimensions.

19.1 Package Parameters

The package parameters are as provided in the following list. The package type is 29 mm x 29 mm, 783 flip chip HITCE ball grid array (HITCE).

Table 19-1. Package Parameters

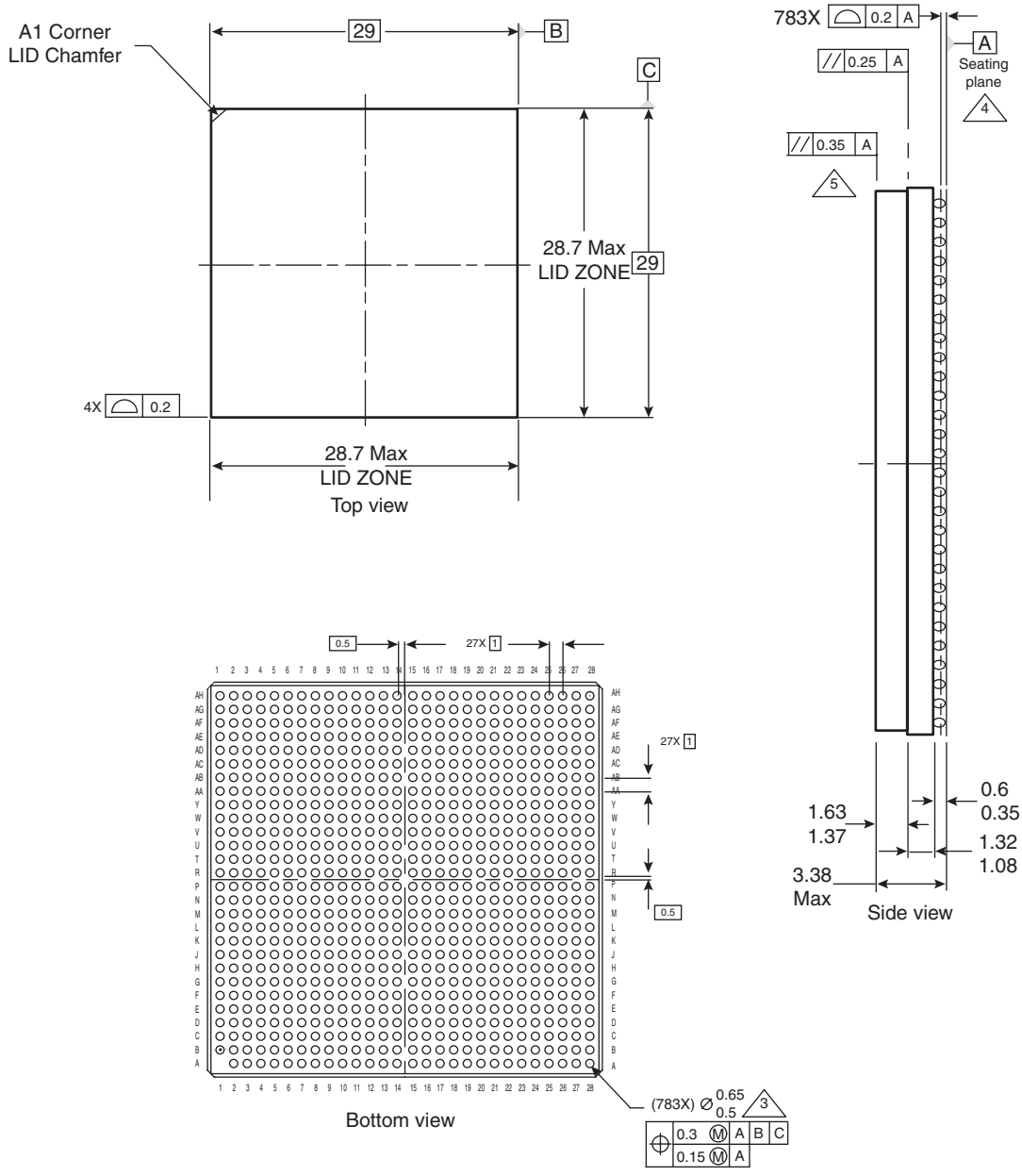
Parameter	CBGA[1]	PBGA[2]
Package outline	29 mm x 29 mm	29 mm x 29 mm
Interconnects	783	783
Ball pitch	1 mm	1 mm
Ball diameter (typical)	0.6 mm	0.6 mm
Solder ball (eutectic)	62% Sn 36% Pb 2% Ag	62% Sn 36% Pb 2% Ag
Solder ball high lead[3]	90% Sn 10pb	N.A.
Solder ball (lead-free)	96,5% Sn 3% Ag 0.5% Cu	96.5% Sn 3.5% Ag

Notes:
1. The HiCTE FC-CBGA package is available on Version 2.0 and 2.1 of the device.
2. The FC-PBGA package is available on only Version 2.1 of the device.
3. High lead solder spheres are upon request.

19.1.1 Mechanical Dimensions of the HITCE

Figure 19-1 shows the mechanical dimensions and bottom surface nomenclature of the 783 HITCE package.

Figure 19-1. Mechanical Dimensions of the HITCE FC-CBGA with Full Lid



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
7. All dimensions are symetric across the package center lines, unless dimensioned otherwise.

19.2 Pinout Listings

Note: The DMA_DACK[0:1] and TEST_SEL/ TEST_SEL pins must be set to a proper state during POR configuration. Please refer to the pinlist table of the individual device for more details.
For PC8548/47/45, GPIOs are still available on PCI1_AD[63:32]/PC2_AD[31:0] pins if they are not used for PCI funcationality.
For MPC8545/43, eTSEC does not support 16 bit FIFO mode.

Table 19-2 provides the pin-out listing for the PC8548E 783 HITCE package.

Table 19-2. PC8548E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (one 64-bit or two 32-bit)				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV_{DD}	(16)
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	(16)
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV_{DD}	(16)
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	(16)
PCI1_PAR64/PCI2_PAR	W15	I/O	OV_{DD}	
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	(4)(8)(29)
PCI1_GNT0	AG5	I/O	OV_{DD}	
PCI1_IRDY	AF11	I/O	OV_{DD}	(2)
PCI1_PAR	AD12	I/O	OV_{DD}	
PCI1_PERR	AC12	I/O	OV_{DD}	(2)
PCI1_SERR	V13	I/O	OV_{DD}	(2)(3)
PCI1_STOP	W12	I/O	OV_{DD}	(2)
PCI1_TRDY	AG11	I/O	OV_{DD}	(2)
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV_{DD}	
PCI1_REQ0	AH3	I/O	OV_{DD}	
PCI1_CLK	AH26	I	OV_{DD}	(32)
PCI1_DEVSEL	AH11	I/O	OV_{DD}	(2)
PCI1_FRAME	AE11	I/O	OV_{DD}	(2)
PCI1_IDSEL	AG9	I	OV_{DD}	
PCI1_REQ64/PCI2_FRAME	AF14	I/O	OV_{DD}	(2)(4)(9)
PCI1_ACK64/PCI2_DEVSEL	V15	I/O	OV_{DD}	(2)

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_CLK	AE28	I	OV_{DD}	(2)
$\overline{\text{PCI2\_IRDY}}$	AD26	I/O	OV_{DD}	(2)
$\overline{\text{PCI2\_PERR}}$	AD25	I/O	OV_{DD}	(2)
$\overline{\text{PCI2\_GNT}}$[4:1]	AE26, AG24, AF25, AE25	O	OV_{DD}	(4)(8)(29)
$\overline{\text{PCI2\_GNT0}}$	AG25	I/O	OV_{DD}	
$\overline{\text{PCI2\_SERR}}$	AD24	I/O	OV_{DD}	(2)(3)
$\overline{\text{PCI2\_STOP}}$	AF24	I/O	OV_{DD}	(2)
$\overline{\text{PCI2\_TRDY}}$	AD27	I/O	OV_{DD}	(2)
$\overline{\text{PCI2\_REQ}}$[4:1]	AD28, AE27, W17, AF26	I	OV_{DD}	
$\overline{\text{PCI2\_REQ0}}$	AH25	I/O	OV_{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV_{DD}	
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV_{DD}	
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV_{DD}	
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV_{DD}	
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV_{DD}	
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV_{DD}	
MBA[0:2]	F7, J7, M11	O	GV_{DD}	
$\overline{\text{MWE}}$	E7	O	GV_{DD}	
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	(10)
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	
MDIC[0:1]	A19, B19	I/O	GV_{DD}	(30)
Local Bus Controller Interface				

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV_{DD}	
LDP[0:3]	K21, C28, B26, B22	I/O	BV_{DD}	
LA[27]	H21	O	BV_{DD}	(4)(8)
LA[28:31]	H20, A27, D26, A28	O	BV_{DD}	(4)(6)(8)
$\overline{\text{LCS}}$[0:4]	J25, C20, J24, G26, A26	O	BV_{DD}	
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	D23	I/O	BV_{DD}	(1)
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	G20	O	BV_{DD}	(1)
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	E21	O	BV_{DD}	(1)
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0]	G25	O	BV_{DD}	(4)(8)
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1]	C23	O	BV_{DD}	(4)(8)
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2]	J21	O	BV_{DD}	(4)(8)
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3]	A24	O	BV_{DD}	(4)(8)
LALE	H24	O	BV_{DD}	(4)(7)(8)
LBCTL	G27	O	BV_{DD}	(4)(7)(8)
LGPL0/LSDA10	F23	O	BV_{DD}	(4)(8)
LGPL1/$\overline{\text{LSDWE}}$	G22	O	BV_{DD}	(4)(8)
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	B27	O	BV_{DD}	(4)(7)(8)
LGPL3/$\overline{\text{LSDCAS}}$	F24	O	BV_{DD}	(4)(8)
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	H23	I/O	BV_{DD}	
LGPL5	E26	O	BV_{DD}	(4)(8)
LCKE	E24	O	BV_{DD}	
LCLK[0:2]	E23, D24, H22	O	BV_{DD}	
LSYNC_IN	F27	I	BV_{DD}	
LSYNC_OUT	F28	O	BV_{DD}	
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV_{DD}	(4)(8)(35)
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV_{DD}	
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV_{DD}	
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV_{DD}	
$\overline{\text{MCP}}$	AG19	I	OV_{DD}	
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV_{DD}	

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[8]	AF19	I	OV_{DD}	
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV_{DD}	(1)
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV_{DD}	(1)
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV_{DD}	(1)
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV_{DD}	(2)(3)
Ethernet Management Interface				
EC_MDC	AB9	O	OV_{DD}	(4)(8)
EC_MDIO	AC8	I/O	OV_{DD}	
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV_{DD}	
Three-SpeeDEthernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV_{DD}	
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV_{DD}	(4)(8)
TSEC1_COL	R4	I	LV_{DD}	
TSEC1_CRS	V5	I/O	LV_{DD}	(18)
TSEC1_GTX_CLK	U7	O	LV_{DD}	
TSEC1_RX_CLK	U3	I	LV_{DD}	
TSEC1_RX_DV	V2	I	LV_{DD}	
TSEC1_RX_ER	T1	I	LV_{DD}	
TSEC1_TX_CLK	T6	I	LV_{DD}	
TSEC1_TX_EN	U9	O	LV_{DD}	(24)
TSEC1_TX_ER	T7	O	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	P2, R2, N1, N2, P3, M2, M1, N3	I		
TSEC2_TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	O		
TSEC2_COL	P1	I		
TSEC2_CRS	R6	I/O		
TSEC2_GTX_CLK	P6	O		
TSEC2_RX_CLK	N4	I		
TSEC2_RX_DV	P5	I		
TSEC2_RX_ER	R1	I	LV_{DD}	
TSEC2_TX_CLK	P10	I	LV_{DD}	
TSEC2_TX_EN	P7	O	LV_{DD}	(24)
TSEC2_TX_ER	R10	O	LV_{DD}	(4)(8)(27)
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	(4)(8)(23)
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	
TSEC3_GTX_CLK	W8	O	TV_{DD}	
TSEC3_RX_CLK	W2	I	TV_{DD}	
TSEC3_RX_DV	W1	I	TV_{DD}	
TSEC3_RX_ER	Y2	I	TV_{DD}	
TSEC3_TX_CLK	V10	I	TV_{DD}	
TSEC3_TX_EN	V9	O	TV_{DD}	(24)
Three-Speed Ethernet Controller (Gigabit Ethernet 4)				
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	(1)(4)(8)(23)
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	(1)
TSEC4_GTX_CLK	AA5	O	TV_{DD}	
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV_{DD}	(1)
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV_{DD}	(1)(25)
TSEC4_TX_EN/TSEC3_TX_ER	AB6	O	TV_{DD}	(1)(24)
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	
I^2C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	(3)(22)
IIC1_SDA	AG21	I/O	OV_{DD}	(3)(22)
IIC2_SCL	AG15	I/O	OV_{DD}	(3)(22)
IIC2_SDA	AG14	I/O	OV_{DD}	(3)(22)
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV_{DD}	
$\overline{\text{SD\_RX}}$[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV_{DD}	
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	
$\overline{\text{SD\_TX}}$[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	
SD_PLL_TPD	U28	O	XV_{DD}	(19)
SD_REF_CLK	T28	I	XV_{DD}	
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	
Reserved	AC1, AC3	–	–	(2)
Reserved	M26, V28	–	–	(33)

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	M25, V27	–	–	(28)
Reserved	M20, M21, T22, T23	–	–	(31)
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	(23)
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	(2)(3)
Debug				
TRIG_IN	AB2	I	OV_{DD}	
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	(5)(8)(17) (23)
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	(4)(5)(8)
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	(5)(17)(23)
MDVAL	AE5	O	OV_{DD}	(5)
CLK_OUT	AE21	O	OV_{DD}	(10)
Clock				
RTC	AF16	I	OV_{DD}	
SYSCLK	AH17	I	OV_{DD}	
JTAG				
TCK	AG28	I	OV_{DD}	
TDI	AH28	I	OV_{DD}	(11)
TDO	AF28	O	OV_{DD}	(10)
TMS	AH27	I	OV_{DD}	(11)
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	(11)
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	(20)
L2_TSTCLK	AE22	I	OV_{DD}	(20)
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	(20)
$\overline{\text{TEST\_SEL}}$	AH14	I	OV_{DD}	(20)
Thermal Management				
THERM0	AG1		–	(13)
THERM1	AH1		–	(13)

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power Management				
ASLEEP	AH18	O	OV_{DD}	(8)(17)(23)
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27 K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28 L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21 U27	–	–	
OVDD	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3V)	OV_{DD}	
LVDD	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5V ,3.3V)	LV_{DD}	
TVDD	W9, Y6	Power for TSEC3 and TSEC4 (2,5V, 3.3V)	TV_{DD}	
GVDD	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/Ovoltage (1.8V,2.5V)	GV_{DD}	
BVDD	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for Local Bus (1.8V, 2.5V, 3.3V)	BV_{DD}	
VDD	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for Core (1.1V)	V_{DD}	

Table 19-2. PC8548E Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SVDD	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1V)	SV_{DD}	
XVDD	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1V)	XV_{DD}	
AVDD_LBIU	J28	Power for local bus PLL (1.1V)		(21)
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1V)		(21)
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1V)		(21)
AVDD_CORE	AH15	Power for e500 PLL (1.1V)		(21)
AVDD_PLAT	AH19	Power for CCB PLL (1.1V)		(21)
AVDD_SRDS	U25	Power for SRDSPLL (1.1V)		(21)
SENSEVDD	M14	O	V_{DD}	(12)
SENSEVSS	M16			(12)
Analog Signals				
MV_{REF}	A18	I Reference voltage signal for DDR	MV_{REF}	
SD_IMP_CAL_RX	L28	I	200Ω to GND	
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	O		(19)

Notes: 1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.

2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.

3. This pin is an open drain signal.

4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
5. Treat these pins as no connects (NC) unless using debug address functionality.
6. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. See Section 20.2 ”CCB/SYSCLK PLL Ratio” on page 85.
7. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. See the Section 20.3 ”e500 Core PLL Ratio” on page 86.
8. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
9. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the PCI Specification.
10. This output is actively driven during reset rather than being three-stated during reset.
11. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
12. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
13. Internal thermally sensitive resistor.
14. No connections should be made to these pins if they are not used.
15. These pins are not connected for any use.
16. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and $\overline{\text{PCI1\_C\_BE}}$[7:4]).
17. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
18. This pin is only an output in FIFO mode when used as Rx Flow Control.
19. Do not connect.
20. These are test signals for factory use only and must be pulled up (100 . - 1 k.) to OV_{DD} for normal machine operation.
21. Independent supplies derived from board V_{DD}.
22. Recommend a pull-up resistor (~1 K.) b placed on this pin to OV_{DD}.
23. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], TSEC4_TXD3/TSEC3_TXD7, HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. For rev 2.0 silicon, cfg_srds_en added to TSEC4_TXD[2]/TSEC3_TXD[6] -This POR config powers down the SERDES block entirely if pulled down. If the SERDES is going to be used in any way, then this pin should be pulled up or it can be left without a pullup or pulldown. For Rev. 1.x/Rev 1.1.x silicon, TSEC4_TXD[2:3] pin values during POR configuration are don’t care.
24. This pin requires an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
25. This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.
26. These pins should be connected to XV_{DD}.
27. TSEC2_TXD1, TSEC2_TX_ER are multiplexedas cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
28. These pins should be pulled to ground through a 300Ω (±10%) resistor.
29. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI n_AD pins as "No Connect" or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCI n_AD pins are not connected to any other PCI device. The PCI block will drive the PCI n_AD pins if it is configured to be the PCI arbiter, through POR config pins, irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
30. MDIC0 is grounded through an 18.2Ω precision 1% resistor and MDIC1 is connected to GV_{DD} through an 18.2Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

31. These pins should be left floating.
32. If PCI1 or PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK or PCI2_CLK. Otherwise the processor will not boot up.
33. These pins should be connected to GND.
34. This pin requires an external 4.7 kΩ resistor to GND.
35. For Rev. 2.0 silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b11 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
36. If these pins are not used as GPINn (general-purpose input), they should be pulled low (to GND) or high (to LV_{DD}) through 2–10 kΩ resistors.
37. These should be pulled low to GND through 2–10 kΩ resistors if they are not used.
38. These should be pulled low or high to LV_{DD} through 2–10 kΩ resistors if they are not used.
39. For Rev. 2.0 silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b10 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
40. For Rev. 2.0 silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b01 during POR configuration; for Rev. 1.x silicon, the pin values during POR configuration are don't care.
41. For Rev. 2.0 silicon, $\overline{\text{DMA\_DACK}}$[0:1] must be 0b11 during POR configuration; for Rev. 1.x silicon, the pin values during POR -+configuration are don't care.
42. This is a test signal for factory use only and must be pulled down (100Ω – 1 kΩ) to GND for normal machine operation.
43. These pins should be pulled high to OV_{DD} through 2–10 kΩ resistors.
44. If these pins are not used as GPINn (general-purpose input), they should be pulled low (to GND) or high (to OV_{DD}) through 2–10 kΩ resistors.
45. This pin must not be pulled down during POR configuration.
46. These should be pulled low or high to OV_{DD} through 2–10 kΩ resistors.

20. Clocking

This section describes the PLL configuration of the PC8548E. Note that the platform clock is identical to the core complex bus (CCB) clock.

20.1 Clock Ranges

Table 20-1 provides the clocking specifications for the processor cores and Table 20-2 provides the clocking specifications for the memory bus.

Table 20-1. Processor Core Clocking Specifications

	Maximum Processor Core Frequency							
	1000 MHz		1200 MHz		1333 MHz			
Characteristic	Min	Max	Min	Max	Min	Max	Unit	Notes
e500 core processor frequency	533	1000	533	1200	533	1333	MHz	(1)(2)

Notes:
1. Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 20.2 ”CCB/SYSCLK PLL Ratio” on page 85, and Section 20.3 ”e500 Core PLL Ratio” on page 86, for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 266 MHz.

Table 20-2. Memory Bus Clocking Specifications

	Maximum Processor Core Frequency			
	1000, 1200, 1333 MHz			
Characteristic	Min	Max	Unit	Notes
Memory bus clock speed	133	266	MHz	(1)(2)

Notes:
1. Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 20.2 ”CCB/SYSCLK PLL Ratio” on page 85, and Section 20.3 ”e500 Core PLL Ratio” on page 86, for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

20.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock.

The frequency of the CCB is set using the following reset signals, as shown in Table 20-3:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the bus frequency, since the frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 20-3. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1
1010	10:1
1011	Reserved
1100	12:1
1101	20:1
1110	Reserved
1111	Reserved

20.3 e500 Core PLL Ratio

Table 20-4 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in Table 20-4.

Table 20-4. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1
001	9:2
010	1:1
011	3:2
100	2:1
101	5:2
110	3:1
111	7:2

20.4 Frequency Options

20.4.1 Sysclk to Platform Frequency Options

Table 20-5 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 20-5. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)									
	16.66	25	33.33	41.66	66.66	83	100	111	133.33	166
	Platform/CCB Frequency (MHz)									
2									267	332
3							300	333	400	498
4					267	333	400	445	533	
5					333	415	500			
6					400	500				
8			267	333	533					
9			300	375						
10			333	417						
12		300	400	500						
16	267	400	533							
20	333	500								

21. Thermal

This section describes the thermal specifications of the PC8548.

21.1 Thermal for Revision 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

Table 21-1 shows the package thermal characteristics.

Table 21-1. Package Thermal Characteristics for HiCTE FC-CBGA

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die Junction-to-Ambient (Natural Convection)	Single-layer board (1s)	$R_{\Theta JA}$	17	°C/W	(1)(2)
Die Junction-to-Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\Theta JA}$	12	°C/W	(1)(2)
Die Junction-to-Ambient (200 ft/min)	Single-layer board (1s)	$R_{\Theta JA}$	11	°C/W	(1)(2)
Die Junction-to-Ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\Theta JA}$	8	°C/W	(1)(2)
Die Junction-to-Board	N/A	$R_{\Theta JB}$	3	°C/W	(3)
Die Junction-to-Case	N/A	$R_{\Theta JC}$	0.8	°C/W	(4)

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.2 Thermal for Version 2.1 Silicon FC-PBGA with Full Lid

This section describes the thermal specifications for the FC-PBGA package for revision 2.1 silicon.

Table 21-2 shows the package thermal characteristics.

Table 21-2. Package Thermal Characteristics for HiCTE FC-PBGA

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die Junction-to-Ambient (Natural Convection)	Single-layer board (1s)	$R_{\Theta JA}$	18	°C/W	(1)(2)
Die Junction-to-Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\Theta JA}$	13	°C/W	(1)(2)
Die Junction-to-Ambient (200 ft/min)	Single-layer board (1s)	$R_{\Theta JA}$	13	°C/W	(1)(2)
Die Junction-to-Ambient (200 ft/min)	Four-layer board (2s2p)	$R_{\Theta JA}$	9	°C/W	(1)(2)
Die Junction-to-Board	N/A	$R_{\Theta JB}$	5	°C/W	(3)
Die Junction-to-Case	N/A	$R_{\Theta JC}$	0.8	°C/W	(4)

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed circuit board is the recommended procedure using a maximum of 10 lbs. force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

22. System Design Information

This section provides electrical and thermal design recommendations for successful application of the PC8548E.

22.1 System Clocking

This device includes five PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 20.2 ”CCB/SYSCLK PLL Ratio” on page 85.
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 20.3 ”e500 Core PLL Ratio” on page 86.
3. The PCI PLL generates the clocking for the PCI bus
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.

22.2 Power Supply Design

22.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 22-1, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

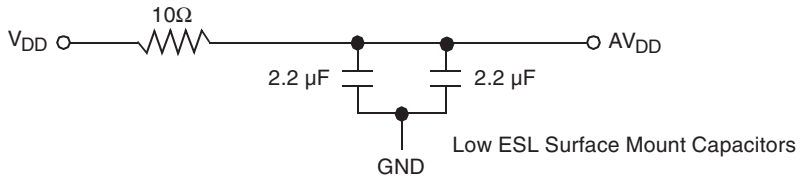
This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL).

Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 HITCE the footprint, without the inductance of vias.

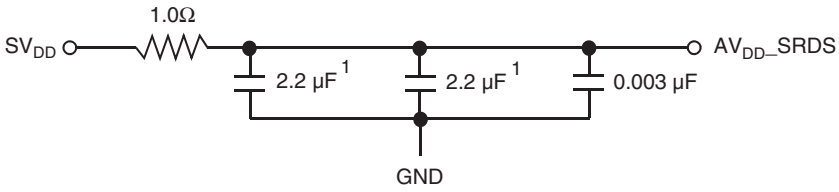
Figure 22-1 shows the PLL power supply filter circuits.

Figure 22-1. PC8548E PLL Power Supply Filter Circuit



The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS ball. The 0.003 µF capacitor is closest to the ball, followed by the 1 µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

Figure 22-2. SerDes PLL Power Supply Filter



Note: 1. An 0805 sized capacitor is recommended for system initial bring-up.

Note the following:

- AV_{DD}_SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Power: XV_{DD} consumes less than 300 mW; SV_{DD} + AV_{DD}_SRDS consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads.

This noise must be prevented from reaching other components in the PC8548E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD},pin of the device. These decoupling capacitors should receive their power from separate V_{DD},TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD},and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD},planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10 nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1 µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10 µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100 µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD},TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD},TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The PC8548E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 22-5 on page 95. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The $\overline{\text{DMA\_DACK}}$[0:1] and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. Please refer to the pinlist table of the individual device for more details.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

22.7 Output Buffer DC Impedance

The PC8548E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 22-3). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 22-3. Driver Impedance Measurement

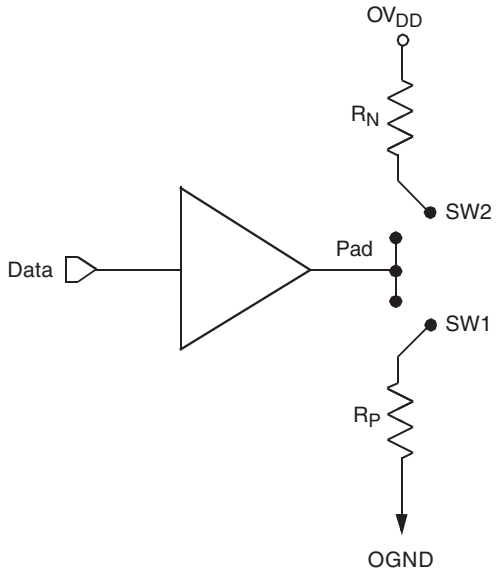


Table 22-1 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 22-1. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 3-1 on page 10, T_C = 105°C.

22.8 Configuration Pin Muxing

The PC8548E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7 kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 22-5 on page 95 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 22-5 on page 95, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 22-5 is common to all known emulators.

22.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 22-4. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

Figure 22-4. COP Connector Physical Pinout

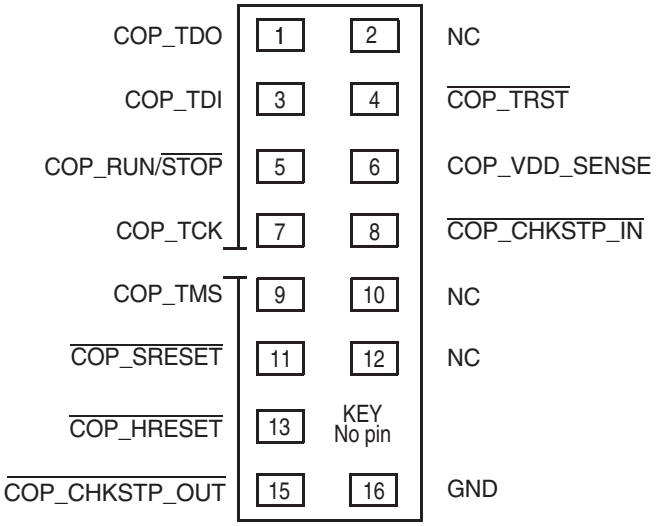
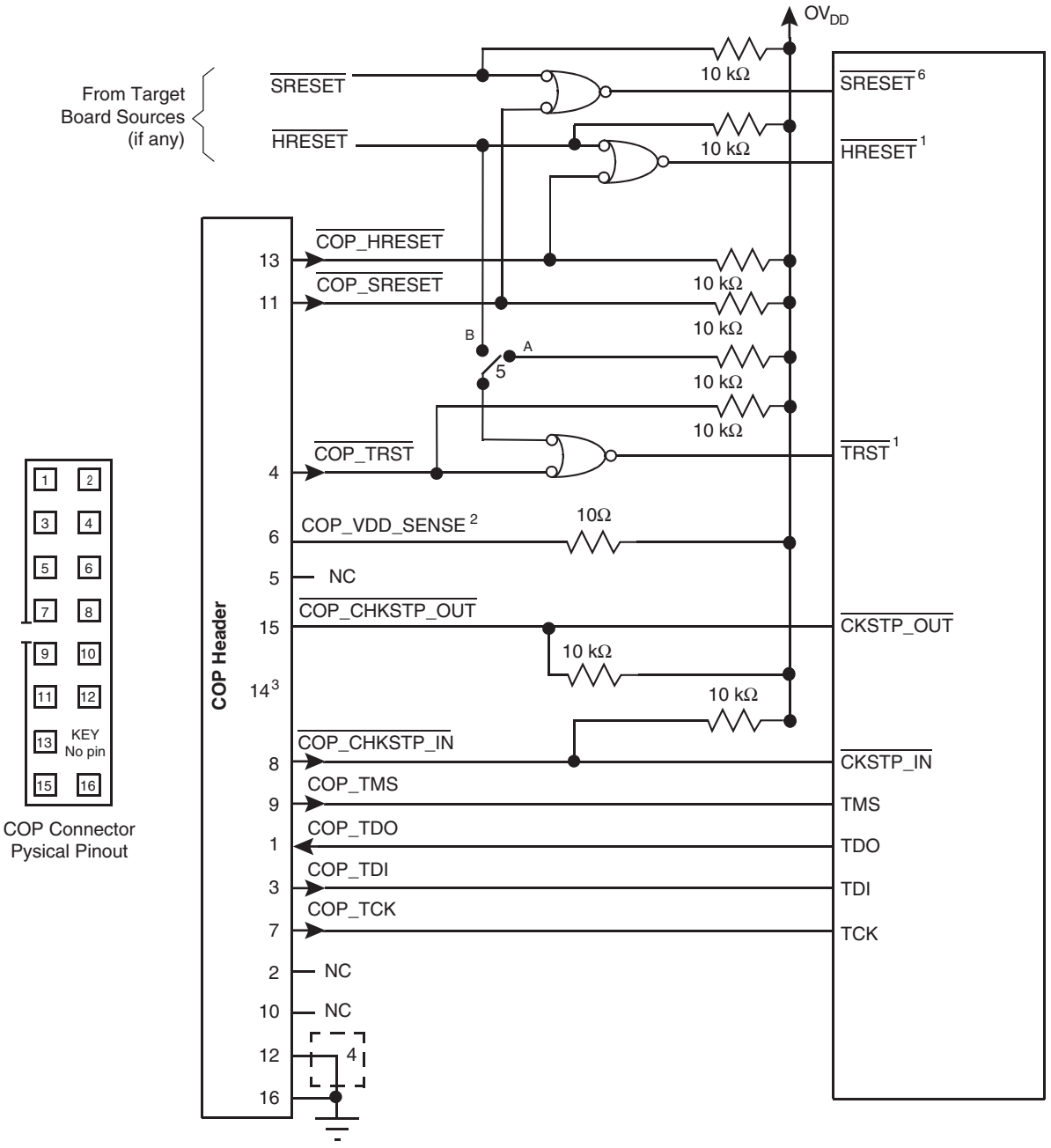


Figure 22-5. JTAG Interface Connection



Note:
1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

22.10 Guidelines for High-Speed Interface Termination

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- SD_RX[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

Note: It is recommended to power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2] /TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

Note: It is recommended to power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300Ω resistor.

22.11 Guideline for PCI Interface Temination

PCI termination if PCI 1 or PCI 2 is not used at all.

Option 1

If PCI arbiter is enabled during POR,

- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10 kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

If PCI arbiter is disabled during POR,

- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10 kΩ resistor(s)
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10K resistor
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.12 Guideline for LBIU Parity Temination

In LBIU parity pins are not used. Here is the termination recommendation:

For LDP[0:3]: tie them to ground or the power supply rail via a 4.7K resistor.

For LPBSE: tie it to the power supply rail via a 4.7K resistor (pull-up resistor).

23. Definitions

23.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

24. Ordering Information

Figure 24-1. Ordering Information

xx	8548	y	xx	U	xx	x	x
Product Code(1)	Part Identifier	Temperature Range(1)	Package(1)	Screening Level	Processor Frequency	Platform Frequency	Revision Level(1)
PC(X)(2)	8548E	V: T_C = -40˚C ; T_J = 110˚C M: T_C = -55˚C ; T_J = 125˚C	GH = HiTCE CBGA LH = HiTCE LGA GHY = ROHS BGA ZF = PBGA	Blank : Standard U: Upscreening	AV = 1500 MHz (TBC) AU = 1333 MHz (TBC) AT = 1200 MHz AQ = 1000 MHz AN = 800 MHz	J = 533 MHz (TBC) G = 400 MHz	Blank = 2.0 A = version 2.1

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

25. Document Revision History

Table 25-1 provides a revision history for this hardware specification.

Table 25-1. Document Revision History

Revision Number	Date	Substantive Change(s)
C	04/2008	Tc replaced by T_J
B	11/2007	• Adjusted maximum SYSCLK frequency down in Table 6, “SYSCLK AC Timing Specifications” per device eratum GEN-13 • Clarified notes to Table 5-2 on page 16 • Added Section 5.4 ”PCI/PCI-X Reference Clock Timing” on page 16 • Clarified descriptions and added PCI/PCI-X to Table 6-2 • Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 7. ”DDR and DDR2 SDRAM” on page 18 • Clarified Note 4 of Table 7-9 on page 21 • Clarified the reference clock used in Section 8.2 ”DUART AC Electrical Specifications” on page 23 • Corrected VIH(min) in Table 9-1 on page 24 • Corrected VIL(max) in Table 9-2 on page 25 • Removed DC parameters from Table 9-3 on page 26, Table 9-5 on page 27, Table 9-5 on page 27, Table 9-6 on page 28, Table 9-7 on page 29, Table 9-14 on page 35, Table 9-11 on page 33, Table 9-13 on page 34 and Table 9-14 on page 35 • Corrected V_{IH}(min) in Table 10-1, “MII Management DC Electrical Characteristics,” on page 36 • Corrected t_{MDC}(min) in Table 10-2, “MII Management AC Timing Specifications (At Recommended Operating Conditions with OVDD is 3.3V ± 5%),” on page 37 • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKH2}$, $t_{LBIXKH1}$, and $t_{LBIXKH2}$ in Table 11-4, “Local Bus Timing Parameters (BVDD = 2.5V): PLL Enabled,” on page 40 and Table 11-5, “Local Bus Timing Parameters: PLL Bypassed,” on page 42 • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKL2}$, $t_{LBIXKH1}$, and $t_{LBIXKL2}$ in Table 11-5, “Local Bus Timing Parameters: PLL Bypassed,” on page 42 Note that $t_{LBIVKL2}$ and $t_{LBIXKL2}$ were previously labeled $t_{LBIVKH2}$ and $t_{LBIXKH2}$ • Added LUPWAIT signal to Figure 11-2 on page 41 and Figure 11-4 on page 44. • Added LGTA signal to Figure 11-4, Figure 11-6, Figure 11-5 and Figure 11-7 • Corrected LUPWAIT assertion in Figure 11-5 and Figure 11-7 • Clarified the PCI reference clock in Section 15.2 ”PCI/PCI-X AC Electrical Specifications” on page 53 • Updated Figure 16-1 on page 56 • Added Section 19.1 ”Package Parameters” on page 73 • Added PBGA thermal information in Section 21.2 ”Thermal for Version 2.1 Silicon FC-PBGA with Full Lid” on page 88 • Updated Section 21.3 ”Heat Sink Solution” on page 89
A	08/2007	Initial revision

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