

8M BIT (1M WORD × 8 BIT) CMOS MASK ROM

T-46-13-15

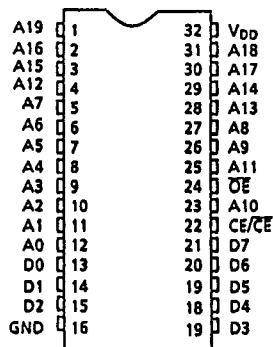
DESCRIPTION

The TC538000P/F is a 8,388,608 bits read only memory organized as 1,048,576 words by 8bits.
 The TC538000P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 200ns, an operation current of 40mA at 5MHz and a standby current of 100µA.
 The TC538000P/F has one programmable chip enable input CE/CE for device selection.
 The TC538000P/F is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns (Max.) $V_{DD}=5V \pm 10\%$
- Power Dissipation
 - Operating Current : 40mA (Max.)
 - Standby Current : 1000µA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC538000P : DIP32-P-600
- TC538000F : SOP32-P-525

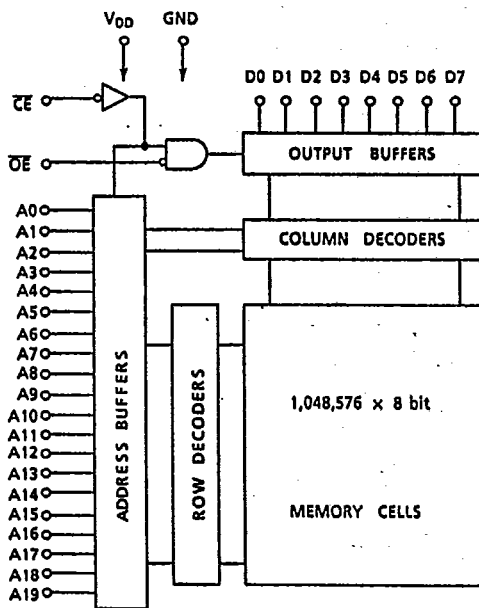
PIN CONNECTION



PIN NAMES

A0~A19	Address Inputs
D0~D7	Data Outputs
OE	Output Enable Input
CE/CE	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC538000P/F-20

TOSHIBA (LOGIC/MEMORY)

42E D

9097248 0021905 3 TOS2

MAXIMUM RATINGS

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SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~ V_{DD}	V
V_{OUT}	Output Voltage	0~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	-55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : * Plastic FP.

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	± 1.0	μA
I_{LO}	Output Leakage Current	$\bar{C}E = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	-	mA
I_{DDs1}	Standby Current	$\bar{C}E = V_{IH}$	-	2	mA
I_{DDs2}		$\bar{C}E = V_{DD}$ and $V_{IN} = 0V (V_{DD})$	-	100	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH}/V_{IL}$, $t_{cycle} = 150\text{ns}$	-	50	mA
I_{DDO2}		$V_{IN} = V_{DD}/0V$, $t_{cycle} = 150\text{ns}$	-	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF
C_{OUT}	Output Capacitance	$f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	-	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

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A.C. CHARACTERISTICS

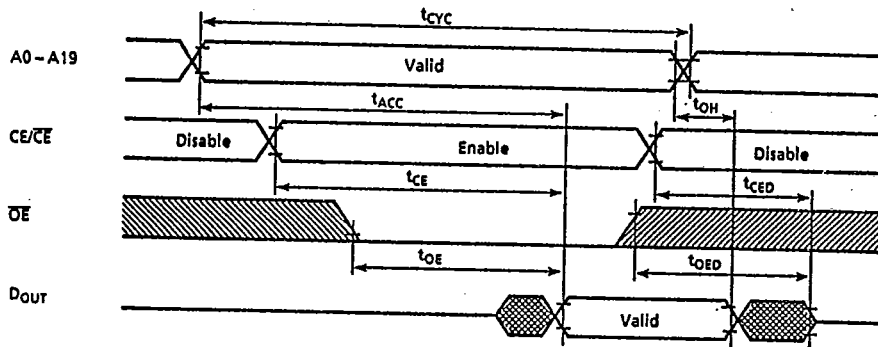
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SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	-	200	ns
t_{CE}	Chip Enable Access Time	-	200	ns
t_{OE}	Output Enable Access Time	-	70	ns
t_{CED}	Output Disable Time from \overline{CE}	0	60	ns
t_{OED}	Output Disable Time from \overline{OE}	0	60	ns
t_{OH}	Output Hold Time	5	-	ns
t_{CYC}	Cycle Time	200	-	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL
 Input Levels : 0.6V, 2.4V
 Timing Measurement Reference Levels Input : 0.8V, 2.2V
 Output : 0.8V, 2.0V
 Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	\overline{CE} (CE)	\overline{OE}	A0-A19	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: VIH L: VIL *: VIH or VIL

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TOSHIBA (LOGIC/MEMORY)

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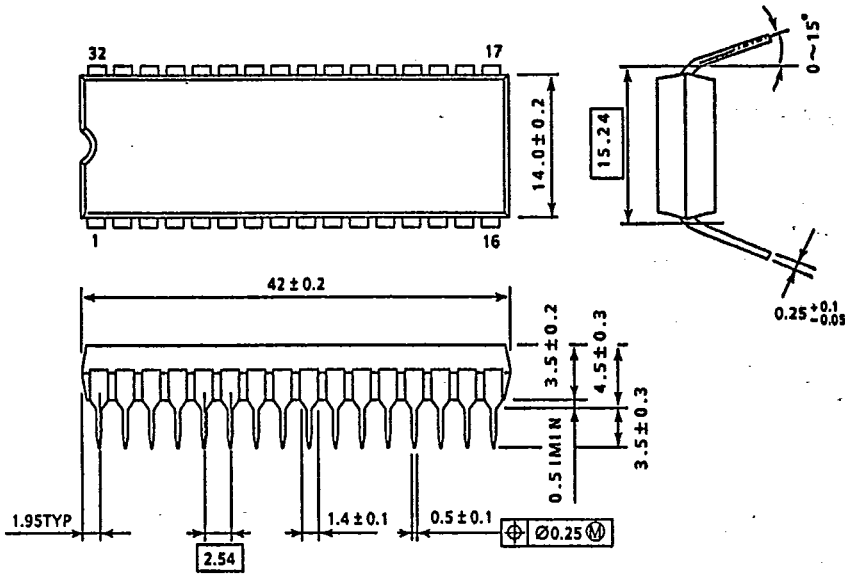
TOS2

OUTLINE DRAWINGS

Plastic DIP (DIP32-P-600)

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UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

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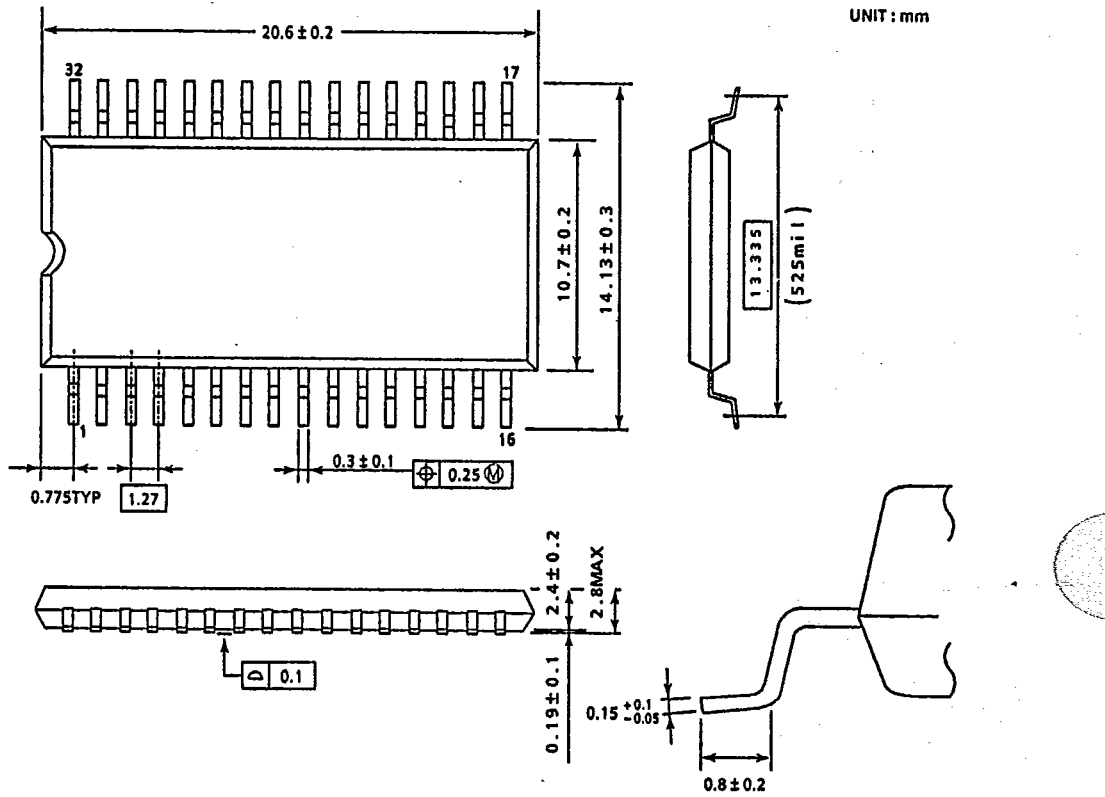
TOSHIBA (LOGIC/MEMORY)

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OUTLINE DRAWINGS
Plastic FP (SOP32 - P - 525)

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UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.