54F/74F256

Dual 4-Bit Addressable Latch

Description

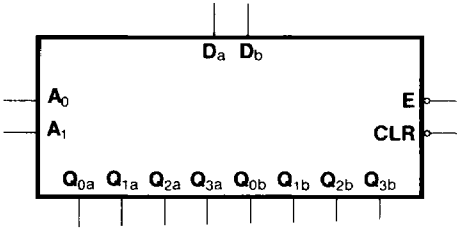
The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the demultiplexing 1-of-4 decoding or demultiplexing mode ($\overline{MR} = \overline{E} =$ LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

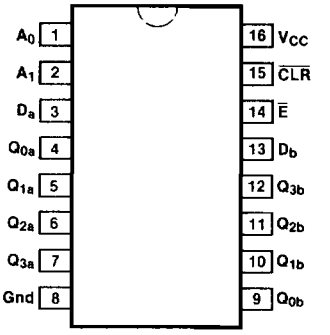
- **Combines Dual Demultiplexer and 8-Bit Latch**
- **Serial-to-Parallel Capability**
- **Output from Each Storage Bit Available**
- **Random (Addressable) Data Entry**
- **Easily Expandable**
- **Common Clear Input**
- **Useful as Dual 1-of-4 Active HIGH Decoder**

Ordering Code: See Section 5

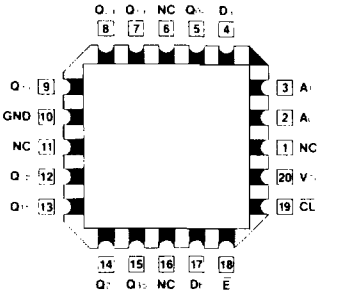
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

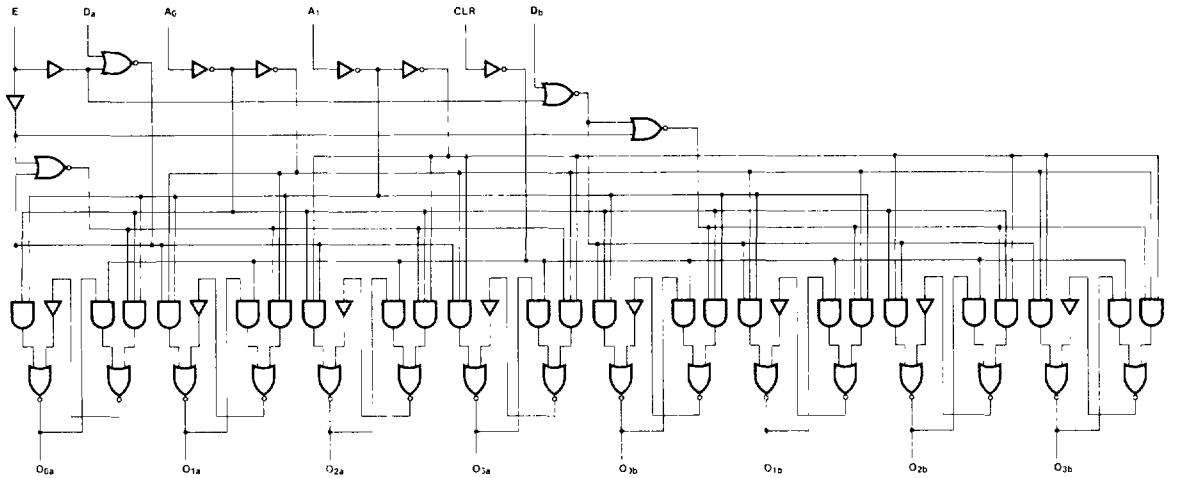
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_a, D_b	Side A, Side B Data Inputs	0.5/0.375
A_0, A_1	Address Inputs	0.5/0.375
$\overline{E}$	Enable Input	1.0/0.75
$\overline{MR}$	Master Reset	0.5/0.375
Q_{0a}-Q_{3a}	Side A Outputs	25/12.5
Q_{0b}-Q_{3b}	Side B Outputs	25/12.5

Mode Select-Function Table

Operating Mode	Inputs					Outputs			
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (Do Nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable Latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q = d

H = HIGH Voltage Level Steady State
L = LOW Voltage Level Steady State
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			40	mA	Output HIGH	V_{CC} = Max
I_{CCL}				60		Output LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		10.5 7.0						ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		9.0 7.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		14.0 9.5						ns	3-1 3-10
t_{PHL}	Propagation Delay $\overline{CLR}$ to Q_n		9.0						ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{E}$	4.0 4.0			ns	3-14
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{E}$	1.0 1.0				
$t_s(H)$ $t_s(L)$	Setup Time A to $\overline{E}$ [a]	4.0 4.0			ns	3-16
$t_h(H)$ $t_h(L)$	Hold Time A to $\overline{E}$ [b]	0 0				
$t_w(H)$ $t_w(L)$	$\overline{E}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-9

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.