

# T6A14

## TFT-LCD DATA DRIVER

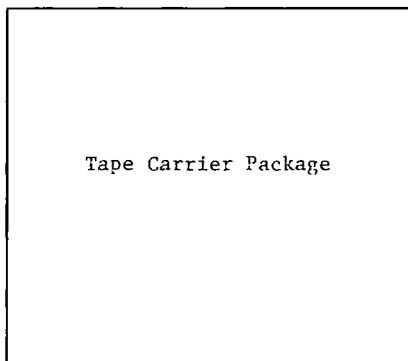
T6A14 is a Data Driver LSI for driving TFT-LCD Panel. It can drive TFT-LCD Panel without D/A converter to input gray scale data in digital.

T6A14 enables to correspond to various TFT-LCD Panel, since the offsets of the output voltages are very little to input eight gray scale voltages from external.

It is easy to drive Large TFT-LCD Panel by High Speed Operation (15MHz max.).

T6A14 realized high integration and low power consumption by using C-MOS Technology.

- . Gray Scale Data is input in Digital and is output an Analog level.
- . 12 bits (4word×3bit) Parallel transfer method.
- . Low offset of output voltage.
- . High speed operation: Transfer speed=15MHz(Max.)
- . TFT-LCD driving pins: 240 outputs (pins).
- . Low power consumption by automatic standby function.
- . It can transfer data to bidirection.
- . Two or more T6A14 can be cascaded.
- . TFT-LCD Gate Driver (T6A15) can be used with T6A14.



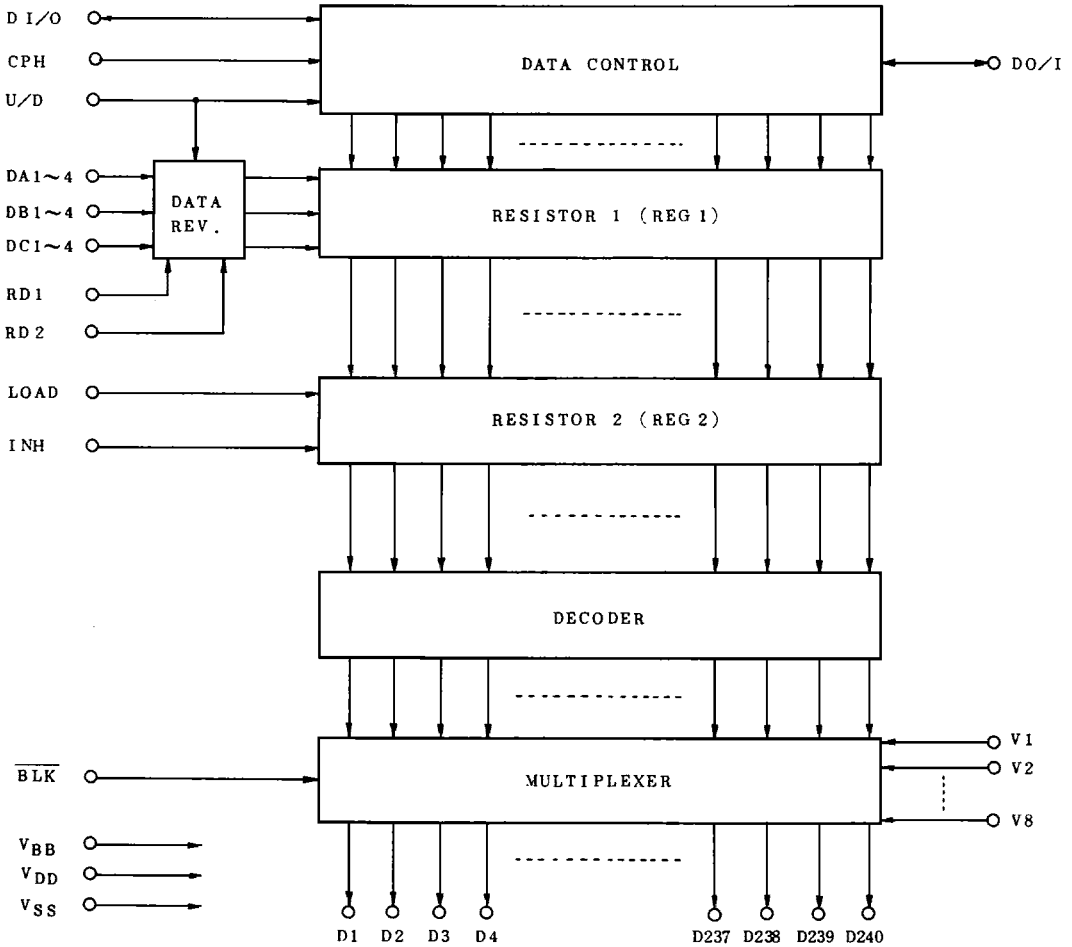
Unit : mm

T6A14	LEAD PITCH	
	IN, I/O	OUT
(JB)	0.70	0.17

\* Refer to Packaging Outline Dimensions.

. Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

BLOCK DIAGRAM





PIN DESCRIPTION

PIN NAME	I/O	FUNCTION									
DI/O DO/I	I/O	<p>DATA TRANSFER ENABLE PIN</p> <p>Case of input When this pin is input "H" level, standby mode turn to data transfer mode.</p> <p>Case of output This pin turns the next LSI to data transfer mode in case of cascade connection.</p> <p>It changes as follows according to U/D pin:</p> <table border="1" data-bbox="442 666 815 782"> <thead> <tr> <th>U/D</th> <th>DI/O</th> <th>DO/I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>INPUT</td> <td>OUTPUT</td> </tr> <tr> <td>L</td> <td>OUTPUT</td> <td>INPUT</td> </tr> </tbody> </table>	U/D	DI/O	DO/I	H	INPUT	OUTPUT	L	OUTPUT	INPUT
U/D	DI/O	DO/I									
H	INPUT	OUTPUT									
L	OUTPUT	INPUT									
U/D	I	<p>Transfer Direction Select Pin</p> <p>This pin defines direction to transfer Gray Scale Data.</p> <p>Data transfer as shown below synchronously to the rise of CPH.</p> <p>U/D="H" level : D1~4, D5~8, D9~12 ...</p> <p>U/D="L" level : D240~237, D236~233 ...</p> <p>It must be used "H" or "L" level in DC level.</p>									
CPH	I	<p>Data Transfer Clock Pin</p> <p>This pin is a clock to transfer Gray Scale Data.</p> <p>(1) These pins are written into LSI synchronously to the rise of CPH.</p> <ul style="list-style-type: none"> <li>. DI/O, DO/I (input)</li> <li>. DA1~4, DB1~4, DC1~4</li> <li>. RD1, RD2</li> </ul> <p>(2) These pins output synchronously to the rise of CPH.</p> <ul style="list-style-type: none"> <li>. DI/O, DO/I (Output)</li> </ul>									

PIN NAME	I/O	FUNCTION
DA1~4 DB1~4 DC1~4	I	Gray Scale Data Bus These pins are bus to transfer Gray Scale Data, which transfer the data to REG1 synchronously to the rise of CPH. 1 word=3 bits: they transfer data of 4 words at once. Mean of bits is as follows. $\text{Gray Scale Data} = 4 \times \text{DCn} + 2 \times \text{DBn} + \text{DAn} \quad *n=1\sim 4$
RD1 RD2	I	Gray Scale Data Mirror Image Control Pin When TFT-LCD Panel is driving, these pins enable to reverse output voltages (V1~V8) without changing data. RD1, RD2 and Gray Scale Data operate as shown. DAn : RD1 Ex-or DAn DBn : RD1 Ex-or DBn DCn : RD1 Ex-or RD2 Ex-or DCn $*n=1\sim 4$ This result of operation is kept in REG1.
LOAD	I	Data Load Input Pin When this pin is "H" level, the data of REG1 transfer to REG2. It can change the voltages of TFT-LCD panel driving pins (D1~D240).
INH	I	Data Clear Input Pin This pin turns all data of REG2 to "L" level. All TFT-LCD panel driving pins (D1~D240) output the voltage of V1.
$\overline{\text{BLK}}$	I	Blanking Input Pin This pin turns TFT-LCD panel driving pins (D1~D240) to High-Impedance.
V1~V8	I	Analog Input Pins These pins input the voltage which output to TFT-LCD Panel driving pins (D1~D240). There are each two pins from V1 to V8, and same voltage must be input.

PIN NAME	I/O	FUNCTION																		
D1~D240	O	<p>TFT-LCD Panel Driving Pin</p> <p>These pins output one of Analog Input Voltages (V1~V8) by Gray Scale Data. The gray scale data is the data of REG2.</p> <table border="1" data-bbox="443 447 978 786"> <thead> <tr> <th data-bbox="443 447 709 487">Gray Scale Data</th> <th data-bbox="709 447 978 487">Output Level</th> </tr> </thead> <tbody> <tr> <td data-bbox="443 487 709 527">0</td> <td data-bbox="709 487 978 527">V1</td> </tr> <tr> <td data-bbox="443 527 709 567">1</td> <td data-bbox="709 527 978 567">V2</td> </tr> <tr> <td data-bbox="443 567 709 607">2</td> <td data-bbox="709 567 978 607">V3</td> </tr> <tr> <td data-bbox="443 607 709 647">3</td> <td data-bbox="709 607 978 647">V4</td> </tr> <tr> <td data-bbox="443 647 709 687">4</td> <td data-bbox="709 647 978 687">V5</td> </tr> <tr> <td data-bbox="443 687 709 727">5</td> <td data-bbox="709 687 978 727">V6</td> </tr> <tr> <td data-bbox="443 727 709 767">6</td> <td data-bbox="709 727 978 767">V7</td> </tr> <tr> <td data-bbox="443 767 709 786">7</td> <td data-bbox="709 767 978 786">V8</td> </tr> </tbody> </table> <p>Note) All these pins are High-Impedance mode when <math>\overline{\text{BLK}}</math> pin is "L" level.</p>	Gray Scale Data	Output Level	0	V1	1	V2	2	V3	3	V4	4	V5	5	V6	6	V7	7	V8
Gray Scale Data	Output Level																			
0	V1																			
1	V2																			
2	V3																			
3	V4																			
4	V5																			
5	V6																			
6	V7																			
7	V8																			
TST1 TST2 TST3	I	<p>Test Pin</p> <p>These pins must be open.</p>																		
V <sub>BB</sub>		<p>Power Supply Voltage</p> <p>It is a power supply pin of high voltage. These are two V<sub>BB</sub> pins, and same voltage must be input.</p>																		
V <sub>DD</sub>		<p>Power Supply Voltage</p> <p>It is a logical power supply pin of LSI.</p>																		
V <sub>SS</sub>		<p>GND Pin</p> <p>It is a ground of LSI. There are three V<sub>SS</sub> pins, and same voltage must be input.</p>																		

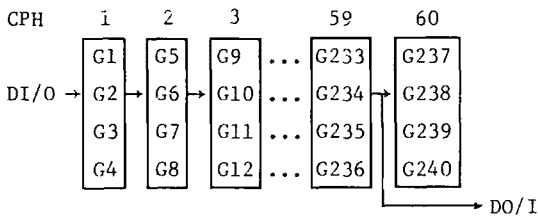
## FUNCTIONAL DESCRIPTION

### . DATA TRANSFER

When DI/O or DO/I(case of input) is input "H" level(\*1) synchronously to the rise of CPH, the standby mode turns to the transfer mode. It starts to transfer the data to REG1 rising of the next CPH.

The data of REG1 is the result which the data of the gray scale data bus(\*2) is operated by RD1 and RD2(\*3). It finishes to transfer the data when the data is input 60 times. And then the data transfer mode turns to the standby mode.

ex. CASE OF UP MODE(cf. Fig.1-TIMING CHART)



DI/O or DO/I(case of output) outputs "H" level synchronously to the rise of CPH.

In case of cascade connection:

UP MODE ..... DO/I(output) connects to DI/O(input).

DOWN MODE ... DI/O(output) connects to DO/I(input).

This pin turns the next LSI to the data transfer mode.

\*1 When user input "H" level, keep "L" level until finish to transfer the data.

\*2 4 words×3 bits

\*3 cf. RD1 and RD2

### . RD1 and RD2

These pins enable to reverse output voltages without changing the data of the gray scale data bus. Don't change these pins during transfer data.

These pins operate the data of gray scale data bus as shown.

DAn=RD1 Ex-or DAN

DBn=RD1 Ex-or DBn

DCn=RD1 Ex-or RD2 Ex-or DCn \*n=1~4

As a result, gray scale data is as follows:

$4 \times (\text{RD1 Ex-or RD2 Ex-or DCn}) + 2 \times (\text{RD1 Ex-or DBn}) + (\text{RD1 Ex-or DAN})$

When LOAD(\*4) is input "H" level, gray scale data of REG1 is transferred to REG2. The data decides analog input voltages (V1-V8) as shown.

Gray Scale Data	RD1="L",RD2="L"	RD1="H",RD2="L"	RD1="L",RD2="H"	RD1="H",RD2="H"
0	V1	V8	V5	V4
1	V2	V7	V6	V3
2	V3	V6	V7	V2
3	V4	V5	V8	V1
4	V5	V4	V1	V8
5	V6	V3	V2	V7
6	V7	V2	V3	V6
7	V8	V1	V4	V5

V1-V8=Output voltage

TFT-LCD Panel driving pins (D1-D240) output analog input voltages (V1-V8) corresponding to the gray scale data.

. LOAD(\*4)

LOAD="H" level : transfers gray scale data from REG1 to REG2.

. INH

INH="H" level : turns gray scale data of REG2 to "L" level. TFT-LCD driving pins output the voltage of V1.

.  $\overline{\text{BLK}}$

$\overline{\text{BLK}}$ ="L" level : turns TFT-LCD driving pins to High-Impedance mode.

Input this before and after inputting LOAD="H" level or INH="H" level.

(cf. Fig.1-TIMING CHART)

# T6A14

## TIMING CHART

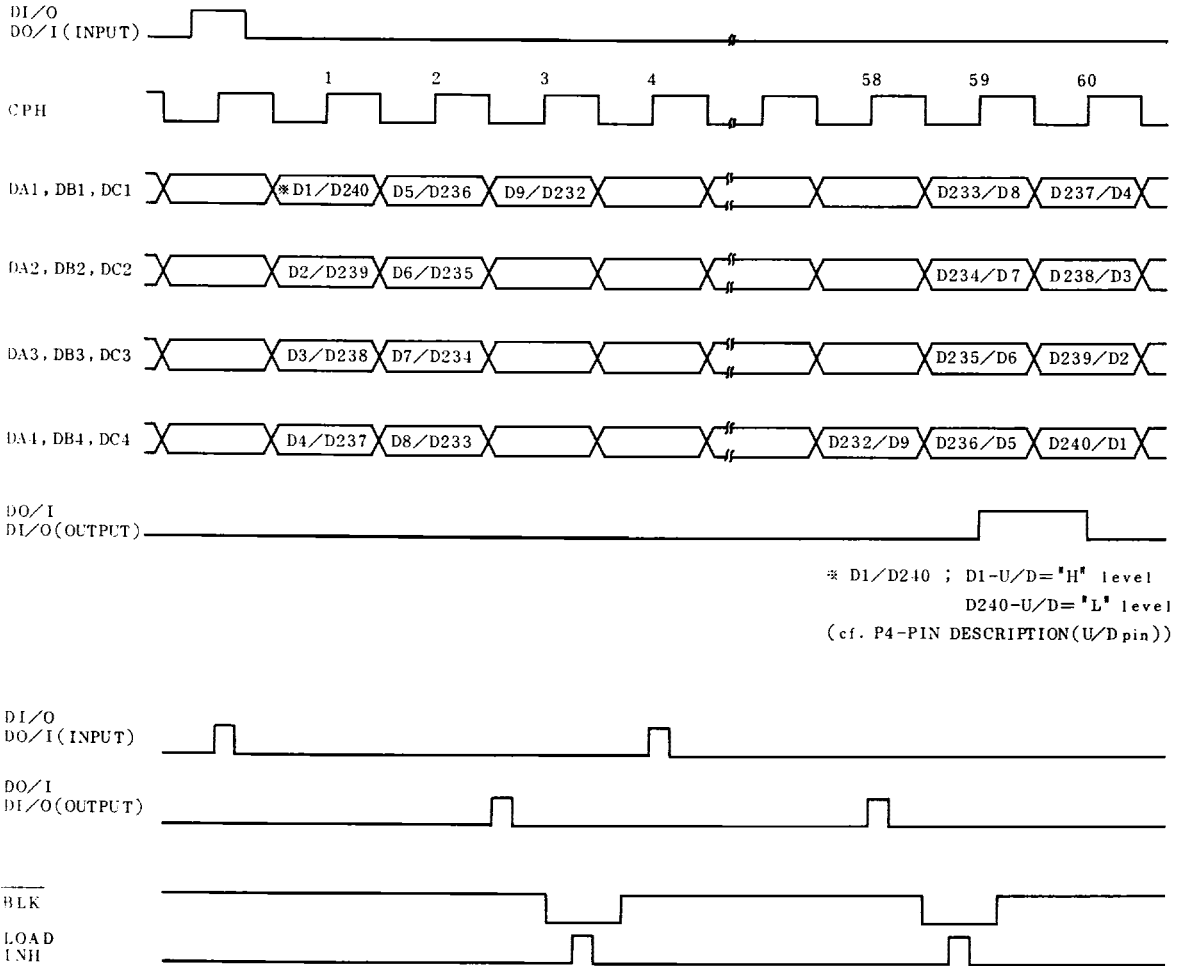


Fig. 1

MAXIMUM RATINGS ( $V_{SS}=0V$ )

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Supply Voltage 1	VDD		-0.3~7.0	V	
Supply Voltage 2	VBB		-0.3~16	V	
Input Voltage	VIN		-0.3~VDD+0.3	V	
Analog Input Voltage	VIX		-0.3~VBB+0.3	V	V1~8
Storage Temperature	Tstg		-55~125	°C	

## ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITION ( $V_{SS}=0V$ )

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Operating Voltage 1	VDD		4.5~5.5	V	
Operating Voltage 2	VBB		VDD~14	V	
Operating Temperature	TOP		-20~75	°C	
Operating Frequency	f <sub>CPH</sub>		DC~15	MHz	CPH
"LOAD" Input Cycle	t <sub>LOAD</sub>		20(MIN)	μs	LOAD
Output Load Capacitance	C <sub>L</sub>		300(MAX)	PF/PIN	D1~240
Analog Input Voltage	VIX		0~VBB	V	V1~8

## DC CHARACTERISTICS

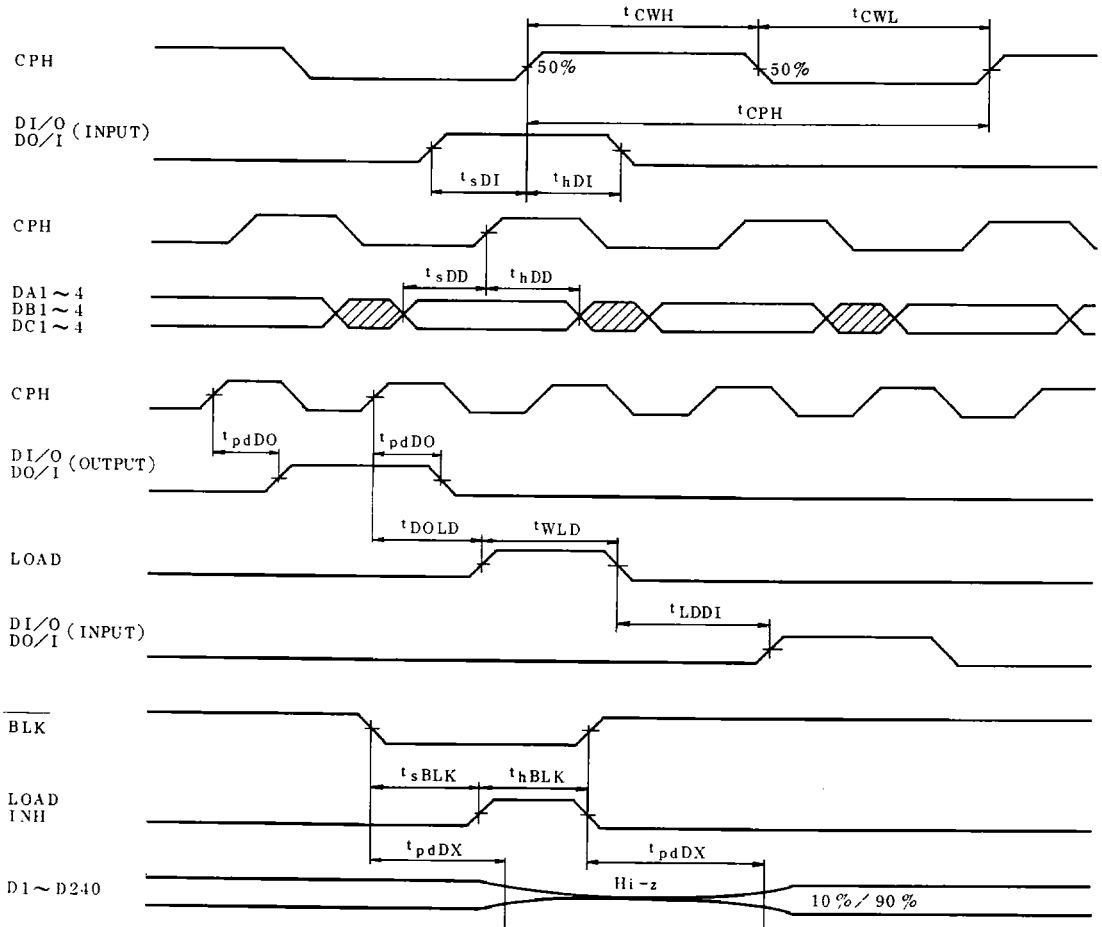
(Unless otherwise specified, VDD=5V±10%, VBB=12V±2V, VSS=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	APPLY PIN
Input "L" Level	VIL		0	0.3×VDD	V	Logic Input
Input "H" Level	VIH		0.7×VDD	VDD	V	Logic Input
Output "L" Level	VOL	IOL=0.6mA	VSS	VSS+0.3	V	Logic Output
Output "H" Level	VOH	IOH=-0.6mA	VDD-0.3	VDD	V	Logic Output
Output Resistance	ROD		-	4.5	kΩ	D1~D240
	ΔROD	*1	-	±500	Ω	D1~D240
Input Leak Current	IIN		-1.0	1.0	μA	Logic Input D1~D240
	IOZ		-5.0	5.0	μA	DI/O, DO/I
	IXL	BLK="L" level	-50	50	μA	V1~V8
Standby Current	ISTB	f <sub>CPH</sub> =DC	-	0.1	mA	VDD
Current Consumption 1	IDD	f <sub>CPH</sub> =15MHz	-	15.0	mA	VDD
Current Consumption 2	IBB	t <sub>LOAD</sub> =20μs	-	1.0	mA	VBB

\*1 In case of selecting same Analog Input (V1~8), it is the difference of resistance in a chip.

# T6A14

## AC CHARACTERISTICS



(Unless otherwise specified,  $V_{DD}=5V\pm 10\%$ ,  $V_{BB}=12V\pm 2V$ ,  $V_{SS}=0V$ ,  $T_a=-20\sim 75^\circ C$ )

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Operating Frequency	$t_{CPH}$		67	-	ns
CPH Pulse Width "H"	$t_{CWH}$		25	-	ns
CPH Pulse Width "L"	$t_{CWL}$		25	-	ns
Data Input Time	$t_{LDDI}$		20	-	ns
Data Set Up Time	$t_{sDI}$		15	-	ns
Data Hold Time	$t_{hDI}$		20	-	ns
Data Set Up Time	$t_{sDD}$		15	-	ns
Data Hold Time	$t_{hDD}$		15	-	ns
Load Input Time	$t_{DOLD}$		20	-	ns
Load Input Width	$t_{WLD}$		20	-	ns
Blanking Set Up Time	$t_{sBLK}$		500	-	ns
Blanking Cancel Time	$t_{hBLK}$		500	-	ns
Output Delay Time 1	$t_{pdDO}$	$C_L=30pF$	-	35	ns
Output Delay Time 2	$t_{pdDX}$	$C_L=0pF$	-	1	$\mu s$

Conditions : Rising and falling time=6ns