4Mx4 Dynamic RAM CMOS, Multichip Microcircuit

The EDI4M44096C is a high performance, low power CMOS Dynamic RAM Multichip Microcircuit organized as 4 Megabits x4. This device is based on four megabit density DRAMs in a Quad Cavity Ceramic Substrate. The IC devices used employ triple-layer polysilicon process combined with silicide technology and a single transistor dynamic storage cell, to provide high circuit density with high performance. The use of dynamic circuitry, including sense amplifiers, assures low power dissipation.

Multiplexed address inputs permit a low pin count for maximum system density.

In addition to the RAS\-only refresh mode, the hidden refresh mode and CAS\ before RAS\ refresh mode are available.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Features

4Mx4 bit CMOS Dynamic
Random Access Memory Multichip Microcircuit

- Access Times 80 and 100ns
- Low Operating Power Dissipation
- Low Standby Power
- All Inputs/Outputs TTL Compatible

High Density Package

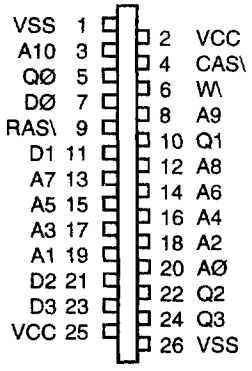
- 26 pin Quad Cavity Ceramic ZIP, No. 34

Single +5V (±10%) Supply Operation

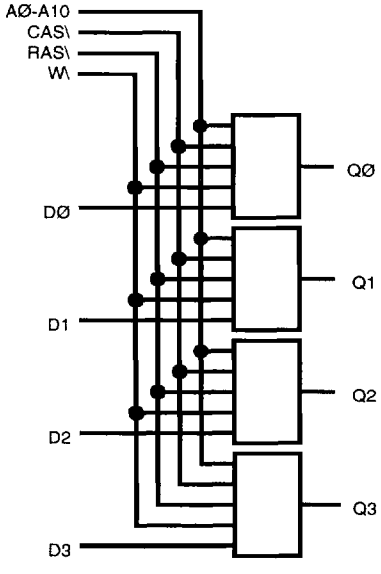
Pin Names

AØ-A10	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
DØ-D3	Data Inputs
QØ-Q3	Data Outputs
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pin Configuration and Block Diagram



TOP VIEW



Ordering Information

Part No.	Speed (ns)	Package No.	Temp. Range
EDI4M44096C80ZM	80	34	Military
EDI4M44096C100ZM	100	34	Military

Package Description

Package No. 34
26 pin Quad Cavity
Sidebrazed
Ceramic ZIP