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FUJITSU

DATA SHEET

MB98A6081x-/6091x-/6101x-/6111x-25 OTPROM MEMORY CARD

ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD 256K / 512K / 1M / 2M-BYTE

The Fujitsu MB98A6081x. MB98A6091x, MB98A6101x and MB98A6111x are One Time Programmable Read Only Memory (OTPROM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and one at the bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card Internal Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, OTPROM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is an OTPROM memory card option. (See page 2 for description of the three available options.)

CRD-68P-M02

- PCMCIA and JEIDA industry standard for 68-pin memory card
- Credit card size dimensions: 85.6mm (length) x 54.0mm (width) x 3.3mm (thick)
- PCMCIA / JEIDA industry standard, two-piece 68-pin connector (with a built-in two-row receptacle)
- Single +5V power supply
- Static operation: No clock required
- TTL compatible inputs and outputs

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	–0.5 to +7.0	V
Input Voltage	VIN	–0.5 to VCC +0.5	V
Output Voltage	VOUT	–0.5 to VCC +0.5	V
Programming Voltage	VPP1, VPP2	–0.5 to +13.5	V
Temperature under Bias	TBIAS	–10 to +60	°C
Storage Temperature	TSTG	–30 to +70	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{\text{REG}}$ pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported. $\overline{\text{REG}}$ Pin : Not Contacted

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A60811	MBM27C1001P x 2pcs	250 ns	N / A	N / A	256K x 8 bits/ 128K x 16 bits
MB98A60911	MBM27C1001P x 4pcs	250 ns	N / A	N / A	512K x 8 bits/ 256K x 16 bits
MB98A61011	MBM27C1001P x 8pcs	250 ns	N / A	N / A	1M x 8 bits/ 512K x 16 bits
MB98A61111	MBM27C1001P x 16pcs	250 ns	N / A	N / A	2M x 8 bits/ 1M x 16 bits

OPTION 2: Attribute memory in a separate location is not supported.

When $\overline{\text{REG}}$ line is asserted, ”FF” is output to the data bus to indicate that attribute data may be stored in main memory.

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A60812	MBM27C1001P x 2pcs	250 ns	N / A	N / A	256K x 8 bits/ 128K x 16 bits
MB98A60912	MBM27C1001P x 4pcs	250 ns	N / A	N / A	512K x 8 bits/ 256K x 16 bits
MB98A61012	MBM27C1001P x 8pcs	250 ns	N / A	N / A	1M x 8 bits/ 512K x 16 bits
MB98A61112	MBM27C1001P x 16pcs	250 ns	N / A	N / A	2M x 8 bits/ 1M x 16 bits

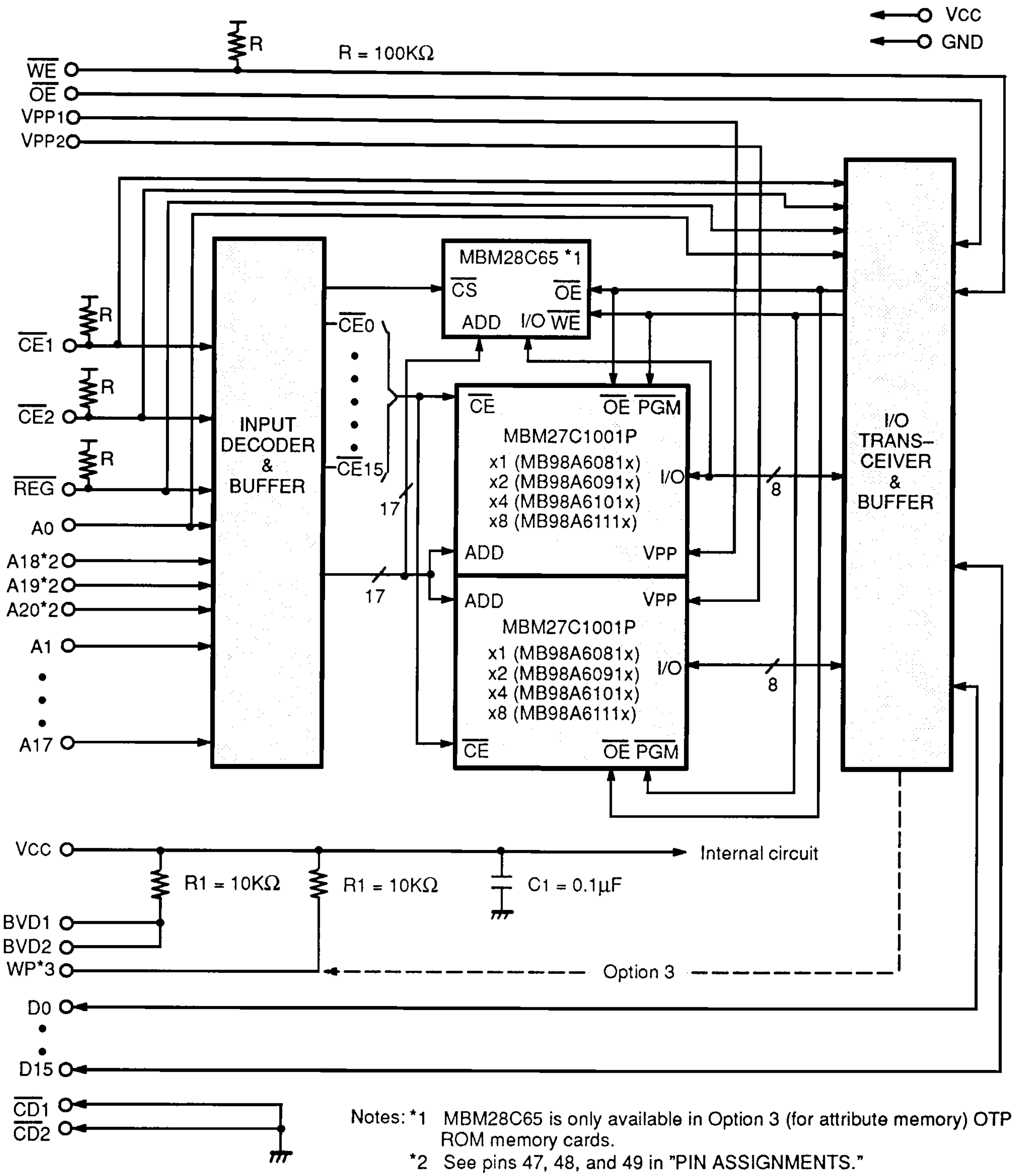
OPTION 3: Attribute memory is supported. The data is stored in an 8K-bit EEPROM.

When the $\overline{\text{REG}}$ line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organizaiton *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A60813	MBM27C1001P x 2pcs	250 ns	MBM28C65 x 1pc	300 ns	256K x 8 bits/ 128K x 16 bits
MB98A60913	MBM27C1001P x 4pcs	250 ns	MBM28C65 x 1pc	300 ns	512K x 8 bits/ 256K x 16 bits
MB98A61013	MBM27C1001P x 8pcs	250 ns	MBM28C65 x 1pc	300 ns	1M x 8 bits/ 512K x 16 bits
MB98A61113	MBM27C1001P x 16pcs	250 ns	MBM28C65 x 1pc	300 ns	2M x 8 bits/ 1M x 16 bits

Note: * To be configured by user.

Fig. 1 – MB98A6081x, 6091x, 6101x, and 6111x BLOCK DIAGRAM



Notes: *1 MBM28C65 is only available in Option 3 (for attribute memory) OTP ROM memory cards.
*2 See pins 47, 48, and 49 in "PIN ASSIGNMENTS."
*3 WP outputs low level in Option 3.

PIN ASSIGNMENTS

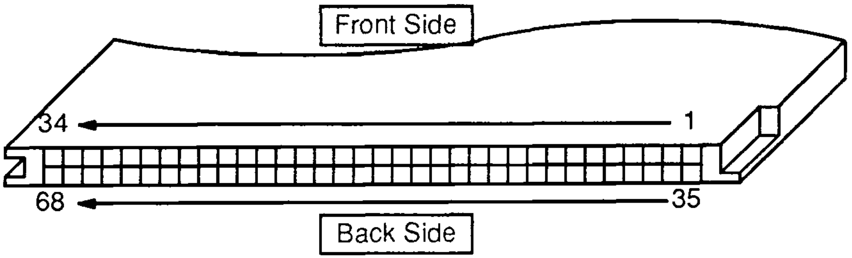
MB98A6081x	MB98A6091x	MB98A6101x	MB98A61111x	Pin No.		MB98A6081x	MB98A6091x	MB98A6101x	MB98A61111x
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{\mathrm{CD}}1$	$\overline{\mathrm{CD}}1$	$\overline{\mathrm{CD}}1$	$\overline{\mathrm{CD}}1$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{\mathrm{CE}}1$	$\overline{\mathrm{CE}}1$	$\overline{\mathrm{CE}}1$	$\overline{\mathrm{CE}}1$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{\mathrm{CE}}2$	$\overline{\mathrm{CE}}2$	$\overline{\mathrm{CE}}2$	$\overline{\mathrm{CE}}2$
$\overline{\mathrm{OE}}$	$\overline{\mathrm{OE}}$	$\overline{\mathrm{OE}}$	$\overline{\mathrm{OE}}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	A17	A17	A17	A17
A13	A13	A13	A13	13	47	NC	A18	A18	A18
A14	A14	A14	A14	14	48	NC	NC	A19	A19
$\overline{\mathrm{PGM}}$	$\overline{\mathrm{PGM}}$	$\overline{\mathrm{PGM}}$	$\overline{\mathrm{PGM}}$	15	49	NC	NC	NC	A20
NC	NC	NC	NC	16	50	NC	NC	NC	NC
VCC	VCC	VCC	VCC	17	51	VCC	VCC	VCC	VCC
VPP1	VPP1	VPP1	VPP1	18	52	VPP2	VPP2	VPP2	VPP2
A16	A16	A16	A16	19	53	NC	NC	NC	NC
A15	A15	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	$\overline{\mathrm{REG}}$	$\overline{\mathrm{REG}}$	$\overline{\mathrm{REG}}$	$\overline{\mathrm{REG}}$
A1	A1	A1	A1	28	62	BVD2	BVD2	BVD2	BVD2
A0	A0	A0	A0	29	63	BVD1	BVD1	BVD1	BVD1
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{\mathrm{CD}}2$	$\overline{\mathrm{CD}}2$	$\overline{\mathrm{CD}}2$	$\overline{\mathrm{CD}}2$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A20	Address Input	Input	Address Inputs, A0–A20.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. The data bus size (8-bit or 16-bit) selected with $\overline{CE}1$ and $\overline{CE}2$.
$\overline{CE}1$	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function of OTPROM cards.
$\overline{CE}2$	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function of OTPROM cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for read/write function of identification data of OTPROM cards. (NC or "FF" data or attribute data.)
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for OTPROM cards.
$\overline{PGM}$	Programming Enable	Input	Active Low. –Write enable for OTPROM cards.
VPP1	Programming Voltage 1	Input	Active VPP –Programming voltage for lower byte.
VPP2	Programming Voltage 2	Input	Active VPP –Programming voltage for upper byte.
$\overline{CD}1$, $\overline{CD}2$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	This pin outputs high level in Option 1 and 2, and outputs low level in Option 3.
BVD1, BVD2	Battery Voltage Detect	Output	Both pins are tied to VCC internally.
VCC	Power Supply	–	Power Supply Voltage. (+5.0V ±5%)
GND	Ground	–	System Ground.
NC	No Connection	–	

PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



FUNCTION TRUTH TABLE

MAIN MEMORY FUNCTION *1 ($\overline{\text{REG}}=V_{IH}$)

$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	A0 (Byte)	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	VPP2	VPP1	VCC	Mode	Data Input/Output	
									D15–D8	D7–D0
H	H	X	X	X	+5V	+5V	+5V	Standby	High–Z	
H	L	L	L	H	+5V	+5V	+5V	Read (x8)	High–Z	DOUT (Lower Byte)
H	L	H	L	H	+5V	+5V	+5V	Read (x8)	High–Z	DOUT (Upper Byte)
H	L	L	H	L	+6V *2	+12.5V	+6V	Write (x8)	High–Z	DIN (Lower Byte)
H	L	H	H	L	+12.5V	+6V *2	+6V	Write (x8)	High–Z	DIN (Upper Byte)
L	H	L	L	H	+5V	+5V	+5V	Read (x8)	DOUT (Upper Byte)	High–Z
L	H	H	H	L	+12.5V	+6V *2	+6V	Write (x8)	DIN (Upper Byte)	High–Z
L	L	L	L	H	+5V	+5V	+5V	Read (x16)	DOUT	
L	L	H	H	L	+12.5V	+12.5V	+6V	Write (x16)	DIN	
X	X	H	H	H	+5V	+5V	+5V	Output Disable	High–Z	

ATTRIBUTE MEMORY FUNCTION *1 ($\overline{\text{REG}}=V_{IL}$) *3

$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	A0 (Byte)	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	VPP2	VPP1	Mode	Data Input/Output	
								D15–D8	D7–D0
H	H	X	X	X	+5V	+5V	Standby	High–Z	
H	L	L	L	H	+5V	+5V	Read (x8)	High–Z	DOUT *4 (Lower Byte)
H	L	H	L	H	+5V	+5V	Read (x8)	High–Z	H
H	L	L	H	L	+5V	+5V	Write (x8)	High–Z	DIN (Lower Byte)
H	L	H	H	L	+5V	+5V	Write (x8)	High–Z	X
L	H	X	L	H	+5V	+5V	Read (x8)	H	High–Z
L	H	X	H	L	+5V	+5V	Write (x8)	X	High–Z
L	L	X	L	H	+5V	+5V	Read (x16)	H	DOUT *4 (Lower Byte)
L	L	X	H	L	+5V	+5V	Write (x16)	X	DIN (Lower Byte)
X	X	X	H	H	+5V	+5V	Output Disable	High–Z	

Notes: *1 H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}
*2 +6V is recommended though it is functionable at 12.5V.
*3 NC for MB98A60811, 60911, 61011, and 61111.
*4 H-level is output for MB98A60812, 60912, 61012, and 61112.

ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

8-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIL, $\overline{CE2}$ = VIH)

A20 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
0 0000 0000 0000 0000 0000	H	L	-----	0 Add.
0 0000 0000 0000 0000 0001	H	L	-----	1 Add.
0 0000 0000 0000 0000 0010	H	L	-----	2 Add.
0 0000 0000 0000 0000 0011	H	L	-----	3 Add.
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 1111 1100	H	L	-----	2,097,148 Add.
1 1111 1111 1111 1111 1101	H	L	-----	2,097,149 Add.
1 1111 1111 1111 1111 1110	H	L	-----	2,097,150 Add.
1 1111 1111 1111 1111 1111	H	L	-----	2,097,151 Add.

8-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIH, $\overline{CE2}$ = VIL) *2

A20 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
0 0000 0000 0000 0000 000X	L	H	1 Add.	-----
0 0000 0000 0000 0000 001X	L	H	3 Add.	-----
0 0000 0000 0000 0000 010X	L	H	5 Add.	-----
0 0000 0000 0000 0000 011X	L	H	7 Add.	-----
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 1111 100X	L	H	2,097,145 Add.	-----
1 1111 1111 1111 1111 101X	L	H	2,097,147 Add.	-----
1 1111 1111 1111 1111 110X	L	H	2,097,149 Add.	-----
1 1111 1111 1111 1111 111X	L	H	2,097,151 Add.	-----

16-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIL, $\overline{CE2}$ = VIL)

A20 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
0 0000 0000 0000 0000 000X	L	L	1 Add.	0 Add.
0 0000 0000 0000 0000 001X	L	L	3 Add.	2 Add.
0 0000 0000 0000 0000 010X	L	L	5 Add.	4 Add.
0 0000 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 1111 100X	L	L	2,097,145 Add.	2.097,144 Add.
1 1111 1111 1111 1111 101X	L	L	2,097,147 Add.	2,097,146 Add.
1 1111 1111 1111 1111 110X	L	L	2,097,149 Add.	2,097,148 Add.
1 1111 1111 1111 1111 111X	L	L	2,097,151 Add.	2,097,150 Add.

Notes: *1 H = VIH, L = VIL, X = Either 0 or 1.
*2 Even addresses are not available in this mode.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	V
Programming Voltage during Read Mode	VPP	VCC–0.6	VCC	VCC+0.6	V
Ground	GND		0		V
Input High Voltage	VIH	2.4		VCC+0.3	V
Input Low Voltage	VIL	–0.1		0.8	V
Ambient Temperature	TA	0		55	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Standby Supply Current	$\overline{CE}$1, $\overline{CE}$2 ≥ VCC –0.2V	ISB1			100	µA
	$\overline{CE}$1, $\overline{CE}$2 = VIH	ISB2			10	mA
Active Supply Current	VIN = VIH or VIL $\overline{CE}$1, $\overline{CE}$2 = VIL, IOUT = 0mA	ICC1			100	mA
Operating Supply Current	VIN = VIH or VIL, Cycle = Min. Duty = 100%, IOUT = 0mA	ICC2			100	mA
Input Leakage Current *1	VIN = 0V to VCC	ILI	–10		10	µA
Output Leakage Current *2	VOUT = 0V to VCC, $\overline{CE}$1, $\overline{CE}$2=VIH or $\overline{OE}$ = VIH or $\overline{PGM}$ = VIL	ILI/O	–10		10	µA
Output High Voltage *3	IOH = –1.0mA	VOH	2.4			V
Output Low Voltage *4	IOL = 2.1mA	VOL			0.4	V

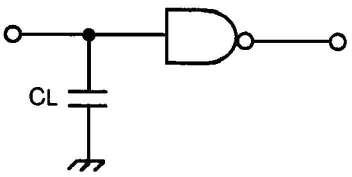
Notes: *1 This value does not apply to $\overline{CE}$1, $\overline{CE}$2, $\overline{REG}$ and $\overline{PGM}$.
*2 This value does not apply to BVD1, BVD2, $\overline{CD}$1, $\overline{CD}$2 and WP.
*3 This value does not apply to BVD1 and BVD2.
*4 This value does not apply to $\overline{CD}$1 and $\overline{CD}$2.

CAPACITANCE (TA=25°C, f=1MHz, VIN=VI/O=GND)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance *1	CIN			50	pF
I/O Capacitance *2	COUT			50	pF

Notes: *1 This value does not apply to VPP1, VPP2, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ and $\overline{PGM}$.
*2 This value does not apply to BVD1, BVD2, $\overline{CD}$1, $\overline{CD}$2 and WP.

Fig. 3 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.6V
- Input Pulse Rise and Fall Times: 5ns
  (Transition between 0.8V and 2.4V)
- Timing Reference Levels
  Input: VIL = 0.8V, VIH = 2.4V
  Output: VOL = 0.8V, VOH = 2.0V
- Output Load: 1TTL gate + CL (100pF)

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRC	250		ns
Address Access Time	tAA		250	ns
Card Enable Access Time	tCE		250	ns
Output Enable Access Time	tOE		120	ns
Output Disable Time *1	tDF		100	ns
Output Hold Time	tOH	0		ns

ATTRIBUTE MEMORY READ CYCLE *2

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRRC	300		ns
Address Access Time	tRAA		300	ns
Card Enable Access Time	tRCE		300	ns
Output Enable Access Time	tROE		120	ns
Output Disable Time *1	tRDF		100	ns
Output Hold Time	tROH	0		ns

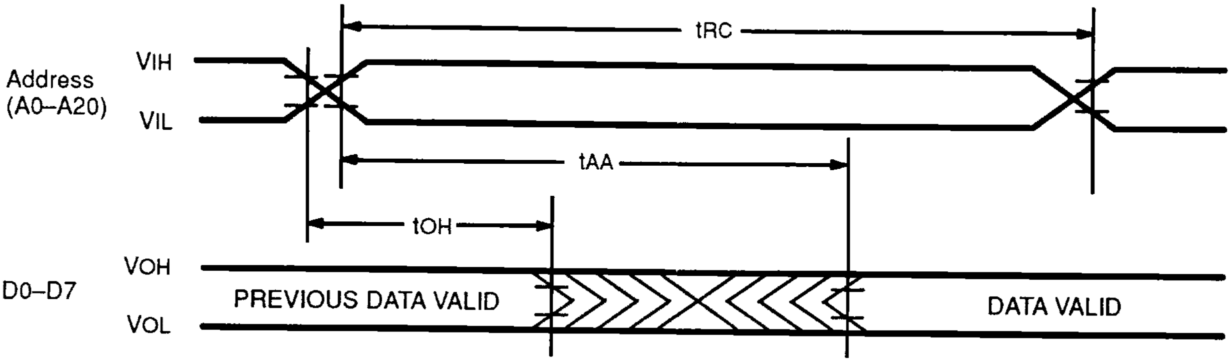
Notes: *1 tDF is specified from the rising edge of $\overline{OE}$, $\overline{CE}1$ and $\overline{CE}2$, whichever occurs first. tDF is defined as the point where data is no longer driven.
*2 This parameter is for MB98A60813, 60913, 61013, and 61113.

AC CHARACTERISTICS (Continued)

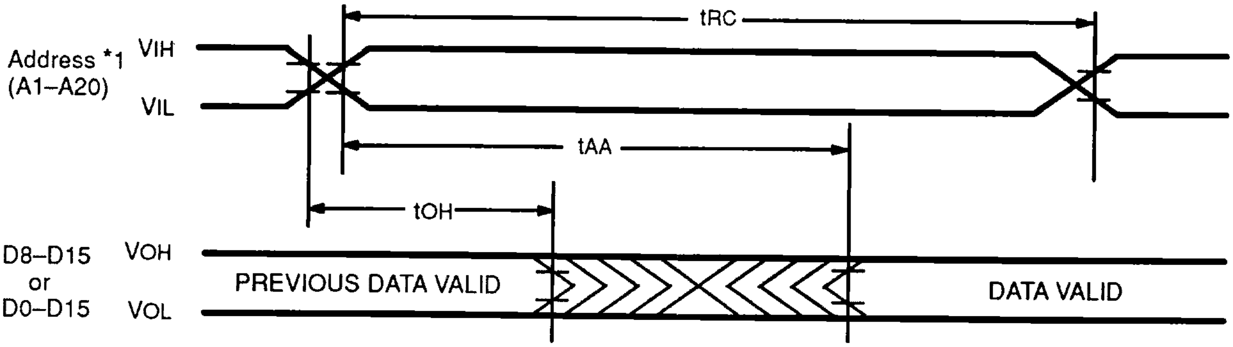
(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{PGM}$ = VIH, $\overline{REG}$ = VIH)

READ CYCLE 1: $\overline{CE}1$ = $\overline{OE}$ = VIL, $\overline{CE}2$ = VIH : x 8–bit Bus Organization



READ CYCLE 2: $\overline{CE}1$ = VIH, $\overline{CE}2$ = $\overline{OE}$ = VIL: x 8–bit Bus Organization
$\overline{CE}1$ = $\overline{CE}2$ = $\overline{OE}$ = VIL: x 16–bit Bus Organization



▨ :Undefined

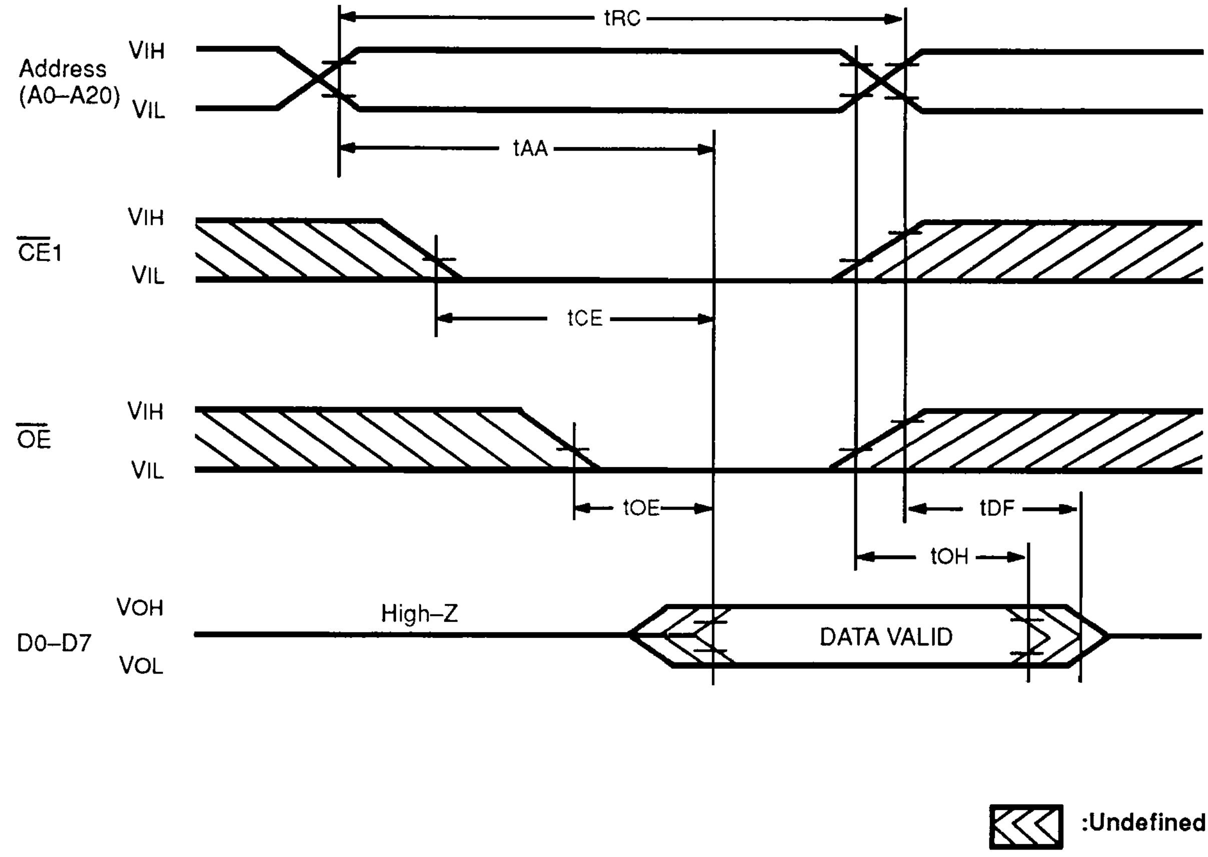
Note: *1 A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{\text{PGM}}$ = VIH, $\overline{\text{REG}}$ = VIH)

READ CYCLE 3: $\overline{\text{CE}}$2 = VIH: x 8–bit Bus Organization

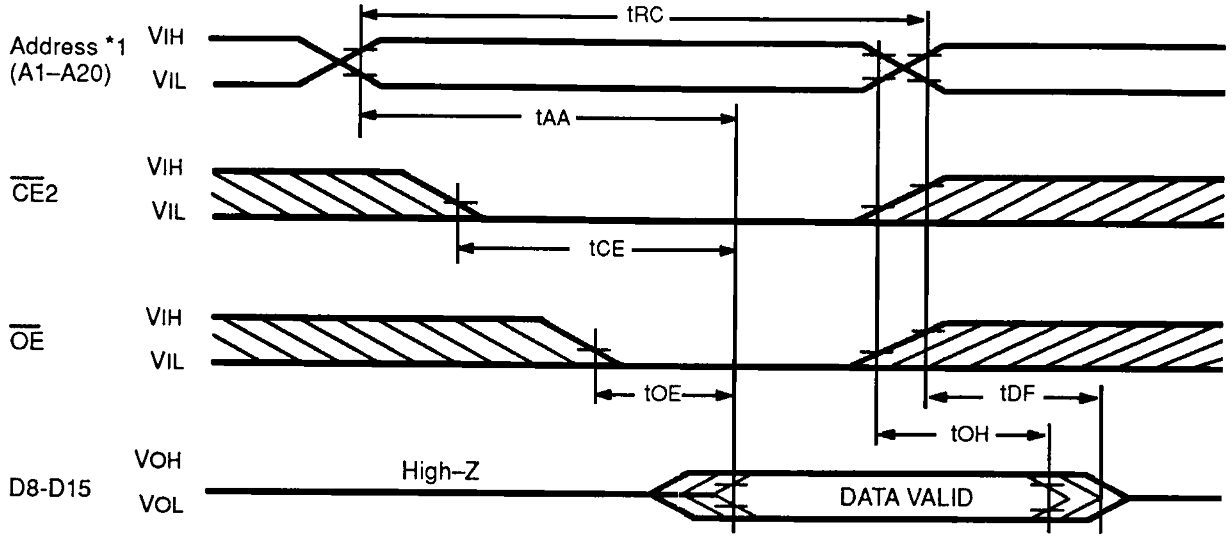


AC CHARACTERISTICS (Continued)

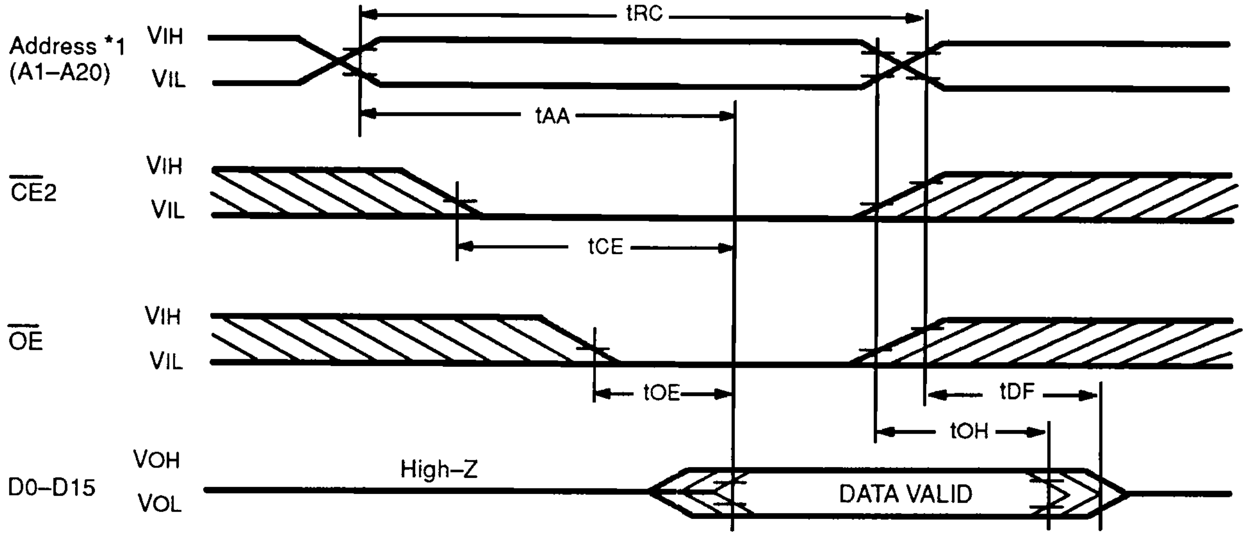
(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{\text{PGM}}$ = VIH, $\overline{\text{REG}}$ = VIH)

READ CYCLE 4: $\overline{\text{CE}}$1 = VIH: x 8–bit Bus Organization



READ CYCLE 5: $\overline{\text{CE}}$1 = $\overline{\text{CE}}$2: x 16–bit Bus Organization



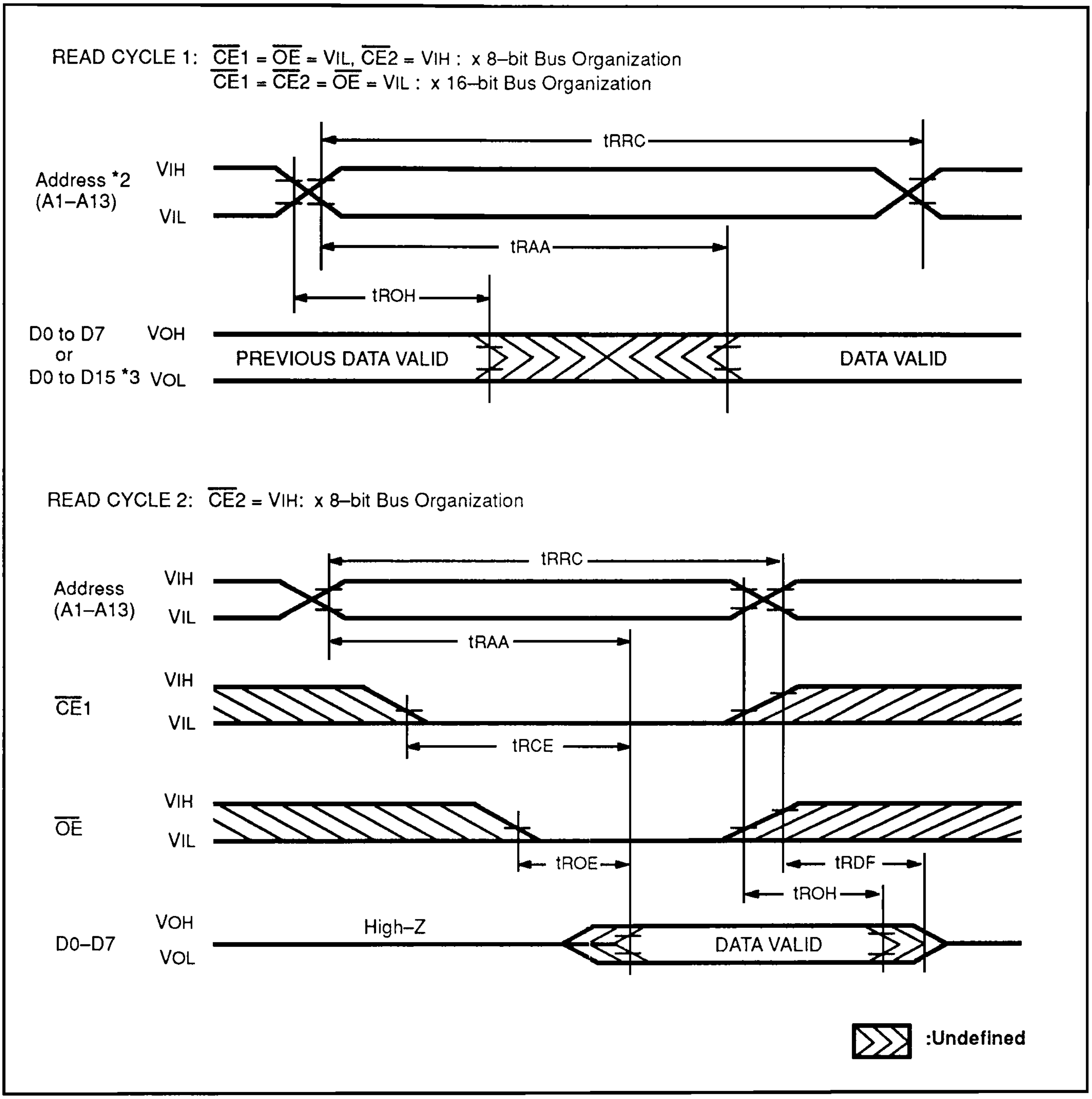
▨ :Undefined

Note: *1 A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM $(\overline{PGM} = V_{IH}, \overline{REG} = V_{IL})$ *1



READ CYCLE 1: $\overline{CE}1 = \overline{OE} = V_{IL}, \overline{CE}2 = V_{IH}$: x 8–bit Bus Organization
$\overline{CE}1 = \overline{CE}2 = \overline{OE} = V_{IL}$: x 16–bit Bus Organization

READ CYCLE 2: $\overline{CE}2 = V_{IH}$: x 8–bit Bus Organization

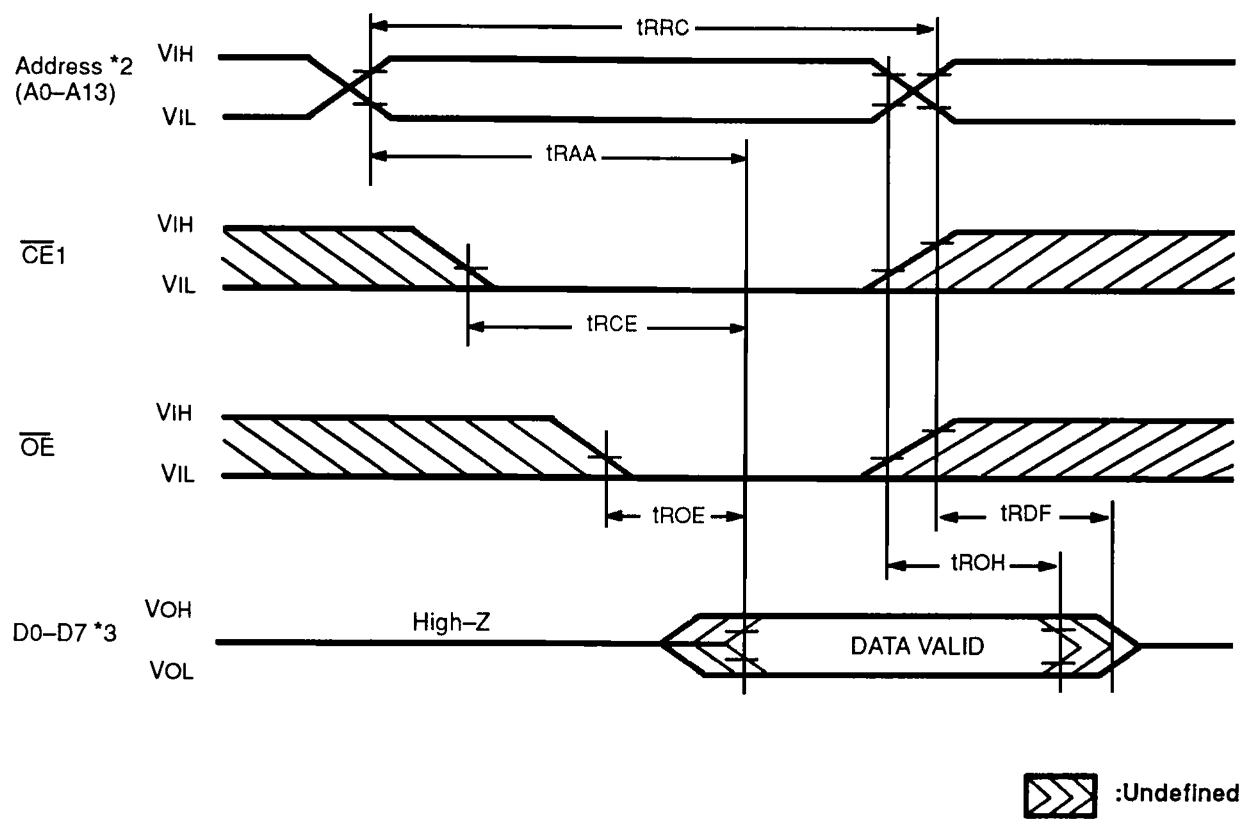
Notes: *1 This timing diagram is for MB98A60813, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.
*2 A0 = Either VIH or VIL during 16 bits bus organization.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{PGM}$ = VIH, $\overline{REG}$ = VIL) *1

READ CYCLE 3: $\overline{CE1}$ = $\overline{CE2}$: x 16–bit Bus Organization



Notes: *1 This timing diagram is for MB98A60813, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.
*2 A0 = Either VIH or VIL.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE *1

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	tRWR		10	ms
Address Setup Time	tRAS	20		ns
Chip Enable Setup Time	tRCS	0		ns
Output Enable Setup Time	tROES	20		ns
Write Pulse Width	tRWP	100		ns
Address Hold Time	tRAH	50		ns
Data Setup Time	tRDS	50		ns
Data Hold Time	tRDH	20		ns
Chip Enable Hold Time	tRCH	0		ns
Output Enable Hold Time	tROEH	20		ns
Write Recovery Time	tRRE	50		ns
End of Write to Output Time	tRRBO		100	ns
Number of Write per Byte	N	10000		Times
Write Enable Hold Time	tRWEH	10		ns

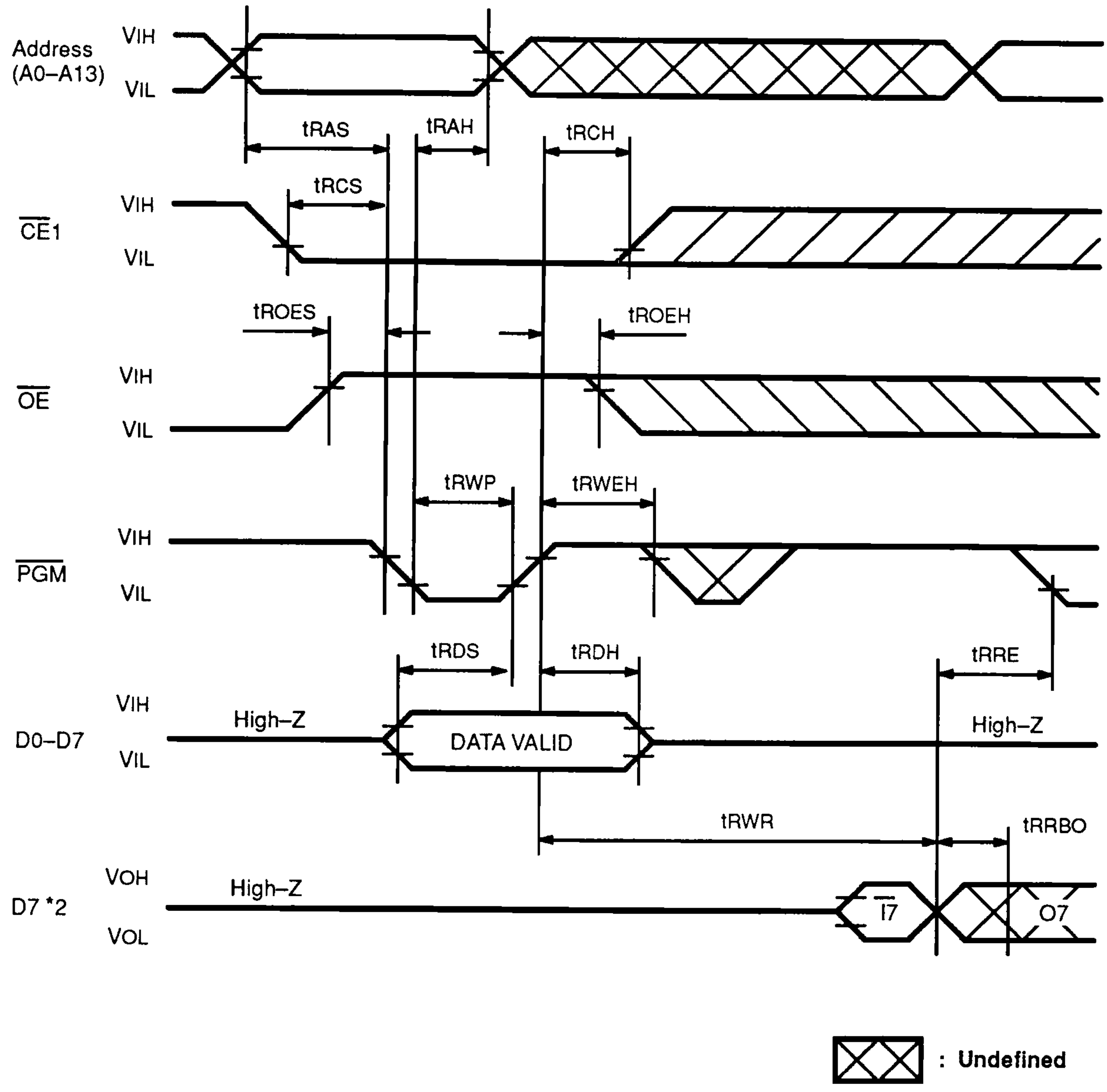
Note: *1 This parameter is for MB98A60813, 60913, 61013, and 61113.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{\text{PGM}}$=CONTROLLED, $\overline{\text{REG}}$ = VIL) *1

WRITE CYCLE 1: $\overline{\text{CE2}}$ = VIH : x 8–bit Bus Organization

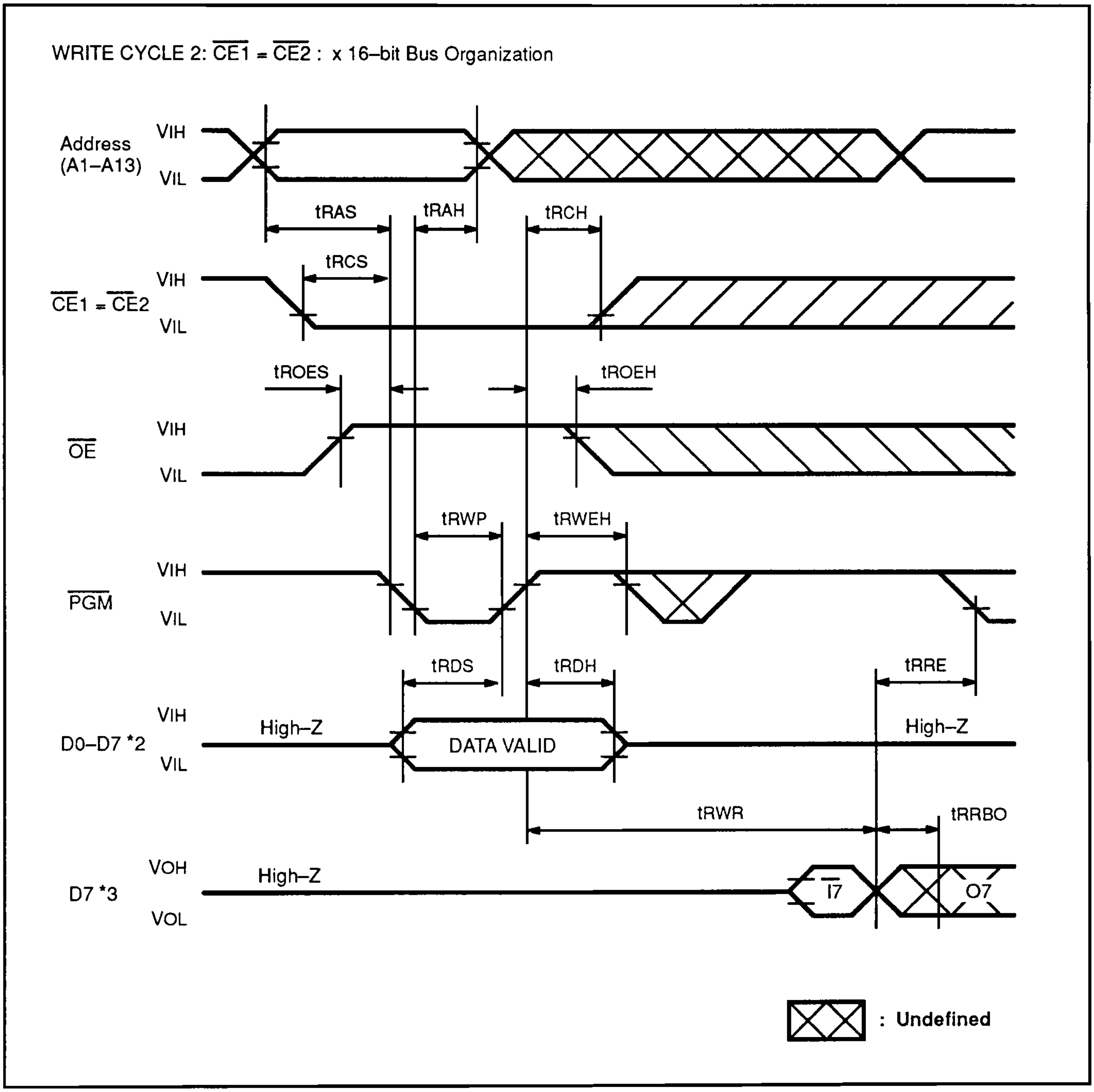


Notes: *1 This timing diagram is for MB98A60813, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.
*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{\text{PGM}}$=CONTROLLED, $\overline{\text{REG}}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A60813, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.

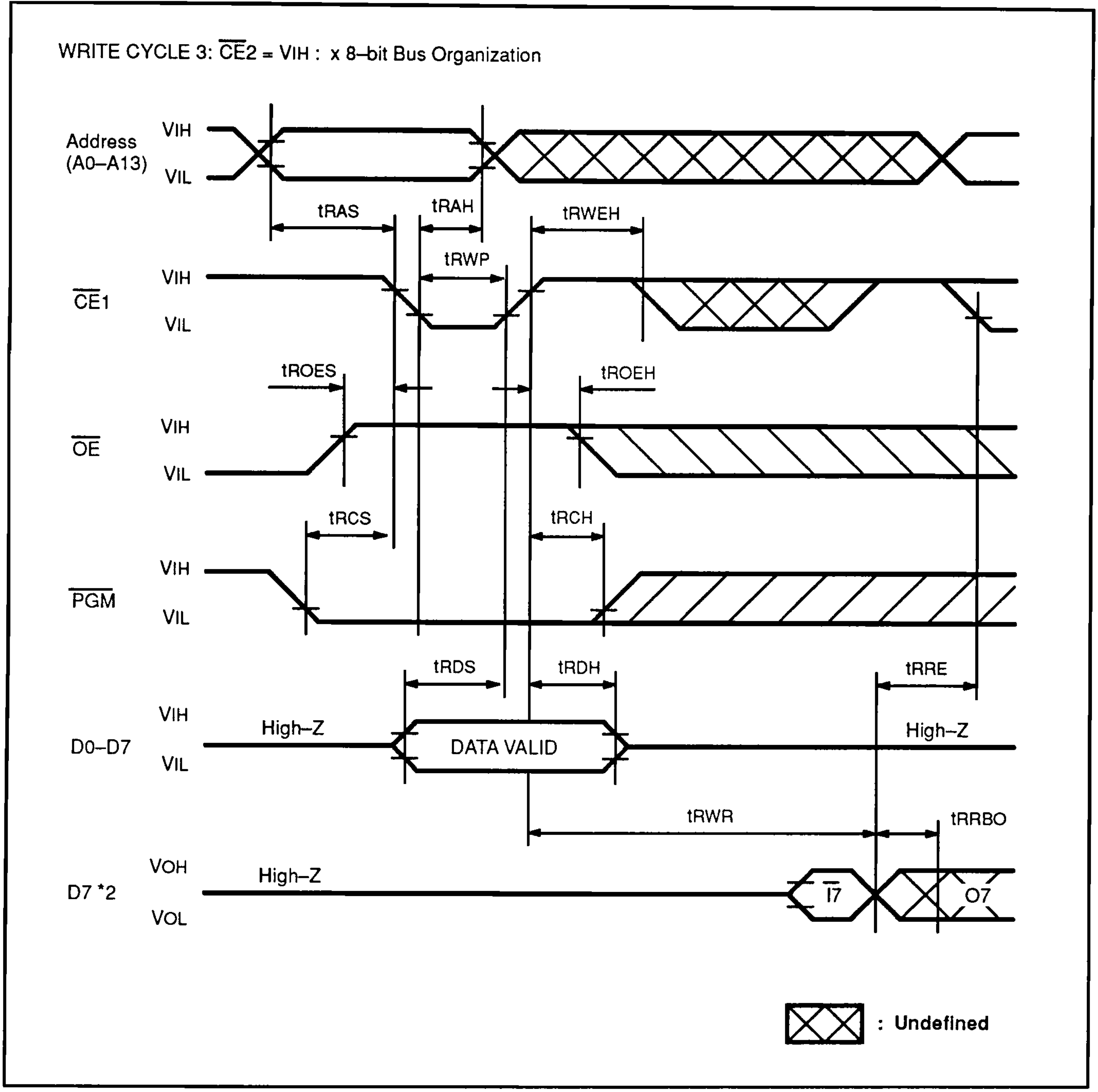
*2 H-level or L-level is output from D8 to D15.

*3 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{\text{CE}}$=CONTROLLED, $\overline{\text{REG}}$ = VIL) *1



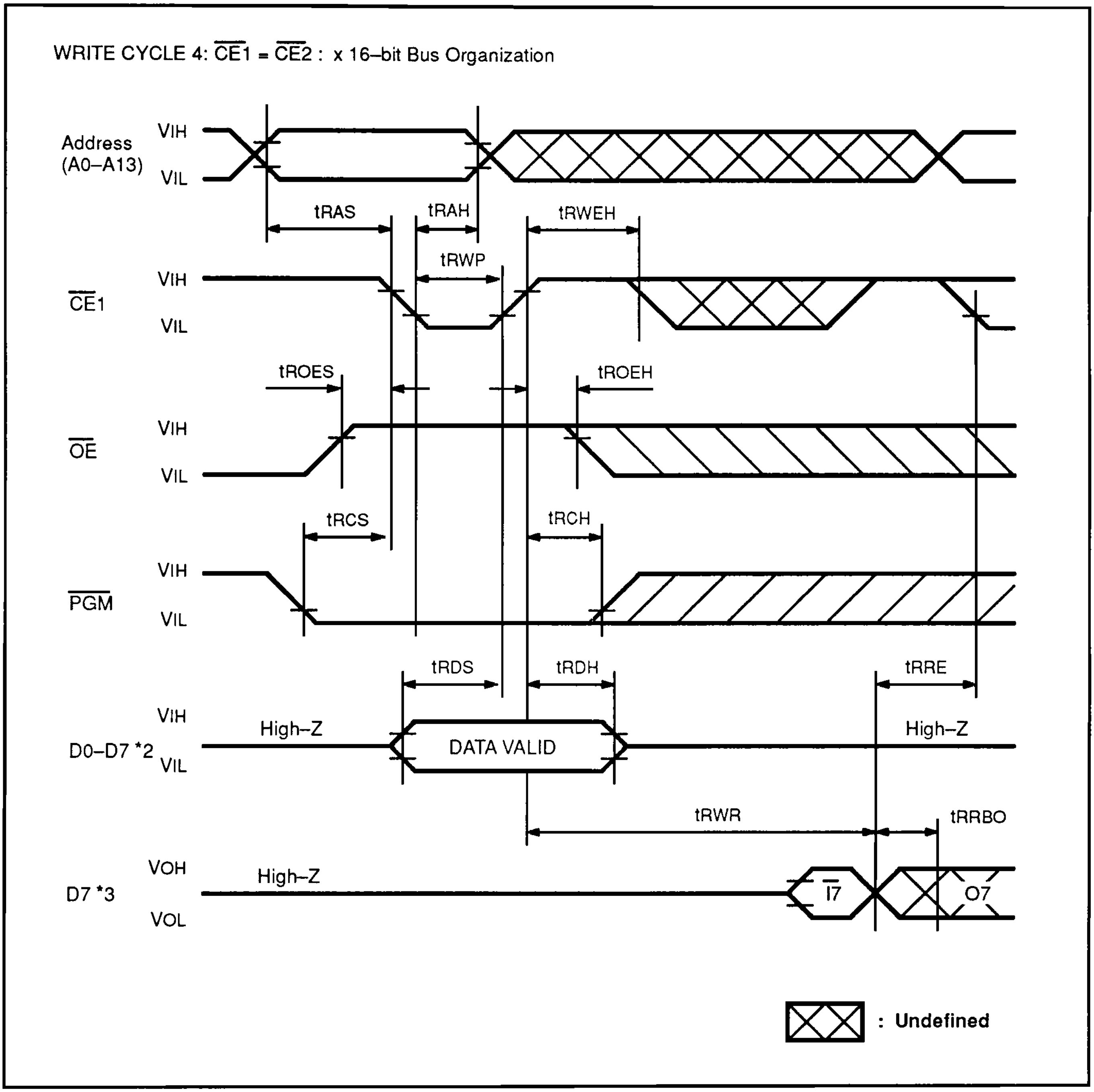
Notes: *1 This timing diagram is for MB98A60813, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.

*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

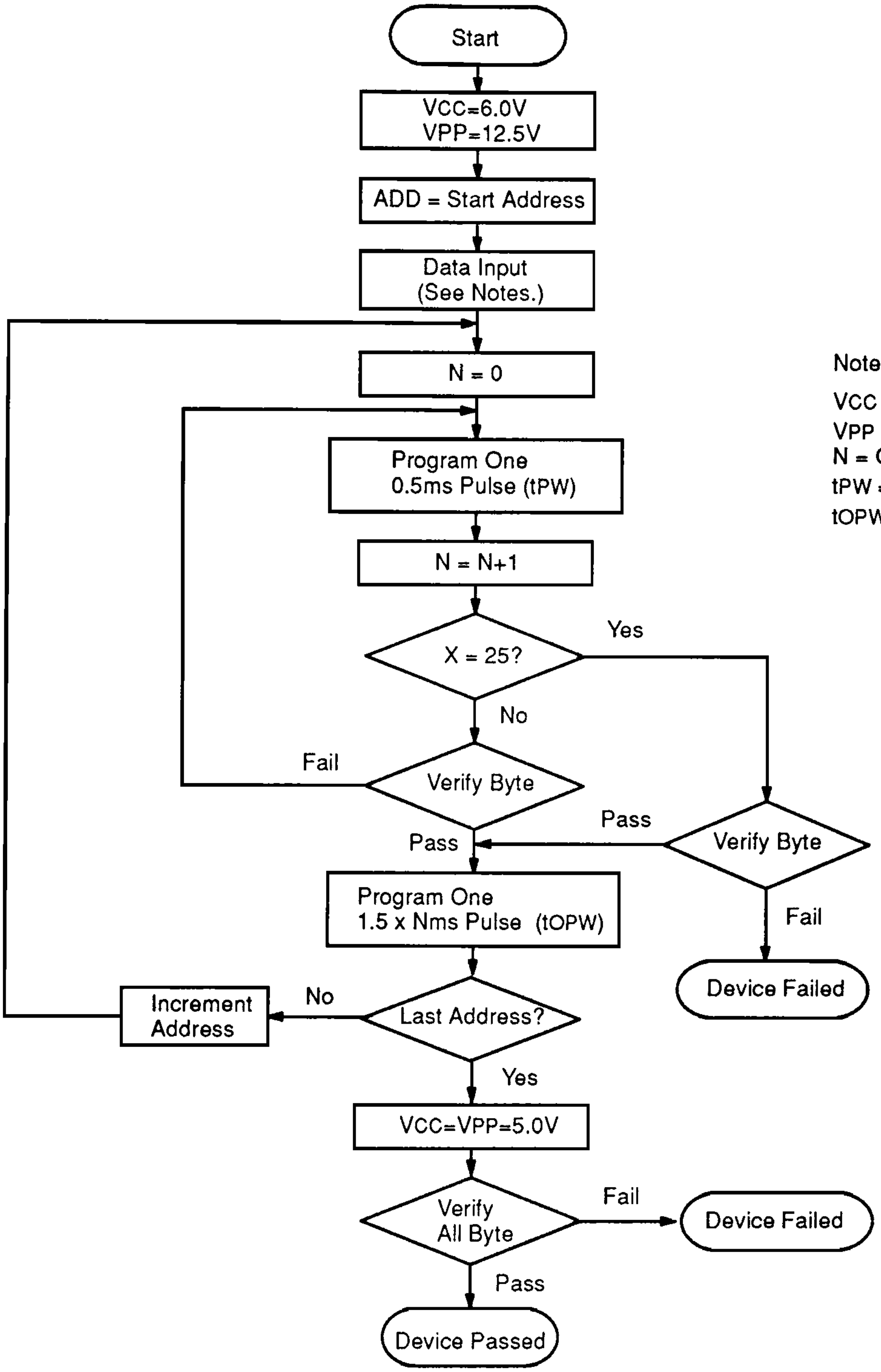
ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{\text{CE}}$=CONTROLLED, $\overline{\text{REG}}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A68013, 60913, 61013, and 61113. "FF" data is available on MB98A60812, 60912, 61012, and 61112 only.
*2 H-level or L-level is output from D8 to D15.
*3 Data polling operation.

PROGRAMMING INFORMATION

PROGRAMMING FLOWCHART



Notes:
VCC = 6V ± 0.25V
VPP = 12.5V ± 0.3V
N = Counter Value
tPW = 0.5ms ± 5%
tOPW = 1.5Nms ± 5%

PROGRAMMING INFORMATION (Continued)

PROGRAMMING

When the MB98A6081x, 6091x, 6101x, and 6111x are shipped from the factory, all memory cells are set to the high state (logic 1). During the programming procedure, affected bit cells are set to the low state (logic 0).

When +12.5 (±0.3) volts is applied to VPP, +6.0 (±0.25) volts is applied to VCC, CE1 or CE2 (or both CE1 and CE2) = VIL, OE and PGM = VIH, the programming mode is initiated. Next, the proper address is input and data pattern is applied to the input buffer. After both the address and data are stable, a 0.5-millisecond TTL pulse is applied to the PGM pin. Upon verification of written data, an overpulse should be applied to complete the programming of one byte with the condition of OE = VIL. (The over pulse is three times the initial pulse width times the number of pulse used to accomplish a write.) Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Caution

The width of one programming pulse **must not** exceed 0.525ms; i.e., do not apply a continuous TTL low level voltage to the PGM.

Caution

Do **not** apply TTL low-level voltage to the PGM pin during the programming mode (VPP = +12.5 volts), or switch the VPP voltage from VCC to +12.5 volts or vice-versa. To do so may cause device failure.

ELECTRONIC SIGNATURE

The MB98A6081x, 6091x, 6101x, and 6111x have no electronic signature code. Therefore, more than +6 volts should not be applied to A9 pin.

DC CHARACTERISTICS (TA=25°C, VCC=6V±0.25V *1, VPP=12.5V±0.5V *2)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current *3		ILI		10	µA
VPP Supply Current during Programing	CE1=CE2=VIL OE=VIH, PGM=VIL	IPP2		100	mA
VPP Supply Current during Programing Inhibit and Verify	PGM=VIH	IPP3		10	mA
VCC Supply Current during Programing and Verify		ICC1		100	mA
Input High Voltage		VIH	2.4	VCC+0.3	V
Input Low Voltage		VIL	−0.1	0.6	V
Output High Voltage *4	VOH=−1.0mA	VOH	2.4		V
Output Low Voltage *5	VOL=2.1mA	VOL		0.45	V

Notes: *1 VPP (+12.5V) must be applied after VCC (+6V) is defined, and must be off before VCC is powered off.

*2 VPP must not be greater than 13.5 volts, including overshoot. Permanent device damage may occur if the card is taken out or put into the programmer while VPP remains at 12.5 volts or greater.

*3 This value does not apply to VPP1, VPP2, CE1, CE2, PGM and REG.

*4 This value does not apply to WP, BVD1 and BVD2.

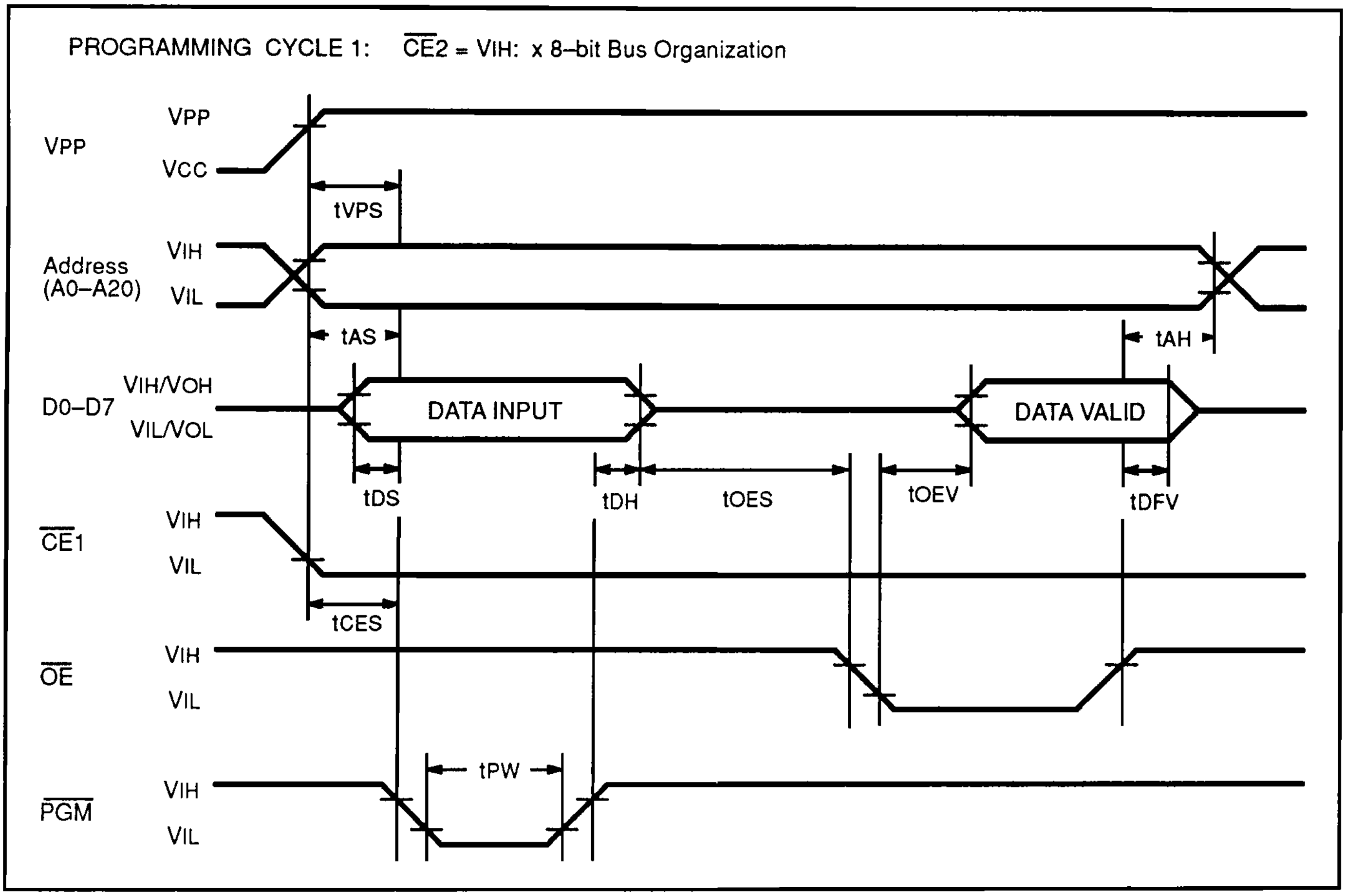
*5 This value does not apply to CD1 and CD2.

PROGRAMMING INFORMATION (Continued)

AC CHARACTERISTICS (TA=25°C, VCC=6V±0.25V, VPP=12.5V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	tAS	2			µs
Data Setup Time	tDS	2			µs
Card Enable Setup Time	tCES	2			µs
Output Enable Setup Time	tOES	2			µs
VCC/VPP Setup Time	tVPS	2			µs
Programming Pulse Width	tPW	0.475	0.5	0.525	ms
Additional Programming Pulse Width	tOPW	1.4		39.4	ms
Programming Pulse Number	N	1		25	Times
Data Hold Time	tDH	2			µs
Address Hold Time	tAH	0			µs
Output Enable to Data Valid	tOEV			500	ns
Output Disable to Output Float Delay	tDFV			150	ns

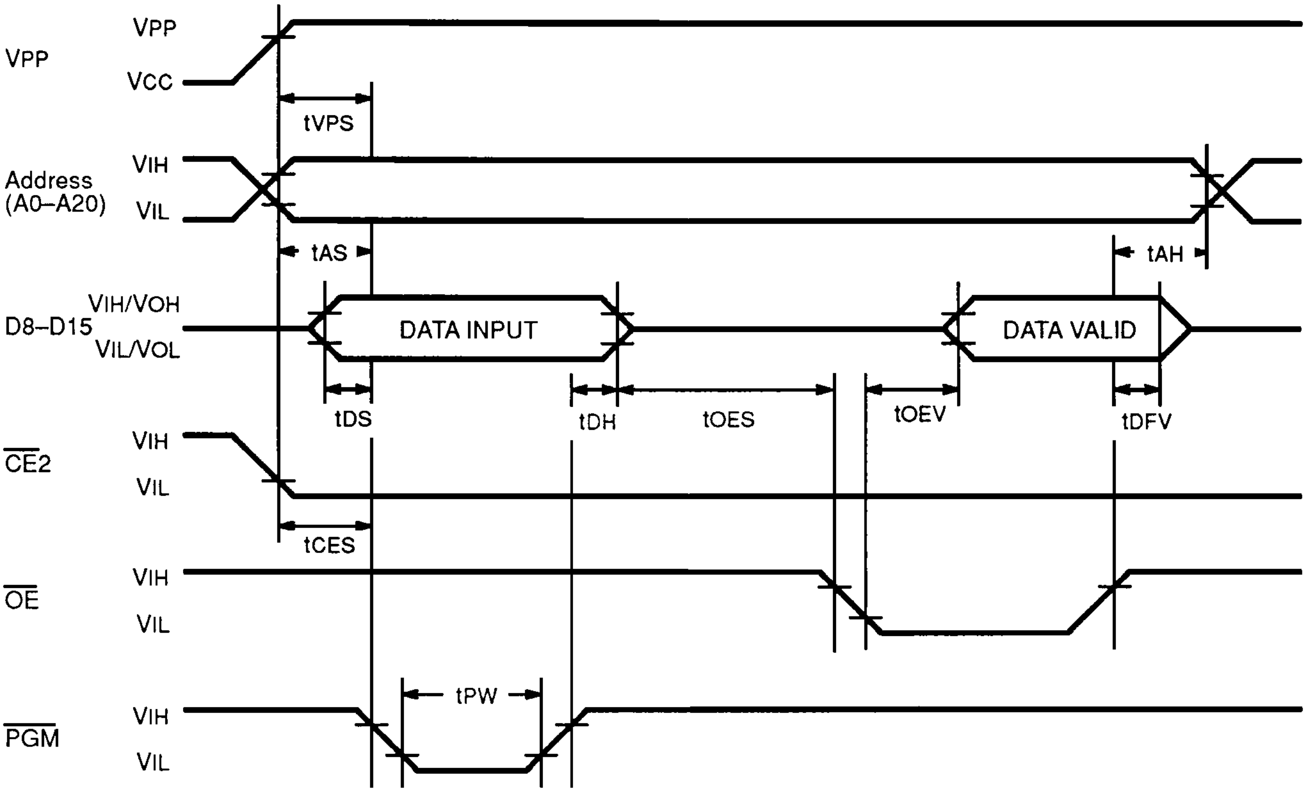
PROGRAMMING CYCLE TIMING DIAGRAM



PROGRAMMING INFORMATION (Continued)

PROGRAMMING CYCLE TIMING DIAGRAM

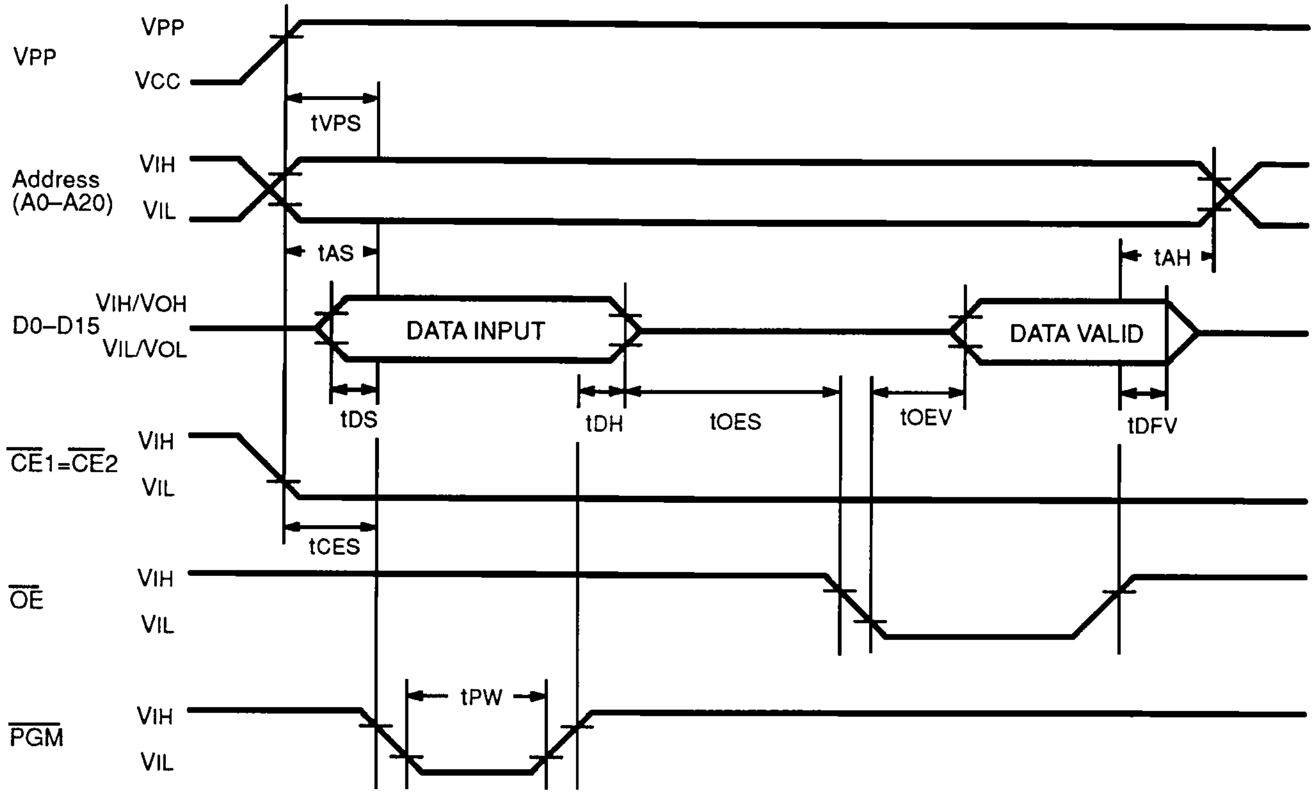
PROGRAMMING CYCLE 2: $\overline{CE}1$ = VIH: x 8–bit Bus Organization



PROGRAMMING INFORMATION (Continued)

PROGRAMMING CYCLE TIMING DIAGRAM

PROGRAMMING CYCLE 3: $\overline{CE1} = \overline{CE2}$: x 16–bit Bus Organization

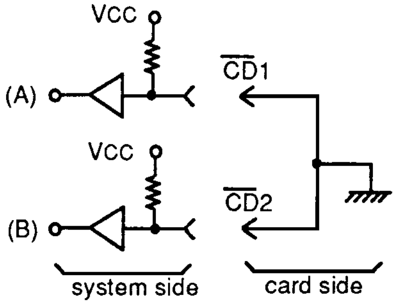


CARD DETECTION FEATURE FOR OTPROM CARD

1. CARD DETECTION PINS

$\overline{\text{CD}}$1, $\overline{\text{CD}}$2: Card Detection Pins

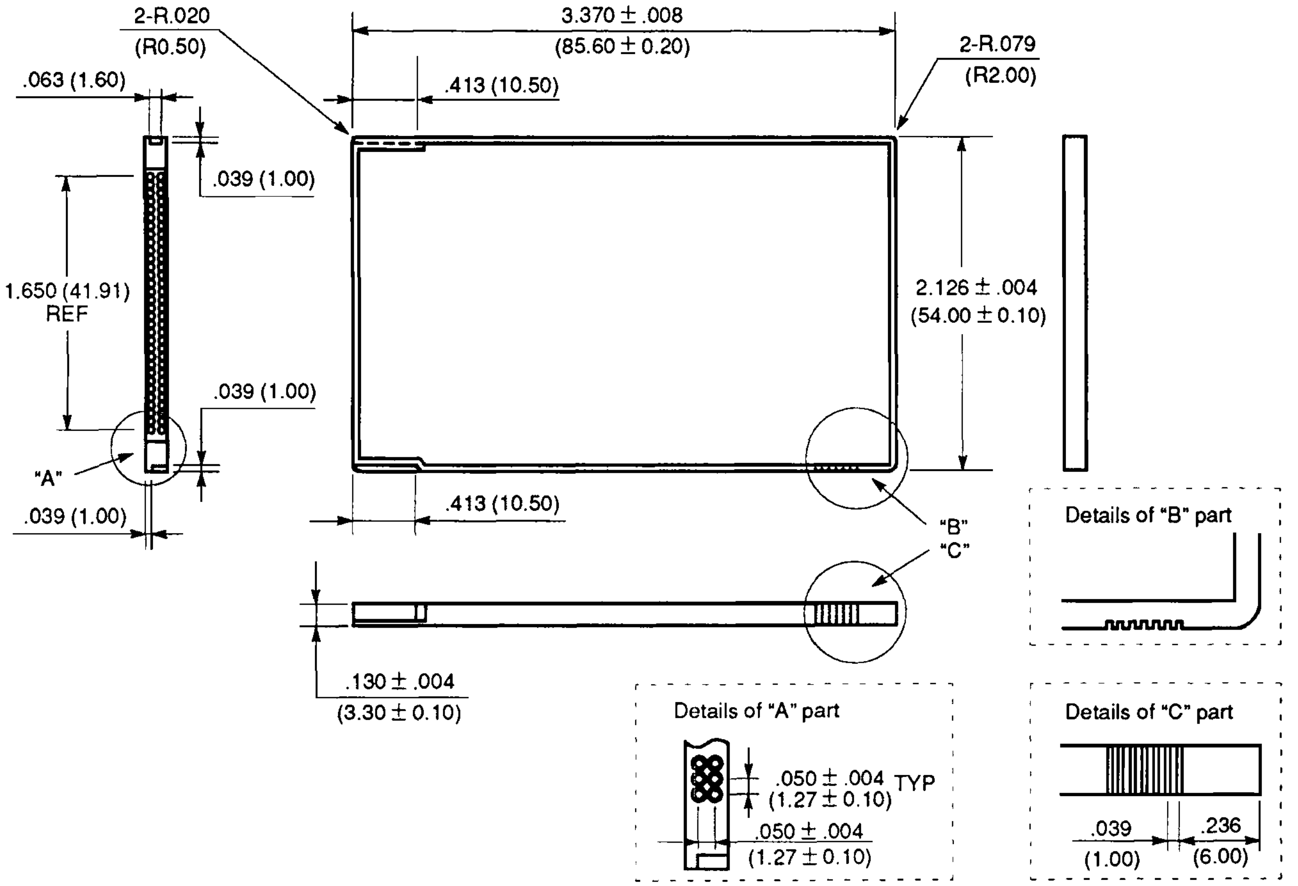
These pins detect the insertion of the card into the system. (See Fig. 4.)
When the memory card has been correctly inserted, $\overline{\text{CD}}$1 and $\overline{\text{CD}}$2 are detected by the system. $\overline{\text{CD}}$1, $\overline{\text{CD}}$2 are tied to ground on the card side as shown in Fig. 4.



– Fig. 4 –

PACKAGE DIMENSIONS

68–PIN PLASTIC CARD
(CASE No.: CRD-68P-M02)



Dimensions in
inches (millimeters)

FUJITSU LIMITED

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