Philips Components–Signetics

Document No.	853–0660
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10131
Flip-Flop

Dual D-Type Master-Slave Flip-Flop

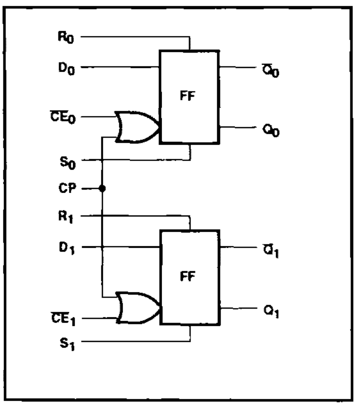
FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 45mA**

DESCRIPTION

The 10131 is a Dual Master-Slave Flip-Flop. Each flip-flop can be clocked separately by holding the common Clock in the Low-State and using the Clock Enable inputs for the clocking function. While the clock is Low, data at the D_n inputs are allowed to enter the master section. The output states of the flip-flops register the data present at the D_n inputs on the rising edge of the Clock. Output data (Q_n) is latched and not affected by changes at the D_n inputs while the Clock (CP) is High. All unused inputs must be tied Low to V_{IL} or V_{EE}.

LOGIC DIAGRAM



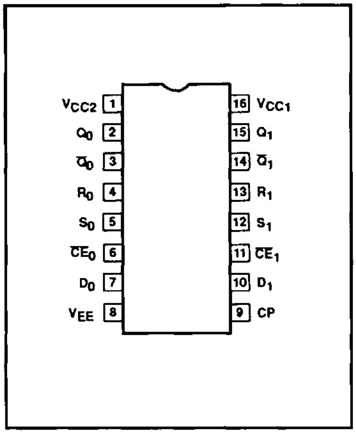
PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
CP	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

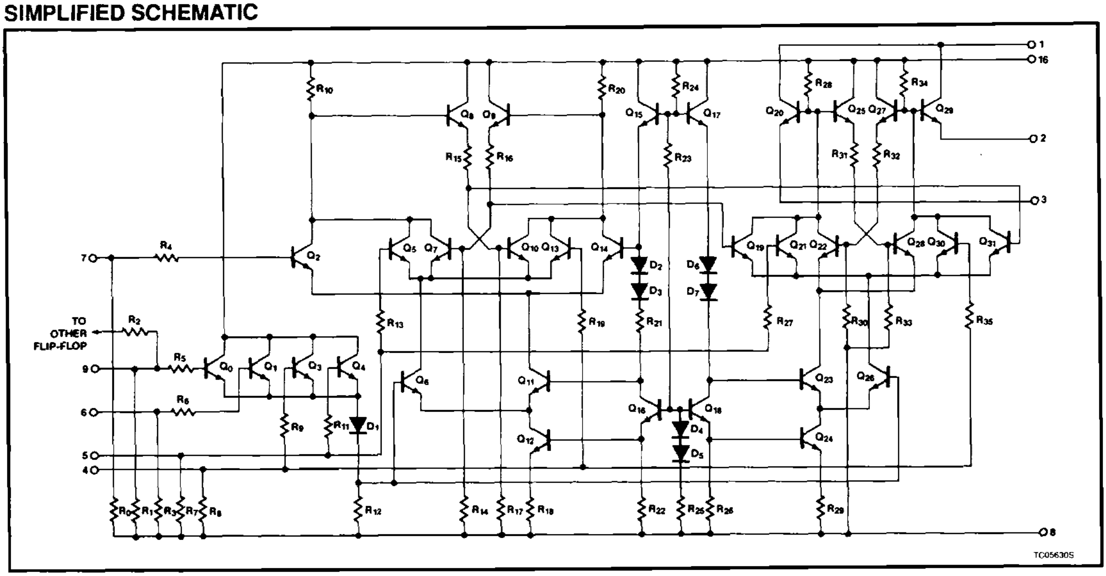
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10131N
16–Pin Ceramic DIP	10131F
16–Pin SO	10131D

PIN CONFIGURATION



SIMPLIFIED SCHEMATIC



FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUT
D_n	CP	$\overline{C}_E$*	Q_{n+1}**
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

* Conditions for CP and $\overline{CE}$ may be interchanged. In this table $\overline{CE}$ is static, while for CP and H represent a transition from Low to High between t_n and t_{n+1}.

** R and S = Low.

ASYNCHRONOUS OPERATION

INPUTS		OUTPUT
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N

H = High Voltage Level
L = Low Voltage Level
N = Not allowed

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to −2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to S_n inputs with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to R_n inputs, with V_{ILMIN} applied to all other inputs.	−1060		−890	mV
			$T_A = +25°C$		−960		−810	mV
			$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to S_n inputs with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to R_n inputs, with V_{ILMIN} applied to all other inputs.	−1080			mV
			$T_A = +25°C$		−980			mV
			$T_A = +85°C$		−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to R_n inputs with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to S_n inputs, with V_{ILMIN} applied to all other inputs.			−1655	mV
			$T_A = +25°C$				−1630	mV
			$T_A = +85°C$				−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to R_n inputs with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to S_n inputs, with V_{ILMIN} applied to all other inputs.	−1890		−1675	mV
			$T_A = +25°C$		−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input with V_{ILMIN} applied to all other inputs.			425	µA
			$T_A = +25°C$				265	µA
			$T_A = +85°C$				265	µA
		$\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		D_n inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
		R_n inputs	$T_A = -30°C$	For R_n inputs, apply V_{IHMAX} to D_n inputs and to R_n input under test with V_{ILMIN} applied to all other inputs.			525	µA
			$T_A = +25°C$				330	µA
			$T_A = +85°C$				330	µA
		S_n inputs	$T_A = -30°C$	For S_n inputs, apply V_{IHMAX} to D_n inputs and to S_n input under test with V_{ILMIN} applied to all other inputs.			525	µA
			$T_A = +25°C$				330	µA
			$T_A = +85°C$				330	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				62	mA
			$T_A = +25°C$			45	56	mA
			$T_A = +85°C$				62	mA

Flip–Flop 10131

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	TYP.	MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

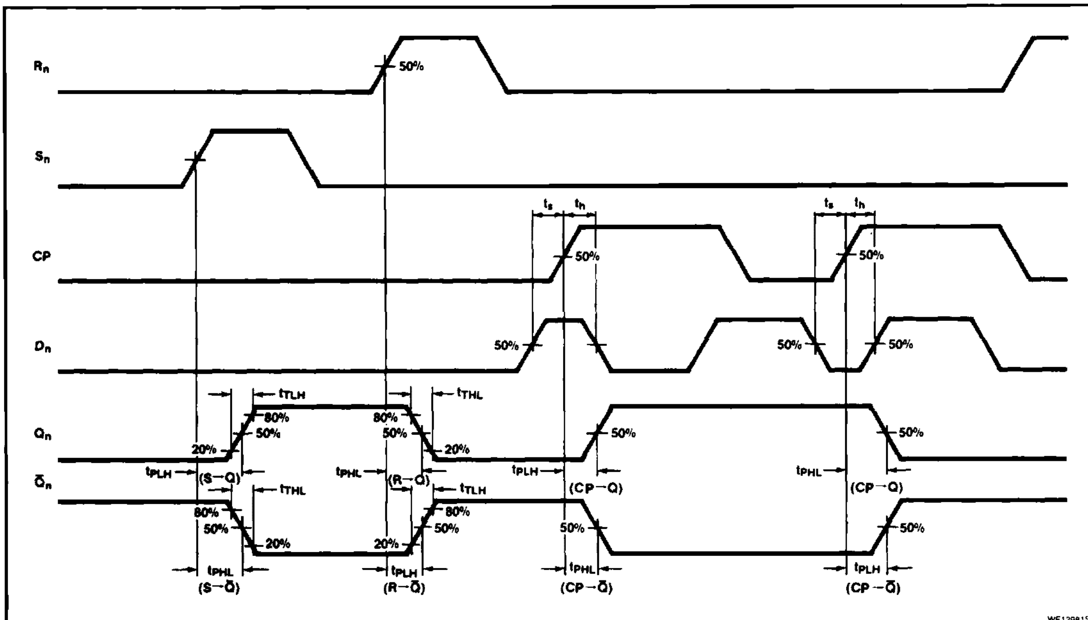
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $T_A = -30°C$ MIN.	$T_A = -30°C$ MAX.	$T_A = +25°C$ MIN.	$T_A = +25°C$ TYP.	$T_A = +25°C$ MAX.	$T_A = +85°C$ MIN.	$T_A = +85°C$ MAX.	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	160		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	1.70 1.70	4.60 4.60	1.80 1.80	3.00 3.00	4.50 4.50	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n to Q_n, $\overline{Q}_n$	Waveform 1	1.70 1.70	4.40 4.40	1.80 1.80	2.80 2.80	4.30 4.30	1.80 1.80	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n, $\overline{Q}_n$	Waveform 1	1.70 1.70	4.40 4.40	1.80 1.80	2.80 2.80	4.30 4.30	1.80 1.80	4.80 4.80	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to CP	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	4.60 4.60	1.10 1.10	2.50 2.50	4.50 4.50	1.10 1.10	4.90 4.90	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

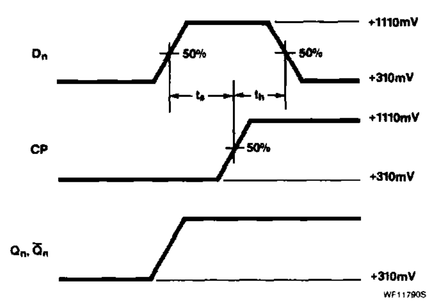
Flip–Flop

10131

AC WAVEFORMS

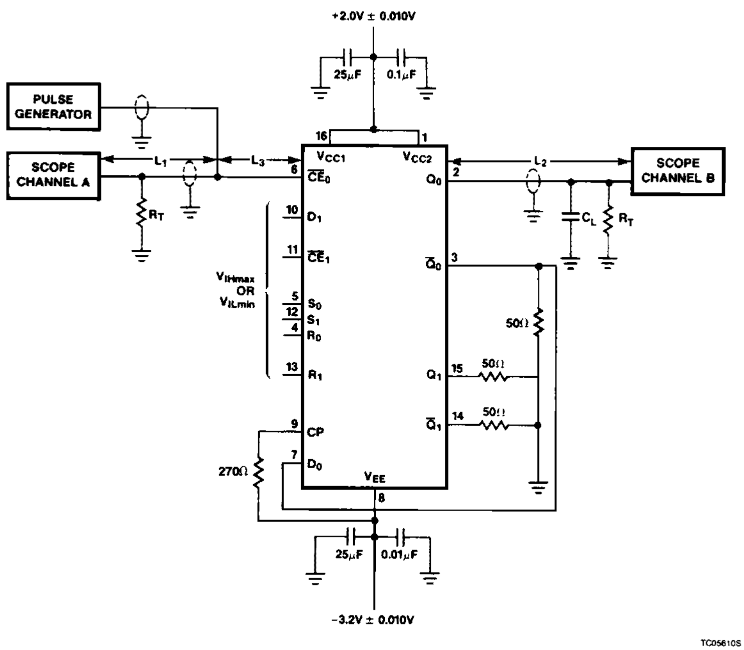


Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times

TOGGLE FREQUENCY TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.