Supertex inc.

HV702
HV712

Product Objective Specifications

200V 40-Channel Vacuum-Fluorescent Display Driver

Ordering Information

Device	Package Options	
	60 Pin Plastic Gullwing	Die
HV702	HV702PG	HV702X
HV712	HV712PG	HV712X

Features

- ☐ 220V push-pull outputs
- ☐ 40 output lines
- ☐ 5V CMOS logic
- ☐ +2.5 / -10mA output sink/source
- ☐ 40-bit shift register
- ☐ 40-bit latch
- ☐ 60-pin 2-sided Gullwing
- ☐ 6MHz shift clock
- ☐ Processed with HVCMOS® technology

General Description

The HV702/712 are designed to drive vacuum fluorescent displays used in graphic applications. The 40 outputs are supplied by 40 output latches which are fed from a 40-bit shift register. Data is shifted in on the HIGH-to-LOW clock transition. Logic control is provided by a latch enable (LE) and output clear ($\overline{CL}$). When $\overline{CL}$ is HIGH, data is reflected at the output: when $\overline{CL}$ is LOW all outputs are LOW.

Pin assignments for the HV712 have pin reversed from the HV702 for ease in PC board layout.

Absolute Maximum Ratings

Supply voltage,[1] V_{DD}	-0.5V to +7V
Supply voltage,[1] V_{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Continuous total power dissipation [2, 3]	800mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds	260°C

Notes:
1. All voltages referenced to GND
2. Duty cycle is limited by the total power dissipated in the package
3. For operation above 25°C ambient, derate linearly to 614mW/°C @ 6.4mW/°C.

Electrical Characteristics (V_{DD} = 5V, V_{PP} = 200V, T_A = -40°C to 85°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Logic supply current	I_{DD}	V_{DD} =5.5V	All outputs low			16.0	mA
		No load f_{CLK} = 6MHz	All outputs low T_A = 25°C			12.0	mA
I_{DD} (quiescent)	I_{DDQ}	V_{DD} = 5.5V T_A = 25°C	All outputs high			100	µA
High voltage supply current	I_{PP}	V_{PP}=200V No load	All outputs low			250	µA
		T_A = 25°C	All outputs low			250	µA
		T_A = 25°C	All outputs high			250	µA
High-level input voltage	V_{IH}		V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level input voltage	V_{IL}		V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
Input leak current	I_I	T_A =25°C				±1	µA
Input capacitance	C_I	T_A =25°C				25	pF
High-level data output voltage	V_{OH}	I_O = -0.1mA	V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level data output voltage	V_{OL}	I_O = +0.1mA	V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
High-level output voltage	V_{HVOH}	I_{HVO} = -1.0mA, T_A =25°C		198			V
Low-level output voltage	V_{HVOL}	I_{HVO} = +0.5mA, T_A =25°C				2.0	V
High-level output current	I_{HVOH}	V_{HVO} = 195V T_A =25°C		-10			mA
Low-level output current	I_{HVOL}	V_{HVO} = 10V, T_A =25°C		2.5			mA

Switching Characteristics (V_{DD} = 5V, V_{PP} = 200V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time, clk to data out	t_{PD}	See Figure 1,2			150	ns
Delay time high voltage output, low to high	t_{DLH}	See Figure 1, 2,[1] Each HVO [2]			4.0	µs
Delay time high voltage output, high to low	t_{DHL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs
Transition time high voltage output, low to high	t_{TLH}	See Figure 1, 2,[1] Each HVO [2]			6.0	µs
Transition time high voltage output, high to low	t_{THL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs

Notes:
1. The values of t_{DLH} and t_{DHL} are the delay times from $\overline{CL}$.
2. High voltage output terminal.

Recommended Operating Conditions

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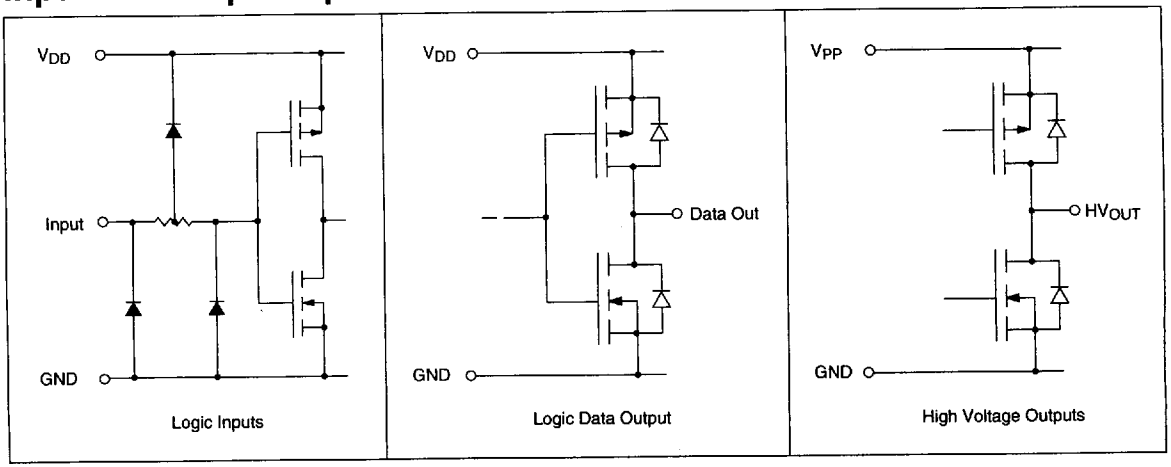
Parameter		Symbol	Conditions		Min	Max	Unit
Supply voltage		V_{DD}	Logic Supply		4.5	5.5	V
Supply voltage		V_{PP}	High voltage supply		25	200	V
High-level input voltage		V_{IH}	Each input	V_{DD} = 4.5V	3.6		V
				V_{DD} = 5.5V	4.4		V
Low-level input voltage		V_{IL}	Each input	V_{DD} = 4.5		0.9	V
				V_{DD} = 5.5		1.1	V
High-level output current		I_{HVOH}	Each HVO*			-10	mA
Low-level output current		I_{HVOL}	Each HVO*			2.5	mA
Clock frequency		f_{CLK}	Cascade			6.0	MHz
Clock pulse width		$t_{w(CLK)}$	See Figure 1, 2		70		ns
Data setup time		t_{su}	See Figure 1, 2		20		ns
Data hold time		t_h	See Figure 1, 2		45		ns
Data pulse width		$t_{w(D)}$	See Figure 1, 2		145		ns
Latch enable pulse width		$t_{w(LE)}$	See Figure 1, 2		80		ns
Data setup time	CLK-LE	$t_{su(CLK-LE)}$	See Figure 1, 2		45		ns
Data setup time	LE-CLK	$t_{su(LE-CLK)}$	See Figure 1, 2		10		ns
Data setup time	LE-$\overline{CL}$	$t_{su(LE-\overline{CL})}$	See Figure 1, 2		10		µs
Clear pulse width		$t_{w(\overline{CL})}$	See Figure 1, 2		2		µs
Operating free-air temperature range		T_{ope}			-40	+85	°C

Note:
HVO*; High voltage output terminal
Power-up sequence should be the following:

1. Connect ground.
2. Apply VDD.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply VPP.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



Parameter Measurement Information

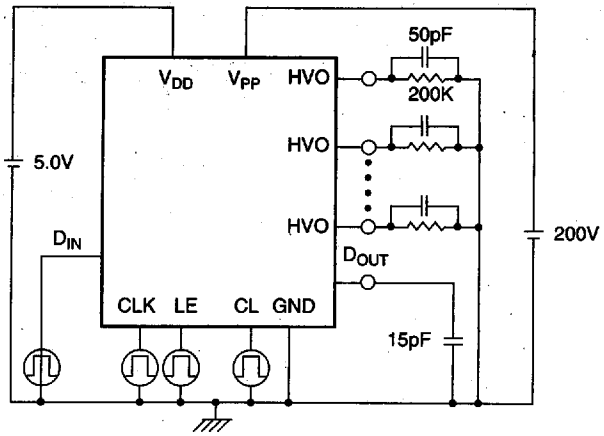


Figure 1: Test Circuit

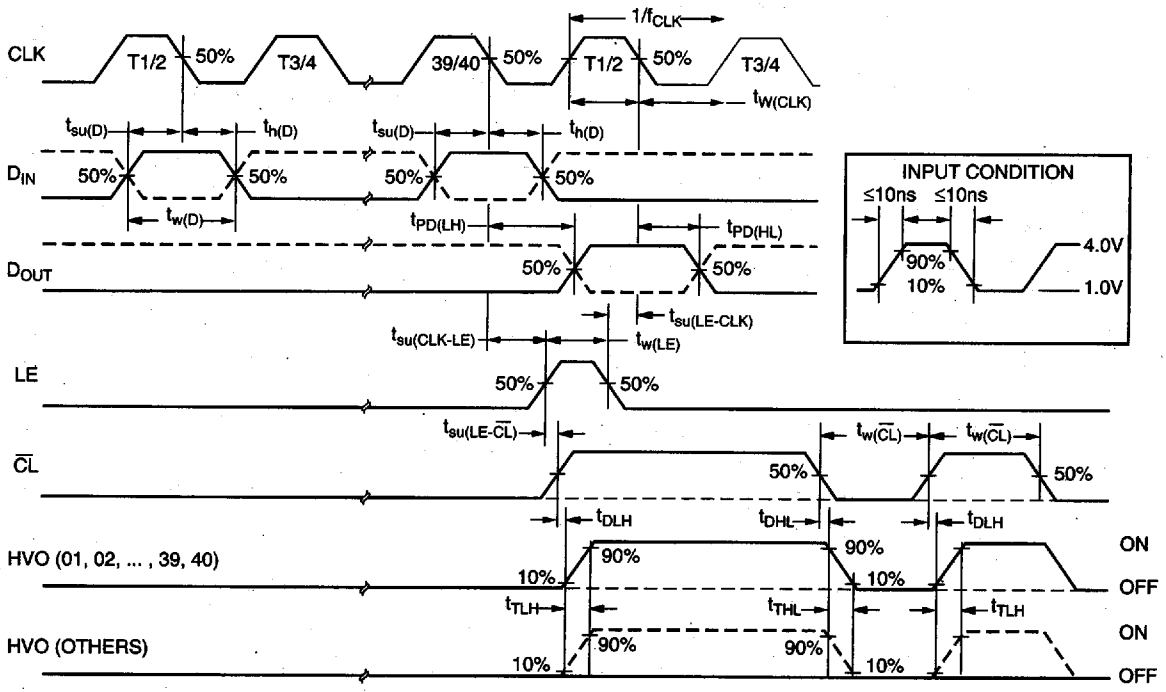
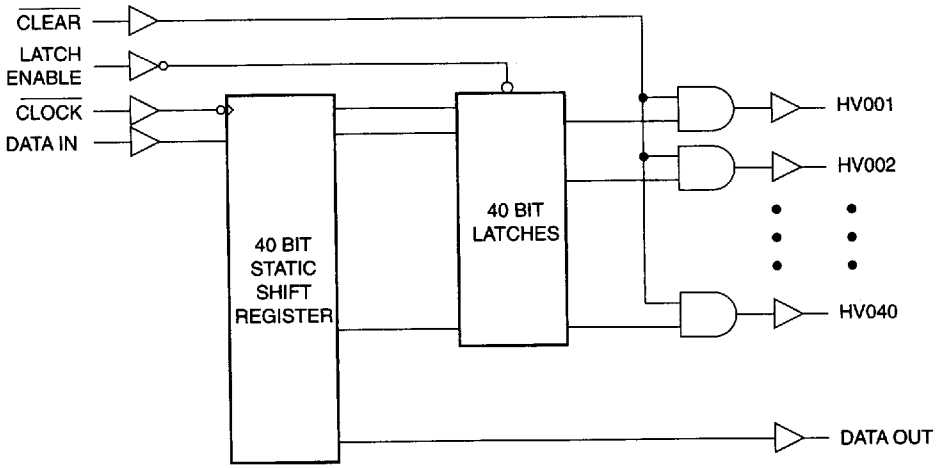


Figure 2: Timing Chart

Logic Diagram



Input Truth Table

CLK	Shift Register
↓	Data is Loaded
No Change	*

Output Truth Table

Data	LE	$\overline{CLR}$	Output
X	X	L	All O/P Low
H	H	H	High
L	H	H	Low
X	L	H	Previous Latch Data

Note:
High = high level, L = low level, X = high or low level,
↓ = high-to-low level transition
* Previous state

Pin Configurations

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Pin	Function	Pin	Function
1	HV_{OUT} 36	31	D_{IN}
2	HV_{OUT} 35	32	NC
3	HV_{OUT} 34	33	NC
4	HV_{OUT} 33	34	CLK
5	HV_{OUT} 32	35	NC
6	HV_{OUT} 31	36	$\overline{CLR}$
7	HV_{OUT} 30	37	NC
8	HV_{OUT} 29	38	NC
9	HV_{OUT} 28	39	V_{PP}
10	HV_{OUT} 27	40	NC
11	HV_{OUT} 26	41	HV_{OUT} 1
12	HV_{OUT} 25	42	HV_{OUT} 2
13	HV_{OUT} 24	43	HV_{OUT} 3
14	HV_{OUT} 23	44	HV_{OUT} 4
15	HV_{OUT} 22	45	HV_{OUT} 20
16	HV_{OUT} 21	46	HV_{OUT} 19
17	HV_{OUT} 37	47	HV_{OUT} 18
18	HV_{OUT} 38	48	HV_{OUT} 17
19	HV_{OUT} 39	49	HV_{OUT} 16
20	HV_{OUT} 40	50	HV_{OUT} 15
21	NC	51	HV_{OUT} 14
22	V_{PP}	52	HV_{OUT} 13
23	NC	53	HV_{OUT} 12
24	GND	54	HV_{OUT} 11
25	NC	55	HV_{OUT} 10
26	LE	56	HV_{OUT} 9
27	NC	57	HV_{OUT} 8
28	V_{DD}	58	HV_{OUT} 7
29	NC	59	HV_{OUT} 6
30	D_{OUT}	60	HV_{OUT} 5

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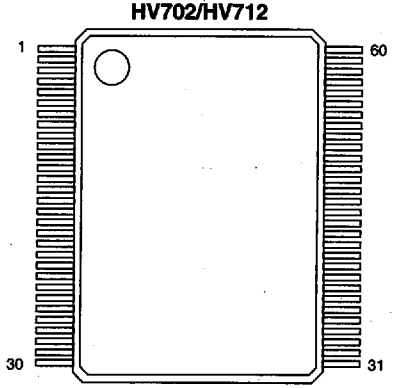
Pin	Function	Pin	Function
1	HV_{OUT} 5	31	D_{OUT}
2	HV_{OUT} 6	32	NC
3	HV_{OUT} 7	33	V_{DD}
4	HV_{OUT} 8	34	NC
5	HV_{OUT} 9	35	LE
6	HV_{OUT} 10	36	NC
7	HV_{OUT} 11	37	GND
8	HV_{OUT} 12	38	NC
9	HV_{OUT} 13	39	V_{PP}
10	HV_{OUT} 14	40	NC
11	HV_{OUT} 15	41	HV_{OUT} 40
12	HV_{OUT} 16	42	HV_{OUT} 39
13	HV_{OUT} 17	43	HV_{OUT} 38
14	HV_{OUT} 18	44	HV_{OUT} 37
15	HV_{OUT} 19	45	HV_{OUT} 21
16	HV_{OUT} 20	46	HV_{OUT} 22
17	HV_{OUT} 4	47	HV_{OUT} 23
18	HV_{OUT} 3	48	HV_{OUT} 24
19	HV_{OUT} 2	49	HV_{OUT} 25
20	HV_{OUT} 1	50	HV_{OUT} 26
21	NC	51	HV_{OUT} 27
22	V_{PP}	52	HV_{OUT} 28
23	NC	53	HV_{OUT} 29
24	NC	54	HV_{OUT} 30
25	$\overline{CLR}$	55	HV_{OUT} 31
26	NC	56	HV_{OUT} 32
27	CLK	57	HV_{OUT} 33
28	NC	58	HV_{OUT} 34
29	NC	59	HV_{OUT} 35
30	D_{IN}	60	HV_{OUT} 36

Package Outline

HV702/HV712



top view