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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35040-XXXFP and M35041-XXXFP are character pattern display controllers designed to display title, time and date, and operation messages inside the viewfinder. It uses a silicon gate CMOS process and is housed in a 20-pin shrink SOP package.

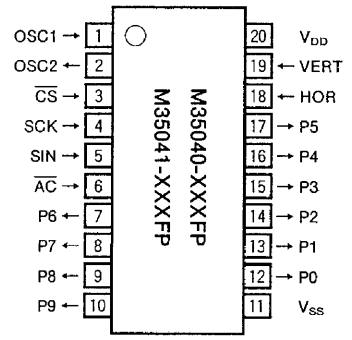
The differences among M35040-XXXFP and M35041-XXXFP are noted below.

The descriptions that follow describe the M35040-XXXFP unless otherwith noted.

Type name	Characters available	DA7 of display RAM (bit 7 of addresses 00_{16} to EF_{16})
M35040-XXXFP	128	Set to "0"
M35041-XXXFP	256	Set the MSB of character code

The character patterns for the M35040-001FP and M35041-001FP which are standard ROM type of the M35040-XXXFP and M35041-XXXFP are also included.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2Q-A

FEATURES

- Screen composition ····· 24 columns × 10 lines
- Number of characters displayed ····· 240 (Max.)
- Character composition ····· 12 × 18 dot matrix
- Characters available
  - M35040-XXXFP ····· 128 characters
  - M35041-XXXFP ····· 256 characters
- Character sizes available ··· 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ····· 62 locations
  - Vertical direction ····· 64 locations
- Blinking ····· Charactherunits
  - Cycle : approximately 1 second, or approximately 0.5 seconds
  - Duty : 25%, 50%, or 75%
- Data input ····· By the 16-bit serial input function
- Coloring
  - Character unit ····· 8 colors (RGB output)
  - Raster coloring ····· 8 colors (RGB output) Specified by register
  - Matrix-outline coloring ····· 8 colors (RGB output) Specified by register
  - Border coloring ····· 8 colors (RGB output) Specified by register
- Blanking
  - Blanking0 ····· Blanking off
    Character size blanking
    Border size blanking
    Matrix-outline blanking
  - Blanking1 ····· Blanking of the border size for the G component of RGB output.
  - Blanking2 ····· Blanking of the border size for the B component of RGB output.
- Synchronized separation circuit ····· Built-in
- Output ports
  - 6 shared output ports (toggled between RGB output)
  - 4 dedicated output ports
- Oscillation stop function
  - Be possible to stop the oscillation for display
- Display RAM erase function
- Reversed character display function (character unit)

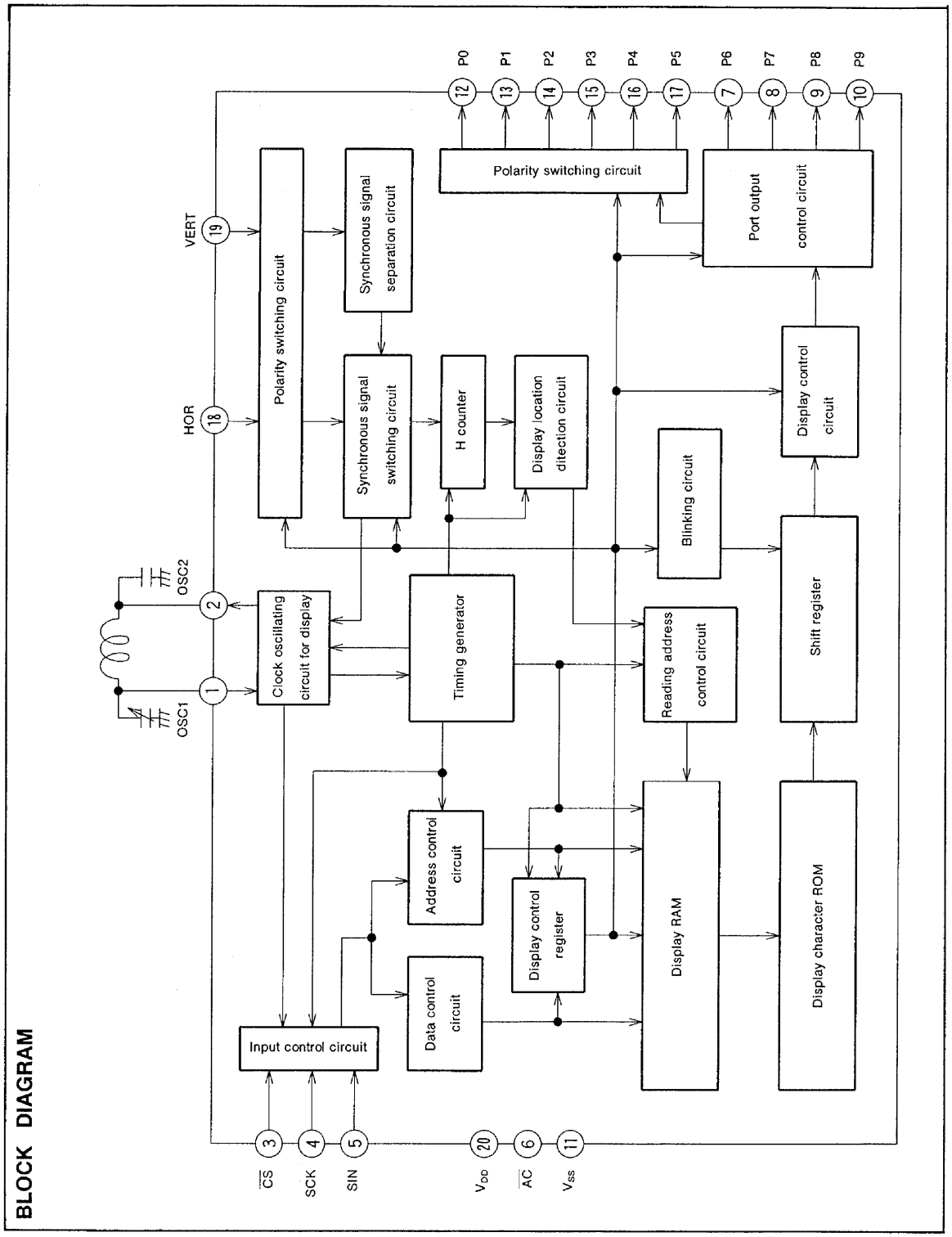
APPLICATION

Cam corder

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input /Output	Function
1	OSC1	Pins for attachment of external oscillator circuit	Input	There are the pins for attaching an external display oscillator circuit. The standard oscillation frequency is approximately 7MHz. This oscillation frequency determines the horizontal position of the display on the viewfinder and the width of the characters. LC oscillation and RC oscillation are possible.
2	OSC2		Output	
3	$\overline{CS}$	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
4	SCK	Serial clock input	Input	When $\overline{CS}$ pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
5	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Inculdes built-in pull-up resistor.
6	$\overline{AC}$	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
7	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
8	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
9	P8	Port P8 output	Output	This is the output port. Port data is set by PTD8.
10	P9	Port P9 output	Output	This is the output port. Port data is set by PTD9.
11	V_{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin.
12	P0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This pin can be toggled between port pin output, BLNK1 signal output, and CO signal output.
15	P3	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This pin can be toggled between port pin output, BLNK2 signal output, and BLNK signal output.
17	P5	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input.
19	VERT	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input.
20	V_{DD}	Power pin	—	Please connection to +5V or +3V with the power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 00_{16} to EF_{16} are assigned to the display RAM, address $F0_{16}$ to $F5_{16}$ are assigned to the display control registers. The internal circuit is reset and all display control registers (address $F0_{16}$ to $F5_{16}$) are set to "0" and display RAM (address 00_{16} to EF_{16}) are set to "FF_{16}" when the $\overline{AC}$ pin level is "L".

The memory constitution of the M35040-XXXFP is different from the M35041-XXXFP.

Each of them are shown in Figure 1 and Figure 2.

Bit / Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00_{16}	0	0	CF	REV	BLINK	B	G	R	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮	⋮	CF	Reverse	Blinking	Character color			⋮	Character code						
EF_{16}	0	0	CF	REV	BLINK	B	G	R	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
$F0_{16}$	0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
$F1_{16}$	0	0	0	TEST 2	TEST 1	TEST 0	PLTV	PLTH	SYNCV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
$F2_{16}$	0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
$F3_{16}$	0	0	0	RB	RG	RR	—	B/$\overline{F}$	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
$F4_{16}$	0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
$F5_{16}$	0	0	0	BB	BG	BR	EXP	CVF	BCOL	STOP 1	DSPON	RAMERS	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 1 Memory constitution (M35040-XXXFP)

Bit / Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00_{16}	0	0	CF	REV	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮	⋮	CF	Reverse	Blinking	Character color			Character code							
EF_{16}	0	0	CF	REV	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
$F0_{16}$	0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
$F1_{16}$	0	0	0	TEST 2	TEST 1	TEST 0	PLTV	PLTH	SYNCV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
$F2_{16}$	0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
$F3_{16}$	0	0	0	RB	RG	RR	—	B/$\overline{F}$	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
$F4_{16}$	0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
$F5_{16}$	0	0	0	BB	BG	BR	EXP	CVF	BCOL	STOP 1	DSPON	RAMERS	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 2 Memory constitution (M35041-XXXFP)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen consitution is shown in Figure 3.

Line \ Row	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00_{16}	01_{16}	02_{16}	03_{16}	04_{16}	05_{16}	06_{16}	07_{16}	08_{16}	09_{16}	$0A_{16}$	$0B_{16}$	$0C_{16}$	$0D_{16}$	$0E_{16}$	$0F_{16}$	10_{16}	11_{16}	12_{16}	13_{16}	14_{16}	15_{16}	16_{16}	17_{16}
2	18_{16}	19_{16}	$1A_{16}$	$1B_{16}$	$1C_{16}$	$1D_{16}$	$1E_{16}$	$1F_{16}$	20_{16}	21_{16}	22_{16}	23_{16}	24_{16}	25_{16}	26_{16}	27_{16}	28_{16}	29_{16}	$2A_{16}$	$2B_{16}$	$2C_{16}$	$2D_{16}$	$2E_{16}$	$2F_{16}$
3	30_{16}	31_{16}	32_{16}	33_{16}	34_{16}	35_{16}	36_{16}	37_{16}	38_{16}	39_{16}	$3A_{16}$	$3B_{16}$	$3C_{16}$	$3D_{16}$	$3E_{16}$	$3F_{16}$	40_{16}	41_{16}	42_{16}	43_{16}	44_{16}	45_{16}	46_{16}	47_{16}
4	48_{16}	49_{16}	$4A_{16}$	$4B_{16}$	$4C_{16}$	$4D_{16}$	$4E_{16}$	$4F_{16}$	50_{16}	51_{16}	52_{16}	53_{16}	54_{16}	55_{16}	56_{16}	57_{16}	58_{16}	59_{16}	$5A_{16}$	$5B_{16}$	$5C_{16}$	$5D_{16}$	$5E_{16}$	$5F_{16}$
5	60_{16}	61_{16}	62_{16}	63_{16}	64_{16}	65_{16}	66_{16}	67_{16}	68_{16}	69_{16}	$6A_{16}$	$6B_{16}$	$6C_{16}$	$6D_{16}$	$6E_{16}$	$6F_{16}$	70_{16}	71_{16}	72_{16}	73_{16}	74_{16}	75_{16}	76_{16}	77_{16}
6	78_{16}	79_{16}	$7A_{16}$	$7B_{16}$	$7C_{16}$	$7D_{16}$	$7E_{16}$	$7F_{16}$	80_{16}	81_{16}	82_{16}	83_{16}	84_{16}	85_{16}	86_{16}	87_{16}	88_{16}	89_{16}	$8A_{16}$	$8B_{16}$	$8C_{16}$	$8D_{16}$	$8E_{16}$	$8F_{16}$
7	90_{16}	91_{16}	92_{16}	93_{16}	94_{16}	95_{16}	96_{16}	97_{16}	98_{16}	99_{16}	$9A_{16}$	$9B_{16}$	$9C_{16}$	$9D_{16}$	$9E_{16}$	$9F_{16}$	$A0_{16}$	$A1_{16}$	$A2_{16}$	$A3_{16}$	$A4_{16}$	$A5_{16}$	$A6_{16}$	$A7_{16}$
8	$A8_{16}$	$A9_{16}$	AA_{16}	AB_{16}	AC_{16}	AD_{16}	AE_{16}	AF_{16}	$B0_{16}$	$B1_{16}$	$B2_{16}$	$B3_{16}$	$B4_{16}$	$B5_{16}$	$B6_{16}$	$B7_{16}$	$B8_{16}$	$B9_{16}$	BA_{16}	BB_{16}	BC_{16}	BD_{16}	BE_{16}	BF_{16}
9	$C0_{16}$	$C1_{16}$	$C2_{16}$	$C3_{16}$	$C4_{16}$	$C5_{16}$	$C6_{16}$	$C7_{16}$	$C8_{16}$	$C9_{16}$	CA_{16}	CB_{16}	CC_{16}	CD_{16}	CE_{16}	CF_{16}	$D0_{16}$	$D1_{16}$	$D2_{16}$	$D3_{16}$	$D4_{16}$	$D5_{16}$	$D6_{16}$	$D7_{16}$
10	$D8_{16}$	$D9_{16}$	DA_{16}	DB_{16}	DC_{16}	DD_{16}	DE_{16}	DF_{16}	$E0_{16}$	$E1_{16}$	$E2_{16}$	$E3_{16}$	$E4_{16}$	$E5_{16}$	$E6_{16}$	$E7_{16}$	$E8_{16}$	$E9_{16}$	EA_{16}	EB_{16}	EC_{16}	ED_{16}	EE_{16}	EF_{16}

The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution

REGISTERS DESCRIPTION

(1) Address $F0_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	⓪	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs RGB output blanking. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP9 settings.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	⓪	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	⓪	P2 output (port P2). Port data is set by PTD2.	BLNK1 outputs the blanking of the border size for the G component of RGB output. BLNK1 outputs the blanking of the border size regardless of BLK0 or BLK1.
		1	BLNK1 output. Polarity is set by PTD2.	
3	PTC3	⓪	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	⓪	P4 output (port P4). Port data is set by PTD4.	BLNK2 outputs the blanking of the border size for the B component of RGB output. BLNK2 outputs the blanking of the border size regardless of BLK0 or BLK1.
		1	BLNK2 output. Polarity is set by PTD4.	
5	PTC5	⓪	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0	⓪	"L" output (P0 output) or negative polarity output (BLNK0 output).	Port data control
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1	⓪	"L" output (P1 output) or negative polarity output (R signal output).	
		1	"H" output (P1 output) or positive polarity output (R signal output).	
8	PTD2	⓪	"L" output (P2 output) or negative polarity output (BLNK1 output).	
		1	"H" output (P2 output) or positive polarity output (BLNK1 output).	
9	PTD3	⓪	"L" output (P3 output) or negative polarity output (G signal output).	
		1	"H" output (P3 output) or positive polarity output (G signal output).	
A	PTD4	⓪	"L" output (P4 output) or negative polarity output (BLNK2 output).	
		1	"H" output (P4 output) or positive polarity output (BLNK2 output).	
B	PTD5	⓪	"L" output (P5 output) or negative polarity output (B signal output).	
		1	"H" output (P5 output) or positive polarity output (B signal output).	
C	SEPV	⓪	Synchronization separated circuit OFF.	Vertical synchronization signal is separated from composite synchronization signal.
		1	Synchronization separated circuit ON.	

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address $F1_{16}$

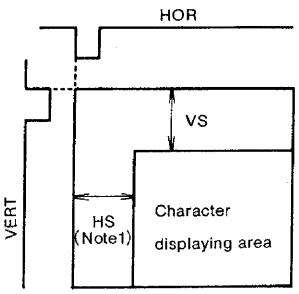
DA	Register	Contents		Remarks
		Status	Function	
0	PTD6	⓪	"L" output (port P6)	Port data control (port P6 to P9)
		1	"H" output (port P6)	
1	PTD7	⓪	"L" output (port P7)	
		1	"H" output (port P7)	
2	PTD8	⓪	"L" output (port P8)	
		1	"H" output (port P8)	
3	PTD9	⓪	"L" output (port P9)	
		1	"H" output (port P9)	
4	SPACE0	⓪	SPACE 2 1 0 / Number of Lines and Space (Ⓢ represents space): 0 0 0 → 10; 0 0 1 → 5 Ⓢ 5; 0 1 0 → 5 Ⓢ Ⓢ 5; 0 1 1 → 5 Ⓢ Ⓢ Ⓢ 5; 1 0 0 → 1 Ⓢ 8 Ⓢ 1; 1 0 1 → 2 Ⓢ 6 Ⓢ 2; 1 1 0 → 3 Ⓢ 4 Ⓢ 3; 1 1 1 → 4 Ⓢ 2 Ⓢ 4. Ⓢ represents one line worth of spaces.	Leave one line worth of space in the vertical direction. For example, 5 Ⓢ 5 indicates two sets of 5 lines with a line of spaces between lines 5 and 6. A line is 18 ×N horizontal scan lines. N is determined by the character size in the vertical direction as follows: ×1 N=1 ×2 N=2 ×3 N=3 ×4 N=4
		1		
5	SPACE1	⓪		
		1		
6	SPACE2	⓪		
		1		
7	SYNCV	⓪	Output after port output is set to PTD9.	Selects whether port P9 output is synchronized with vertical synchronization.
		1	Output after synchronizing port output to V.	
8	PLTH	⓪	Negative polarity input (HOR pin).	Sets the polarity of HOR pin.
		1	Positive polarity input (HOR pin).	
9	PLTV	⓪	Negative polarity input (VERT pin).	Sets the polarity of VERT pin.
		1	Positive polarity input (VERT pin).	
A	TEST0	⓪	It should be fixed to "0".	
		1	Can not be used.	
B	TEST1	⓪	It should be fixed to "0".	
		1	Can not be used.	
C	TEST2	⓪	It should be fixed to "0".	
		1	Can not be used.	

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(3) Address $F2_{16}$

DA	Register	Contents: Status	Contents: Function	Remarks
0	HP0 (LSB)	⓪	If HS is the horizontal display start location, $HS = T \times (4 \sum_{n=0}^{5} 2^n HP_n + N)$. T : The oscillation cycle of oscillator OSC1, 2	Horizontal display start location is specified using the 6 bits from HP5 to HP0. Note : HP5 to 0 = (000000_2) and (000001_2) setting is forbidden
		1		
1	HP1	⓪		
		1		
2	HP2	⓪		
		1		
3	HP3	⓪		
		1		
4	HP4	⓪		
		1		
5	HP5 (MSB)	⓪		
		1		
6	VP0 (LSB)	⓪	If VS is the vertical display start location, $VS = H \times (4 \sum_{n=0}^{5} 2^n VP_n + 3)$. H : Cycle with the horizontal synchronizing pulse	The vertical start location is specified using the 6 bits from VP5 to VP0. Note1. In case of B/$\overline{F}$ register is "0".
		1		
7	VP1	⓪		
		1		
8	VP2	⓪		
		1		
9	VP3	⓪		
		1		
A	VP4	⓪		
		1		
B	VP5 (MSB)	⓪		
		1		
C	BLINK2	⓪	Division of vertical synchronization signal into 1/64. Cycleapproximately 1 second	Blinking cycle can be altered
		1	Division of vertical synchronization signal into 1/32. Cycleapproximately 0.5 second	

HSZ11	HSZ10	N
HSZ21	HSZ20	
0	0	9
0	1	10
1	0	11
1	1	12



Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(4) Address $F3_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HSZ10</td><td>⓪
1</td><td rowspan="2">HSZ10 \ HSZ11 | 0 | 1
0 | 1T/1dot | 2T/1dot
1 | 3T/1dot | 4T/1dot</td><td rowspan="2">Character size setting in the horizontal direction for the first line.</td></tr>
<tr><td>1</td><td>HSZ11</td><td>⓪
1</td></tr>
<tr><td>2</td><td>HSZ20</td><td>⓪
1</td><td rowspan="2">HSZ20 \ HSZ21 | 0 | 1
0 | 1T/1dot | 2T/1dot
1 | 3T/1dot | 4T/1dot</td><td rowspan="2">Character size setting in the horizontal direction for the 2nd line to 10th line.</td></tr>
<tr><td>3</td><td>HSZ21</td><td>⓪
1</td></tr>
<tr><td>4</td><td>VSZ10</td><td>⓪
1</td><td rowspan="2">VSZ10 \ VSZ11 | 0 | 1
0 | 1H/1dot | 2H/1dot
1 | 3H/1dot | 4H/1dot</td><td rowspan="2">Character size setting in the vertical direction for the first line.</td></tr>
<tr><td>5</td><td>VSZ11</td><td>⓪
1</td></tr>
<tr><td>6</td><td>VSZ20</td><td>⓪
1</td><td rowspan="2">VSZ20 \ VSZ21 | 0 | 1
0 | 1H/1dot | 2H/1dot
1 | 3H/1dot | 4H/1dot</td><td rowspan="2">Character size setting in the vertical direction for the 2nd line to 10th line.</td></tr>
<tr><td>7</td><td>VSZ21</td><td>⓪
1</td></tr>
<tr><td>8</td><td>B/$\overline{F}$</td><td>⓪
1</td><td>Synchronize with the leading edge of horizontal synchronazation.
Synchronize with the trailing edge of horizontal synchronazation.</td><td>Synchronize with the front porch or back porch of the horizontal synchronazation signal.</td></tr>
<tr><td>9</td><td>—</td><td>⓪
1</td><td>It should be fixed to "0".
Can not be used.</td><td></td></tr>
<tr><td>A</td><td>RR</td><td>⓪
1</td><td rowspan="3">RB | RG | RR | Color
0 | 0 | 0 | Black
0 | 0 | 1 | Red
0 | 1 | 0 | Green
0 | 1 | 1 | Yellow
1 | 0 | 0 | Blue
1 | 0 | 1 | Magenta
1 | 1 | 0 | Cyan
1 | 1 | 1 | White</td><td rowspan="3">Sets the color of all blankings.</td></tr>
<tr><td>B</td><td>RG</td><td>⓪
1</td></tr>
<tr><td>C</td><td>RB</td><td>⓪
1</td></tr>
</table>

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(5) Address $F4_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	⓪	Line 1 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 1.
		1	Line 1 is in a different display mode (Note 2).	
1	DSP1	⓪	Line 2 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 2.
		1	Line 2 is in a different display mode (Note 2).	
2	DSP2	⓪	Line 3 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 3.
		1	Line 3 is in a different display mode (Note 2).	
3	DSP3	⓪	Line 4 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 4.
		1	Line 4 is in a different display mode (Note 2).	
4	DSP4	⓪	Line 5 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 5.
		1	Line 5 is in a different display mode (Note 2).	
5	DSP5	⓪	Line 6 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 6.
		1	Line 6 is in a different display mode (Note 2).	
6	DSP6	⓪	Line 7 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 7.
		1	Line 7 is in a different display mode (Note 2).	
7	DSP7	⓪	Line 8 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 8.
		1	Line 8 is in a different display mode (Note 2).	
8	DSP8	⓪	Line 9 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 9.
		1	Line 9 is in a different display mode (Note 2).	
9	DSP9	⓪	Line 10 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 10.
		1	Line 10 is in a different display mode (Note 2).	
A	FR	⓪	FB FG FR Color: 0 0 0 Black; 0 0 1 Red; 0 1 0 Green; 0 1 1 Yellow; 1 0 0 Blue; 1 0 1 Magenta; 1 1 0 Cyan; 1 1 1 White	Sets the blanking color of the border size.
		1		
B	FG	⓪		
		1		
C	FB	⓪		
		1		

Note1 : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
Note2 : See the display form.

(6) Address $F5_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>BLINK0</td><td>0
1</td><td rowspan="2"><table><tr><th>BLINK1 \ BLINK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking OFF</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table></td><td rowspan="2">Blinking duty ratio can be altered</td></tr>
<tr><td>1</td><td>BLINK1</td><td>0
1</td></tr>
<tr><td>2</td><td>BLK0</td><td>0
1</td><td rowspan="2"><table><tr><th>BLK1 \ BLK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blanking OFF</td><td>Character size</td></tr><tr><td>1</td><td>Border size</td><td>Matrix-outline size</td></tr></table></td><td rowspan="2">Display mode variable</td></tr>
<tr><td>3</td><td>BLK1</td><td>0
1</td></tr>
<tr><td>4</td><td>RAMERS</td><td>0
1</td><td>RAM not erased
RAM erased</td><td>There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>5</td><td>DSPON</td><td>0
1</td><td>Display OFF
Display ON</td><td>Display can be altered.</td></tr>
<tr><td>6</td><td>STOP1</td><td>0
1</td><td>Oscillation of OSC1, OSC2 for display
Stop the oscillation of OSC1, OSC2 for display</td><td>OSC1 and OSC2 oscillation switching. To stop the oscillation, set $\overline{CS}$ pin to "H" level and DSPON (address $F5_{16}$) to "0".</td></tr>
<tr><td>7</td><td>BCOL</td><td>0
1</td><td>Blanking of BLK0, BLK1
All raster blanking</td><td>Sets all raster blanking</td></tr>
<tr><td>8</td><td>CVF</td><td>0
1</td><td>R, G, B, BLNK0, BLNK1, and BLNK2 signal output
R, G, B, BLNK0, CO, and BLNK signal output</td><td>CO and BLNK are output in association with CF bits in the addresses 00_{16} to EF_{16} of the display RAM (DAD).</td></tr>
<tr><td>9</td><td>EXP</td><td>0
1</td><td>BLNK0 signal outputs blanking regardless of the character color
Cuts BLNK0 signal for black character.</td><td>Select whether to output BLNK0 signal or cut in case of black character.</td></tr>
<tr><td>A</td><td>BR</td><td>0
1</td><td rowspan="3"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="3">Sets the blanking color of the Matrix-outline size.</td></tr>
<tr><td>B</td><td>BG</td><td>0
1</td></tr>
<tr><td>C</td><td>BB</td><td>0
1</td></tr>
</table>

DISPLAY FORM 1

The M35040-XXXFP has blanking 0 to blanking 2 function.
Table 1 shows display form of blanking 0.
Table 2 shows display form of blanking 1 and blanking 2.

Table 1. Display form of blanking 0

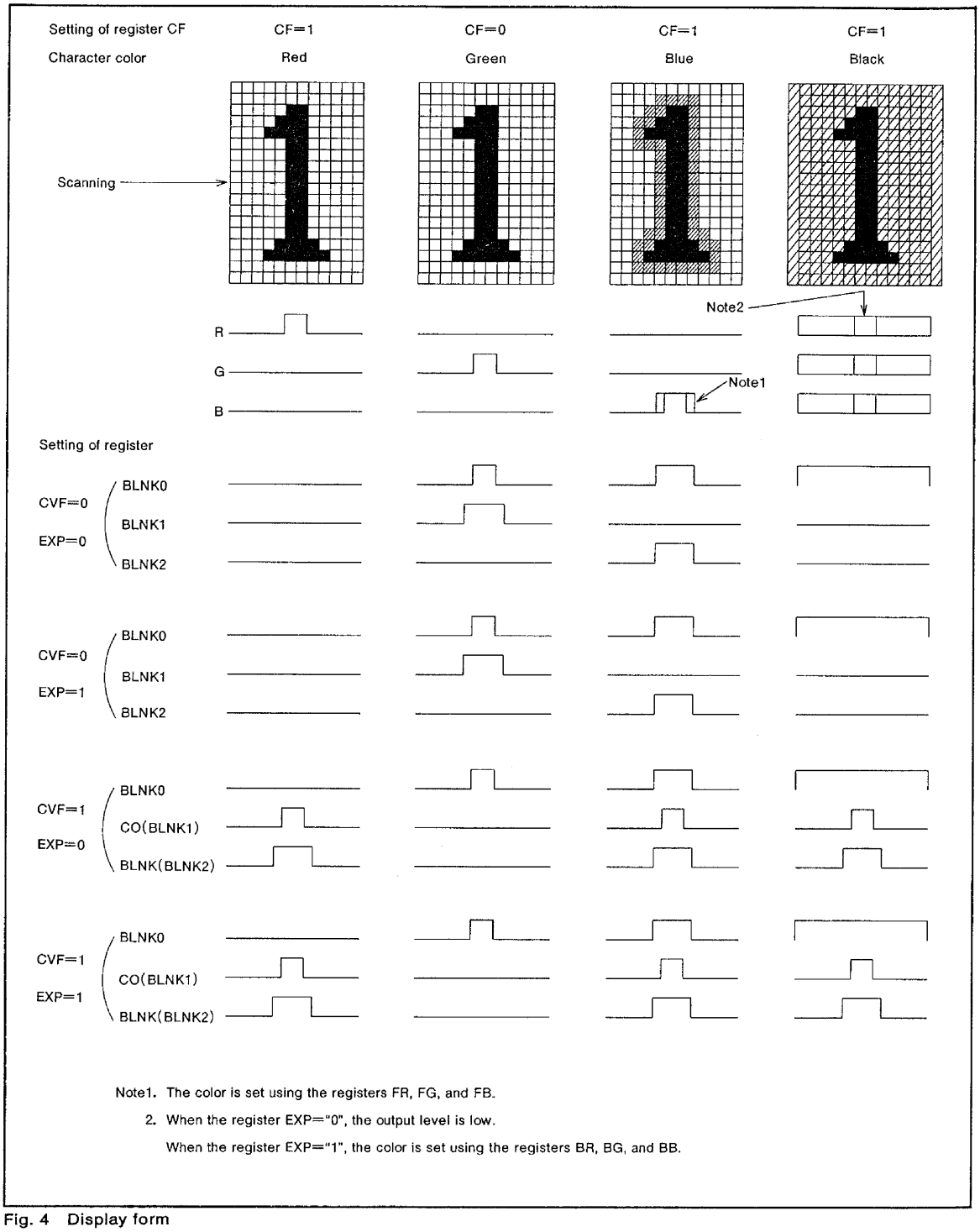
BCOL	Standard blanking		When the all of registers	When some of registers DSPi are set to "1".		BLNK0 output
	BLK1	BLK0	DSPi are set to "0".	DSPi=0	DSPi=1	
0	0	0	OFF	Border F (RGB)	Character	When the blanking status is blanking off, the BLNK0 output is outline output. B (RGB)
0	0	1	Character	Character	Border F (RGB)	
0	1	0	Border F (RGB)	Border F (RGB)	Matrix-outline B (RGB)	
0	1	1	Matrix-outline B (RGB)	Matrix-outline B (RGB)	Character	
1	0	0	Character	Border F (RGB)	Character	All raster blanking
1	0	1	Character	Character	Border F (RGB)	All raster blanking
1	1	0	Border F (RGB)	Border F (RGB)	Matrix-outline B (RGB)	All raster blanking
1	1	1	Matrix-outline B (RGB)	Matrix-outline B (RGB)	Character	All raster blanking

Note : i=0 to 9

Table 2. Display form of blanking 1 and blanking 2

BLNK1 output	Blanking for G bit (display RAM)	Border
BLNK2 output	Blanking for B bit (display RAM)	Border

Display form 2



Note1. The color is set using the registers FR, FG, and FB.

2. When the register EXP="0", the output level is low.

When the register EXP="1", the color is set using the registers BR, BG, and BB.

Fig. 4 Display form

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting at M35040-XXXFP is shown in Figure 5 and example of data setting at M35041-XXXFP is shown in Figure 6.

No.	Memory Contents		DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/Data	Addition																
1	Address ($F5_{16}$)	Setting to address	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1
2	Data ($F5_{16}$)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
3	Data (00_{16})	Setting to display RAM (addresses 00_{16} to EF_{16}) and registers (addresses $F0_{16}$ to $F5_{16}$)	0	0	CF	REV	BLINK	B	G	R	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
4	Data (01_{16})		0	0	CF	REV	BLINK	B	G	R	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮		⋮															
242	Data (EF_{16})		0	0	CF	REV	BLINK	B	G	R	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
243	Data ($F0_{16}$)		0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
244	Data ($F1_{16}$)		0	0	0	0	0	0	PLTV	PLTH	SYNCV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
245	Data ($F2_{16}$)		0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
246	Data ($F3_{16}$)		0	0	0	RB	RG	RR	0	B/$\overline{F}$	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data ($F4_{16}$)		0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data ($F5_{16}$)		0	0	0	BB	BG	BR	EXP	CVF	0	0	1	0	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 5 Example of data setting at M35040-XXXFP by the serial input function

No.	Memory Contents		DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0
	Address/Data	Addition																
1	Address ($F5_{16}$)	Setting to address	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1
2	Data ($F5_{16}$)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
3	Data (00_{16})	Setting to display RAM (addresses 00_{16} to EF_{16}) and registers (addresses $F0_{16}$ to $F5_{16}$)	0	0	CF	REV	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
4	Data (01_{16})		0	0	CF	REV	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	⋮		⋮															
242	Data (EF_{16})		0	0	CF	REV	BLINK	B	G	R	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
243	Data ($F0_{16}$)		0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
244	Data ($F1_{16}$)		0	0	0	0	0	0	PLTV	PLTH	SYNCV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
245	Data ($F2_{16}$)		0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
246	Data ($F3_{16}$)		0	0	0	RB	RG	RR	0	B/$\overline{F}$	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
247	Data ($F4_{16}$)		0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
248	Data ($F5_{16}$)		0	0	0	BB	BG	BR	EXP	CVF	0	0	1	0	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 6 Example of data setting at M35041-XXXFP by the serial input function

SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.
(2) The address consists of 16 bits.
(3) The data consists of 16 bits.
(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

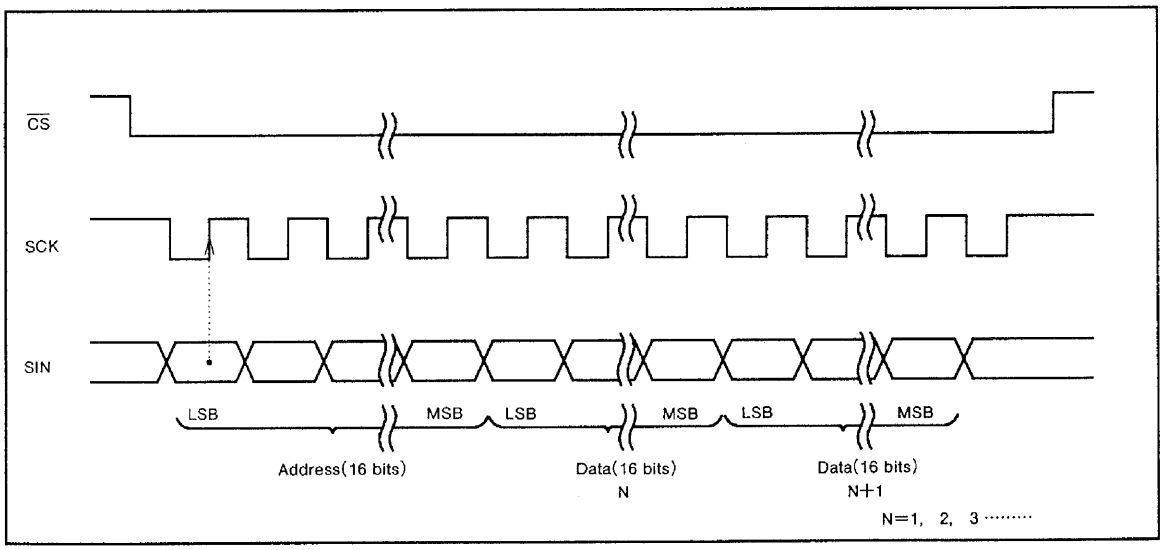


Fig. 7 Serial input timing

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

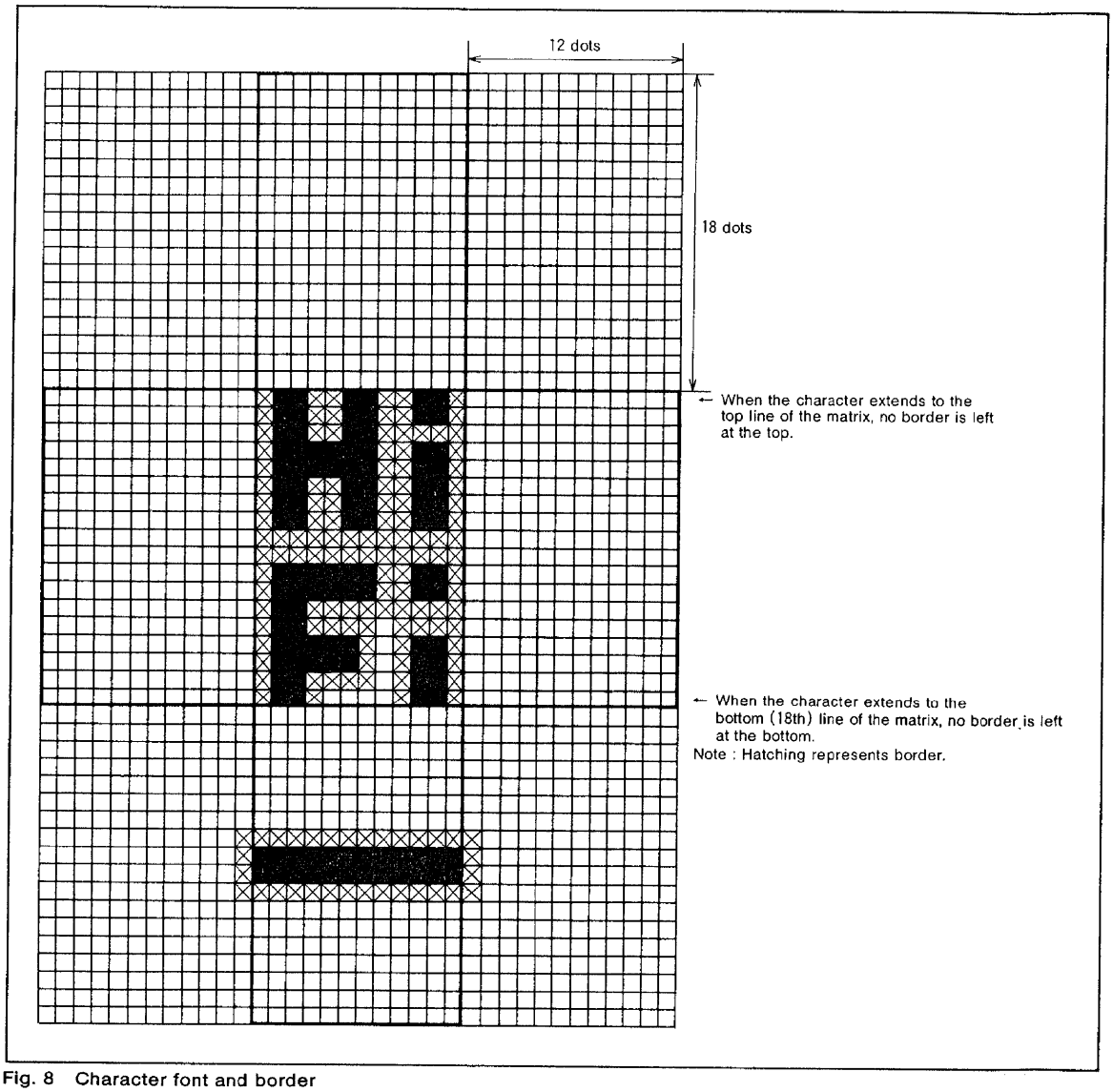


Fig. 8 Character font and border

Character code FF_{16} is fixed as blank, without a background.

Timing Requirements (T_a=−20℃ to +70℃, V_{DD}=5±0.5V, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 9
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	μs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

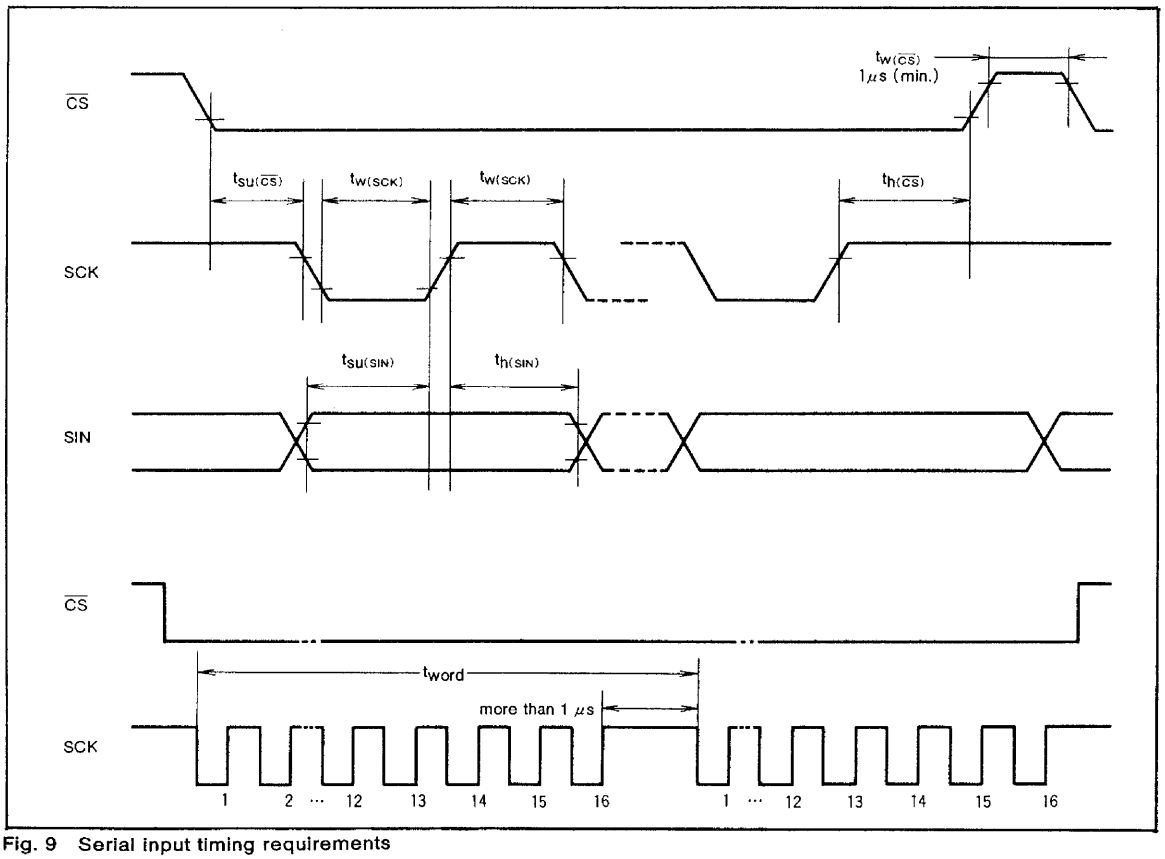


Fig. 9 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	−0.3 to 6.0	V
V_I	Input voltage		$V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$	V
V_O	Output voltage		$V_{SS} \leqq V_O \leqq V_{DD}$	V
P_d	Power dissipation	T_a=25℃	150	mW
Topr	Operating temperature		−20 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{DD}=5V, T_a=−20 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	3.0	5.0	5.5	V
V_{IH}	"H" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT	$0.8V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT	0	0	$0.2V_{DD}$	V
f_{OSC1}	Oscillating frequency for display	6.3	7.0	7.7	MHz

ELECTRICAL CHARACTERISTICS (V_{DD}= 5 V, f_{OSC1}=7.0MHz, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	T_a=−20 to 70℃	3.0	5.0	5.5	V
I_{DD}	Supply current	V_{DD}=5.5V	—	10	20	mA
V_{OH}	"H" level output voltage, P0 to P9	V_{DD}=4.5V, I_{OH}=0.4mA	3.5	—	—	V
V_{OL}	"L" level output voltage, P0 to P9	V_{DD}=4.5V, I_{OL}=0.4mA	—	—	0.4	V
R_I	Pull-up resistance SCK, $\overline{AC}$, $\overline{CS}$, SIN		10	30	100	kΩ

Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35040-XXXFP/M35041-XXXFP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 10.

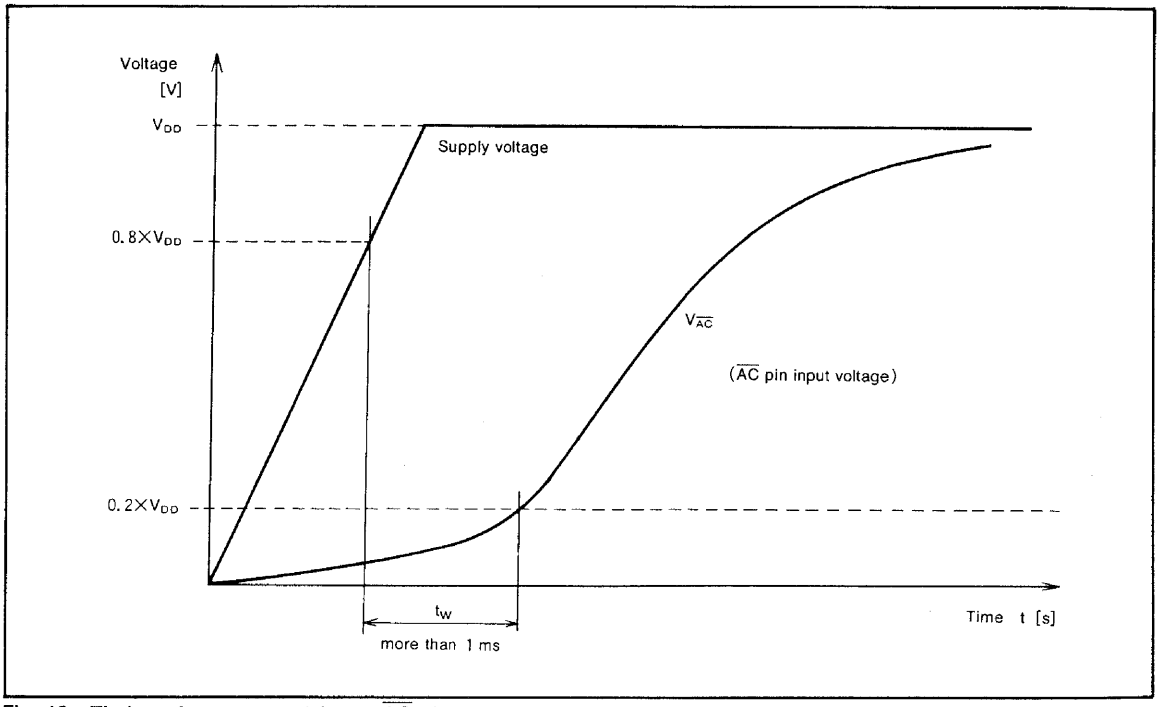


Fig. 10 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35040-XXXFP/ M35041-XXXFP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD} pin and V_{SS} pin using a heavy wire.

STANDARD ROM TYPE : M35040-001FP

M35040-001FP is a standard ROM type of M35040-XXXFP.
The character patterns are fixed to the contents of Figure 11 to 13.

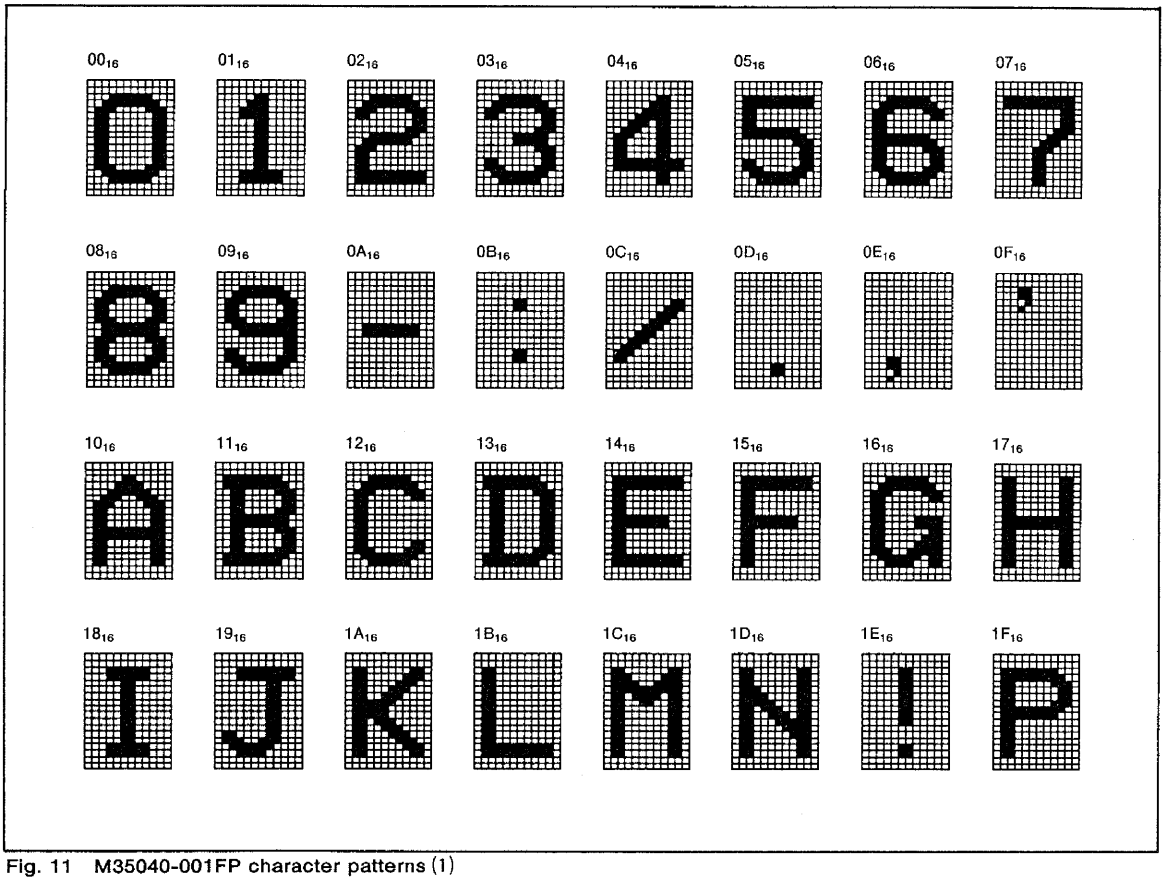


Fig. 11 M35040-001FP character patterns (1)

Fig. 12 M35040-001FP character patterns (2)

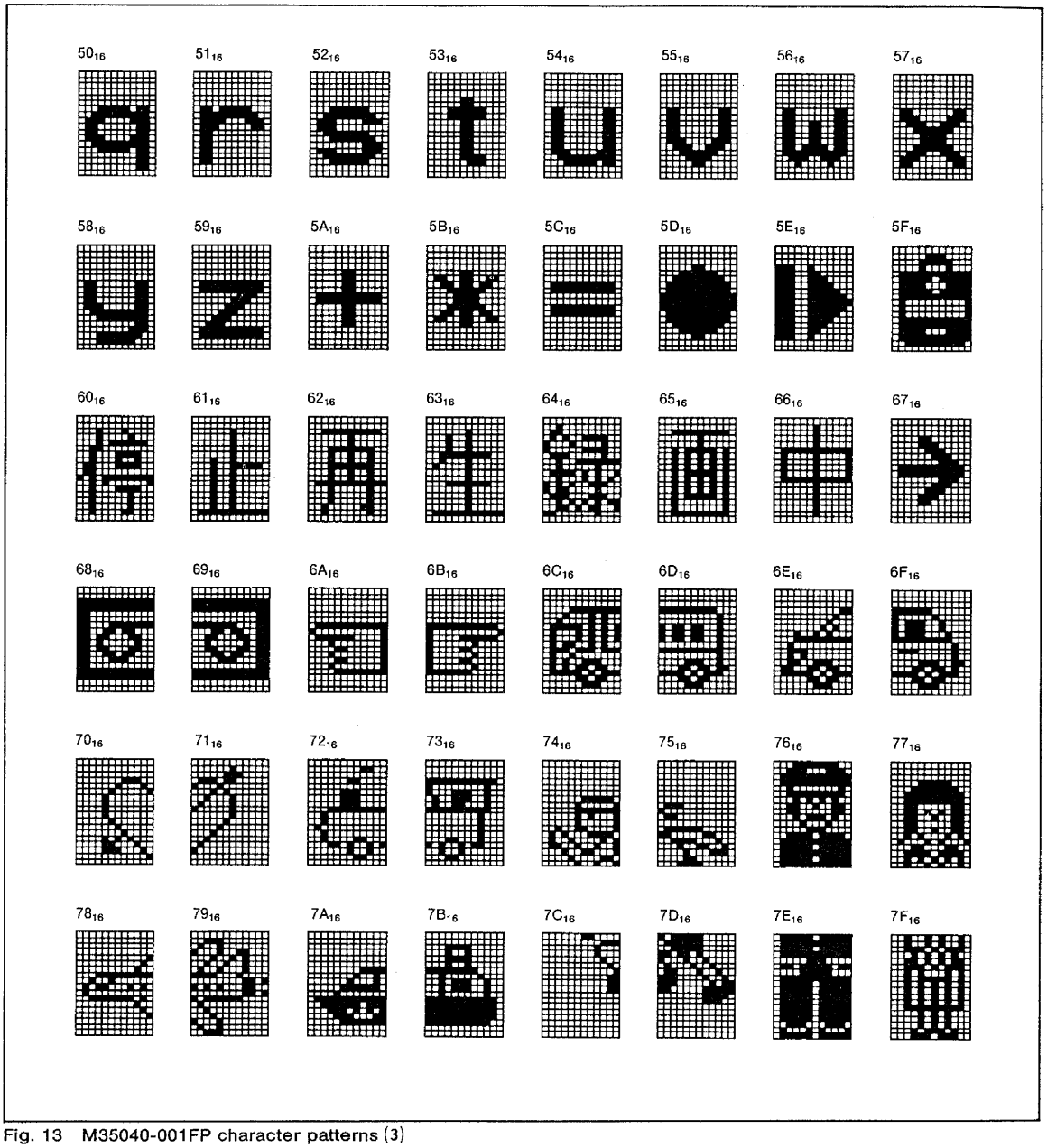


Fig. 13 M35040-001FP character patterns (3)

STANDARD ROM TYPE : M35041-001FP

M35041-001FP is a standard ROM type of M35041-XXXFP.
The character patterns are fixed to the contents of Figure 14 to 19.

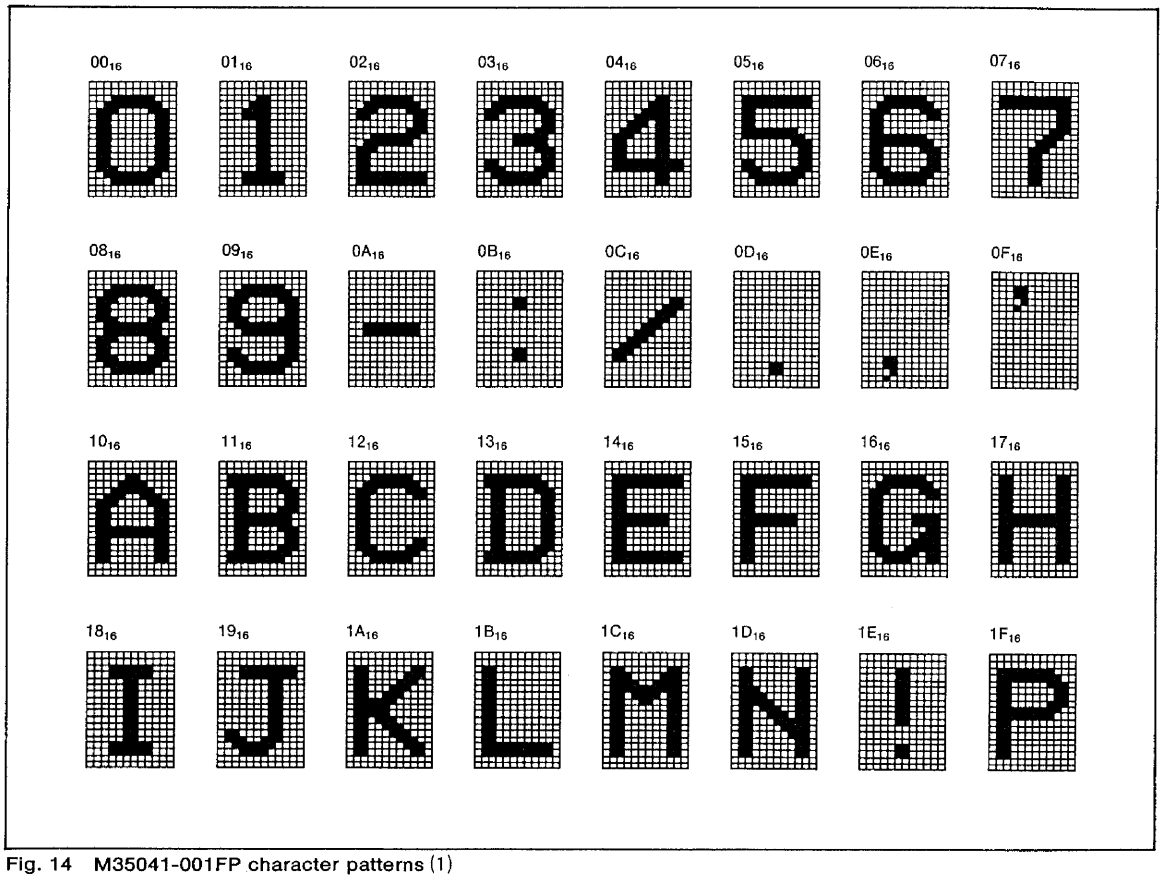


Fig. 14 M35041-001FP character patterns (1)

Fig. 15 M35041-001FP character patterns (2)

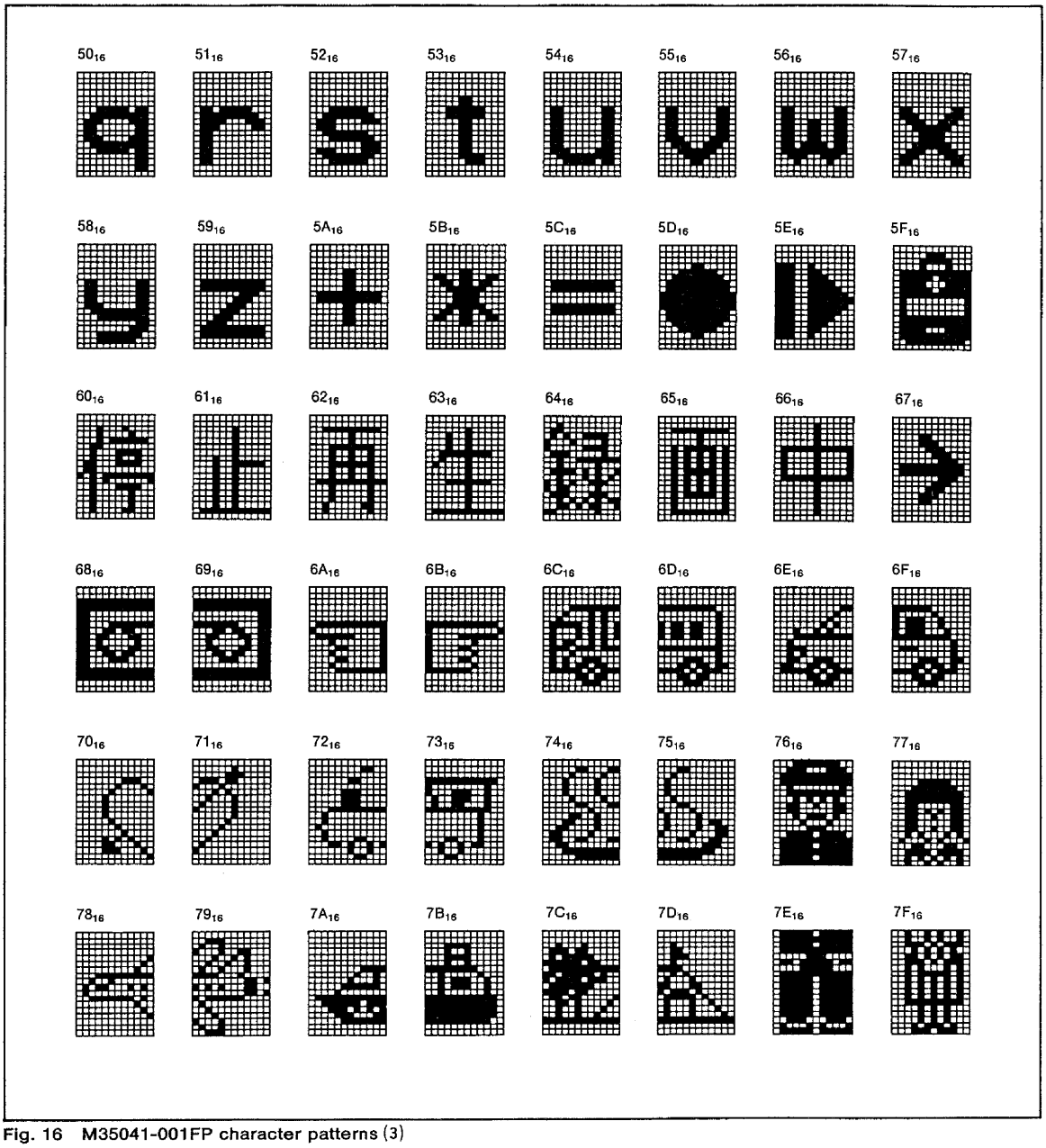


Fig. 16 M35041-001FP character patterns (3)

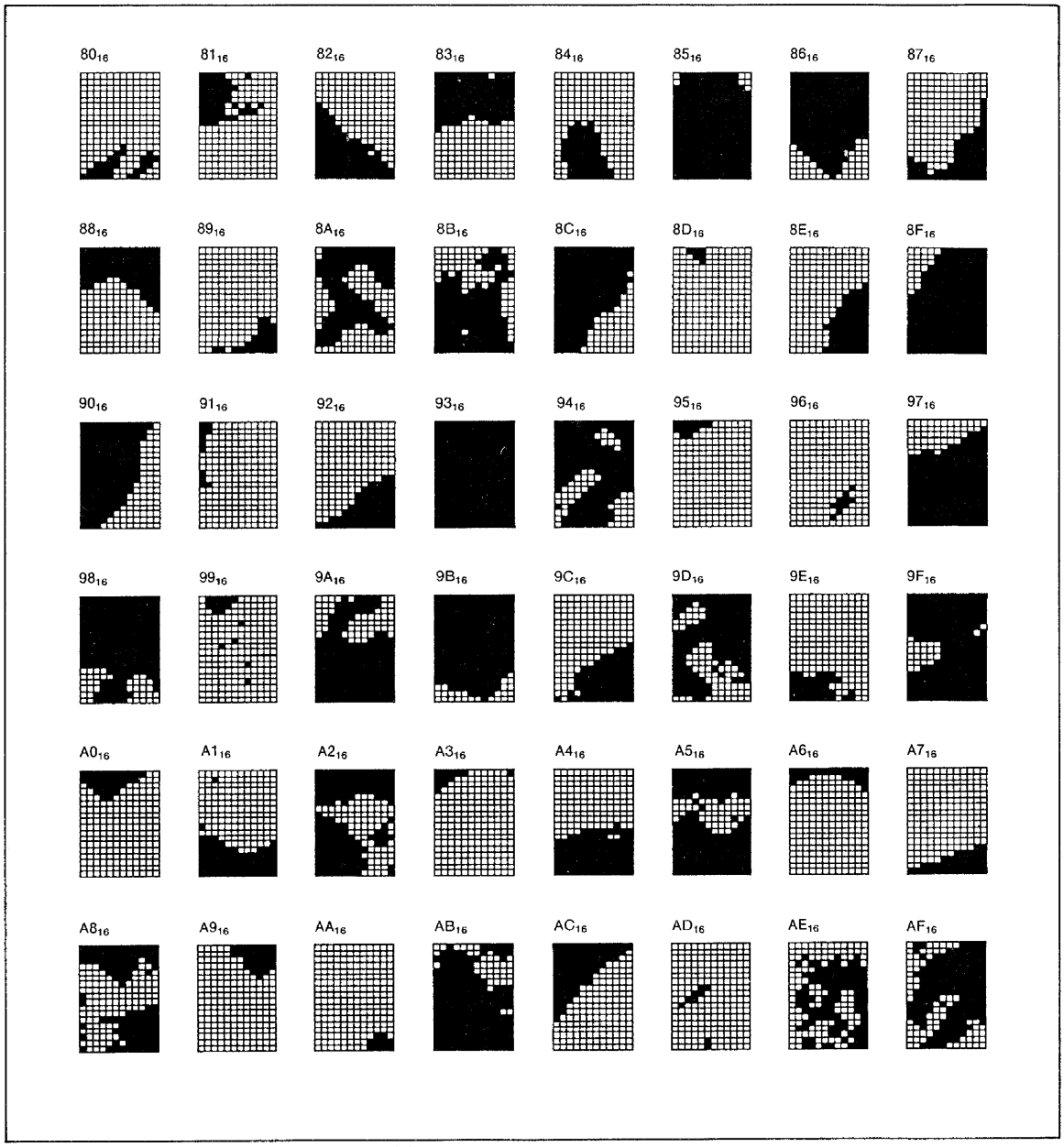


Fig. 17 M35041-001FP character patterns (4)

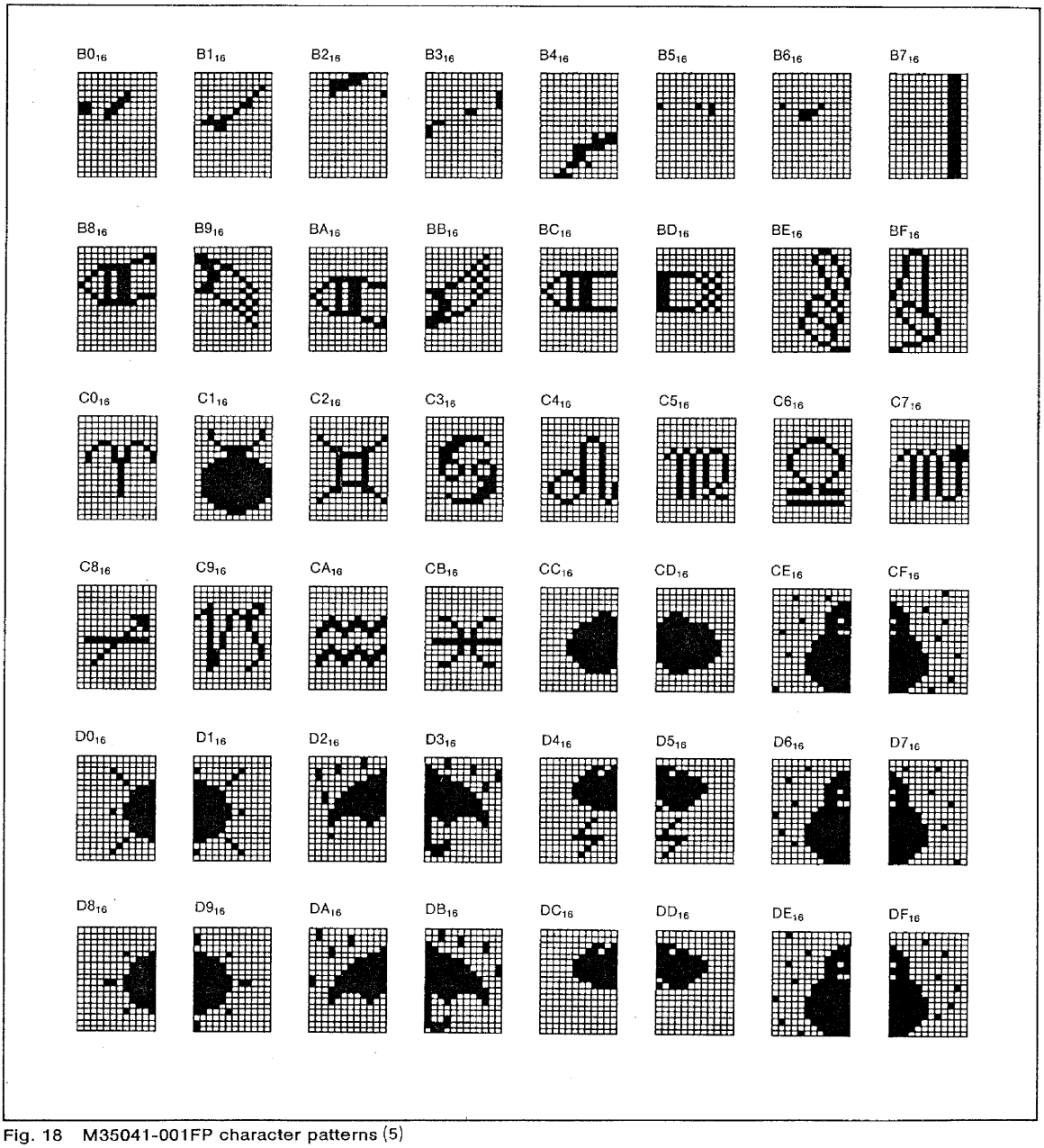


Fig. 18 M35041-001FP character patterns (5)

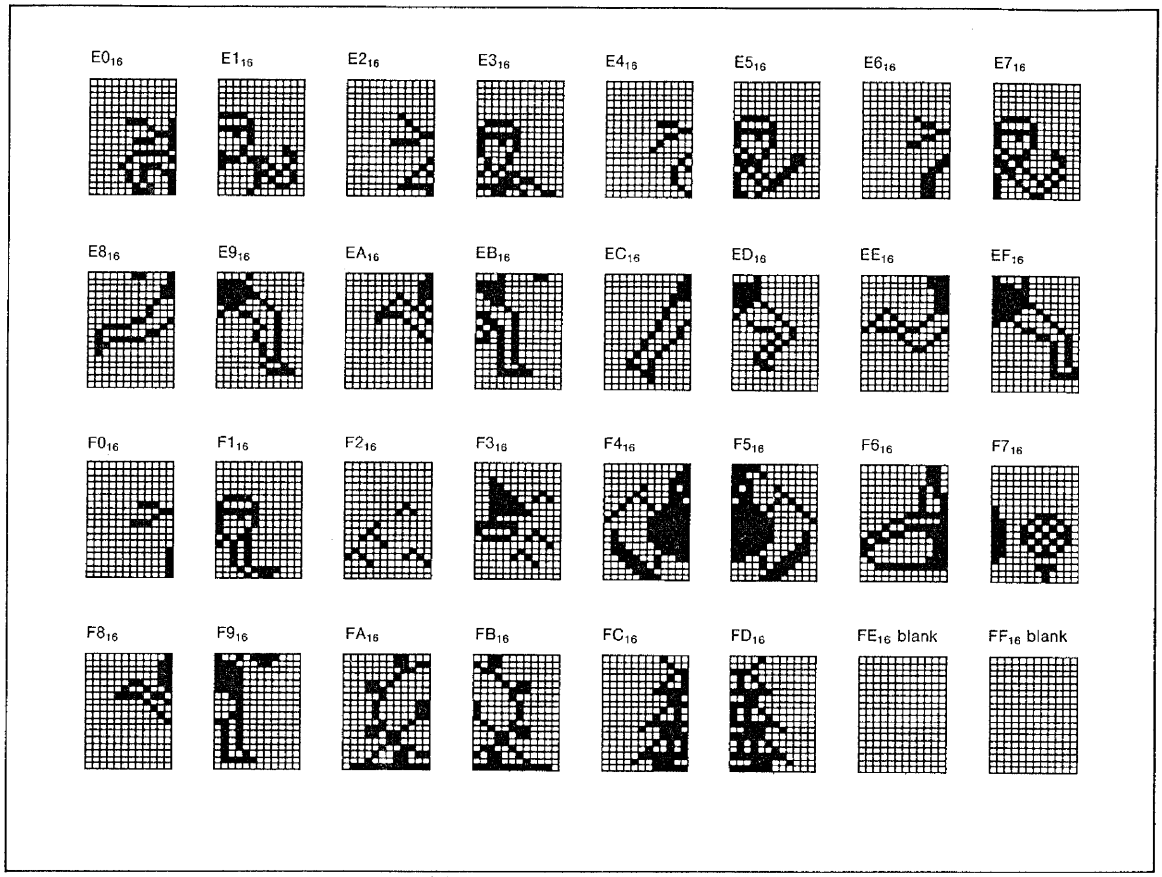


Fig. 19 M35041-001FP character patterns (6)