

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1 DRAM Dual-Ported Controllers

This document contains Product specifications for the 74F764/765 and 74F764-1/765-1, and Preliminary specification for the 74F764A/765A

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing, and refresh
- 9 address output pins allow direct control of up to 256K dynamic RAMS
- External address multiplexing enables control of 1Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- F764/F764A/F764-1 have on-chip 18-bit address input latch
- F764/765, F764-1/765-1 allow control of dynamic RAMs with row access times down to 40ns
- F764A/765A allow control of dynamic RAMs with row access times down to 30ns
- F764/765, F764A/765A output drivers designed for incident wave switching
- F764-1/765-1 output drivers designed for first reflected wave switching

DESCRIPTION

The 74F764/765 DRAM Dual-ported Controller is a High-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, micro-

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F764/765	150MHz	150mA
74F764A/765A	175MHz	150mA
74F764-1/765-1	150MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	74F764N, 74F765N, 74F764AN, 74F765AN, 74F764-1N, 74F765-1N
PLCC-44	74F764A, 74F765A, 74F764AA, 74F765AA, 74F764-1A, 74F765-1A

controllers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F764 vs 74F765

The F764, though functionally and pin-to-pin compatible with the F765, differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

74F764/765 vs 74F764A/765A

The 74F764A/765A is a faster version of the F764/765. The F764/765, rated at a maximum clock frequency of 100MHz, can control dynamic RAMs with row access times down to 40ns. The F764A/765A devices on the other

hand are rated at 150MHz which translates to control of 30ns dynamic RAMs.

74F764/765, 74F764A/765A vs 74F764-1/765-1

The 74F764-1/765-1, though as fast as the 74F764/765, differs from the 74F764/765 and 74F764A/765A in the following respects:

- they reduce the row address hold time by half-a-clock cycle, and
- their outputs are optimized for first reflected wave switching as opposed to incident wave switching.

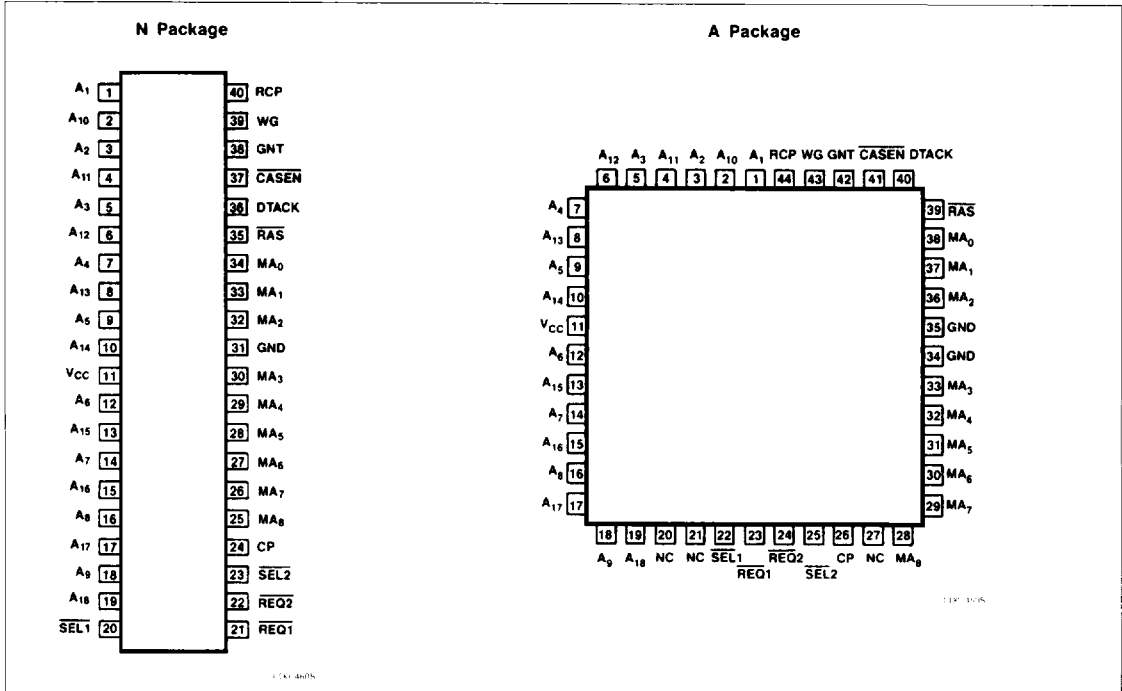
The specialized outputs eliminate the need for signal terminations in essentially all applications.

All devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

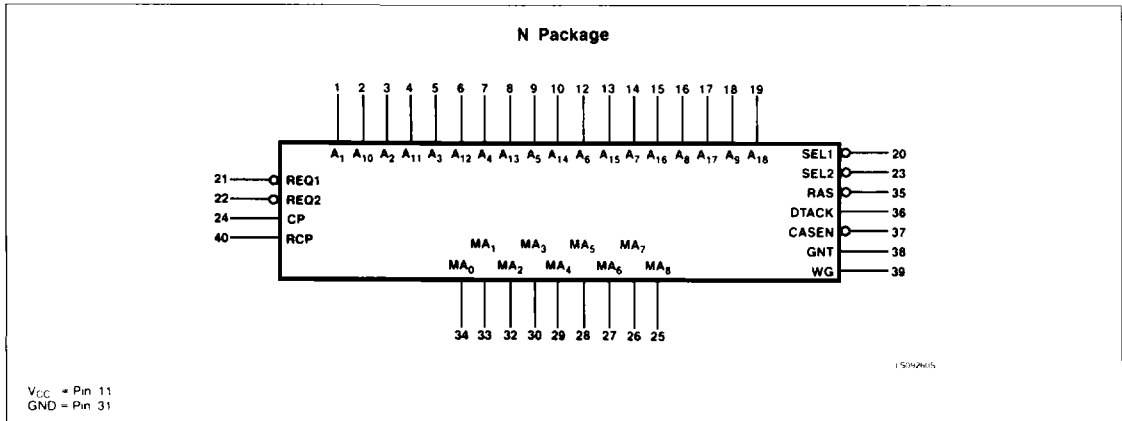
DRAM Dual-Ported Controllers

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PIN CONFIGURATION



LOGIC SYMBOL



DRAM Dual-Ported Controllers

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PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A ₁	1	1	I	Address inputs used to generate memory row address
A ₂	3	3	I	
A ₃	5	5	I	
A ₄	7	7	I	
A ₅	9	9	I	
A ₆	12	12	I	
A ₇	14	14	I	
A ₈	16	16	I	
A ₉	18	18	I	
A ₁₀	2	2	I	Address inputs used to generate memory column address
A ₁₁	4	4	I	
A ₁₂	6	6	I	
A ₁₃	8	8	I	
A ₁₄	10	10	I	
A ₁₅	13	13	I	
A ₁₆	15	15	I	
A ₁₇	17	17	I	
A ₁₈	19	19	I	
REQ ₁	21	23	I	Memory access request from Microprocessor 1
REQ ₂	22	24	I	Memory access request from Microprocessor 2
CP	24	26	I	Clock input which determines the master timing
RCP	40	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
SEL ₁	20	22	O	Select signal is activated in response to active REQ ₁ input, indicating selection of Microprocessor 1
V _{CC}	11	11		Power supply +5V ± 10%
GND	31	34 35		Ground
SEL ₂	23	25	O	Select signal is activated in response to active REQ ₂ input, indicating selection of Microprocessor 2
MA ₀	34	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA ₁	33	37	O	
MA ₂	32	36	O	
MA ₃	30	33	O	
MA ₄	29	32	O	
MA ₅	28	31	O	
MA ₆	27	30	O	
MA ₇	26	29	O	
MA ₈	25	28	O	
GNT	38	42	O	Grant output, activated upon start of a memory access cycle
RAS	35	39	O	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the RAS inputs of the DRAMs)
WG	39	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
CASEN	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

ARCHITECTURE

The 74F764/765 DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F764/765 arbitration logic is divided into two stages. The first stage controls which one of the two REQ inputs will be serviced by activating the corresponding SEL output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the REQ₁ and REQ₂ inputs on different edges of the CP clock. REQ₁ is sampled on the rising edge and REQ₂ on the falling edge (refer to Figures 1 - 4).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at

the end of every refresh cycle, and provides the refresh address.

Since SEL outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the SEL outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock for the F764/765 and F764A/765A should be set equal to: (T_{ras}(of the DRAM) + 16 - 5)/4ns plus any system guard-band required.

For the F764-1/765-1 the CP clock input period should be equal to: (T_{ras}(of the DRAM) + 22 - 10)/4ns plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate REQ input. If a refresh cycle is not in process and the other request input is not active, the SEL output corresponding to the active REQ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If

however, a refresh cycle is in process, and there is only one active REQ input, the SEL output corresponding to the active input REQ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 10, 11, 14 and 15).

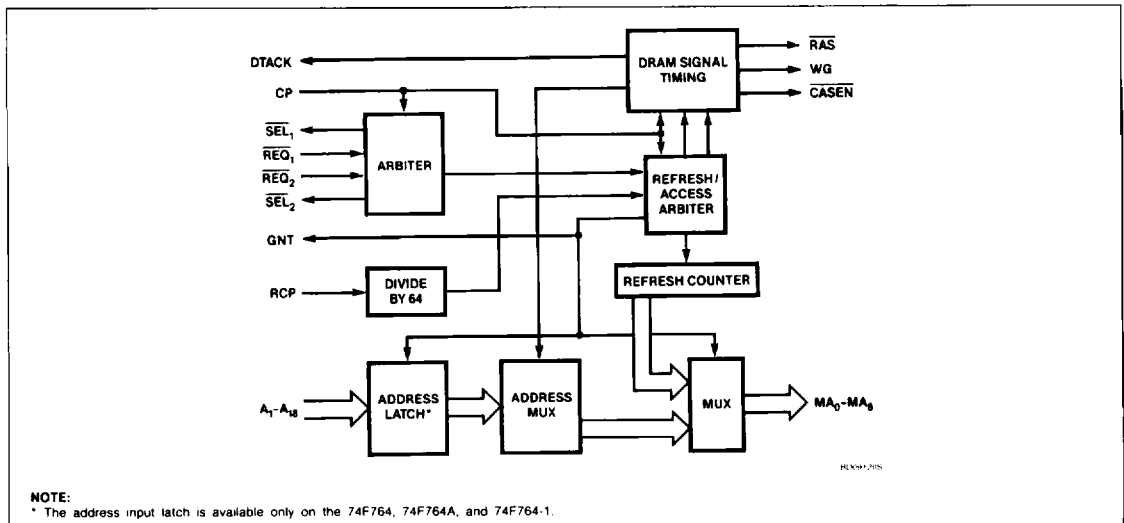
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the SEL output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the SEL output corresponding to the awaiting REQ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the A₁ - A₁₈ address inputs to the 'F764/F764A/F764-1 are latched internally and the A₁ - A₉ signals are propagated to the MA₀ - MA₈ outputs. The address inputs are not latched by the 'F765/F765A/F765-1 and therefore, A₁ - A₉ inputs propagate directly to the MA₀ - MA₈ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the RAS output is asserted.

BLOCK DIAGRAM



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One clock cycle later, the $A_{10} - A_{18}$ latch outputs on the 'F764/F764A or $A_{10} - A_{18}$ inputs to the 'F765/F765A are selected and propagated to the $MA_0 - MA_8$ outputs. This occurs half a clock cycle earlier on the F764-1/765-1 (refer to Figures 3 and 4). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

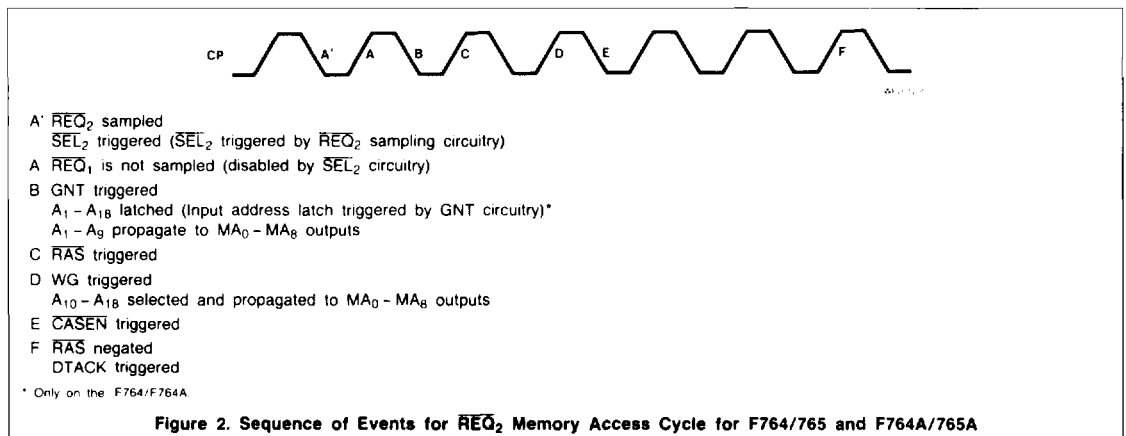
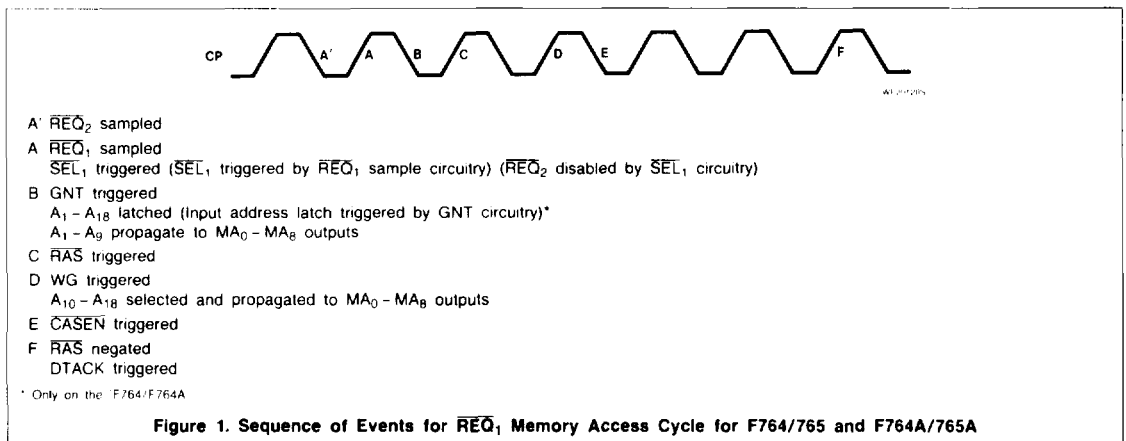
A half-clock cycle is again allowed for the $A_{10} - A_{18}$ signals to propagate and stabilize. \overline{CASEN} then becomes valid. \overline{CASEN} can be used as \overline{CAS} output or decoded with Higher-order address signals to produce multiple

\overline{CAS} signals. After \overline{CASEN} is valid, the controller will wait for $2\frac{1}{2}$ clock cycles before negating \overline{RAS} , making a total \overline{RAS} pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its \overline{REQ} input

High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 9 refresh counter address signals to the $MA_0 - MA_8$ outputs. After a half-clock cycle the \overline{RAS} output is asserted for four cycles and then negated for three clock cycles to meet the \overline{RAS} precharge requirements of the DRAMs (see Figures 5 and 6).



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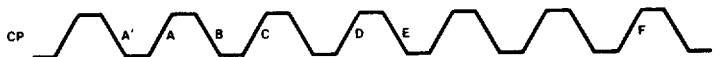


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- A' \overline{REQ}_2 sampled
- A \overline{REQ}_1 sampled (\overline{REQ}_2 disabled by \overline{SEL}_1 circuitry)
 \overline{SEL}_1 triggered (\overline{SEL}_1 triggered by \overline{REQ}_1 sample circuitry)
- B GNT triggered
 $A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
 $A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
- C \overline{RAS} triggered
- D WG triggered
 $A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
- E \overline{CASEN} triggered
- F \overline{RAS} negated
DTACK triggered

* Only on the F764-1.

Figure 3. Sequence of Events for \overline{REQ}_1 Memory Access Cycle for F764-1/765-1



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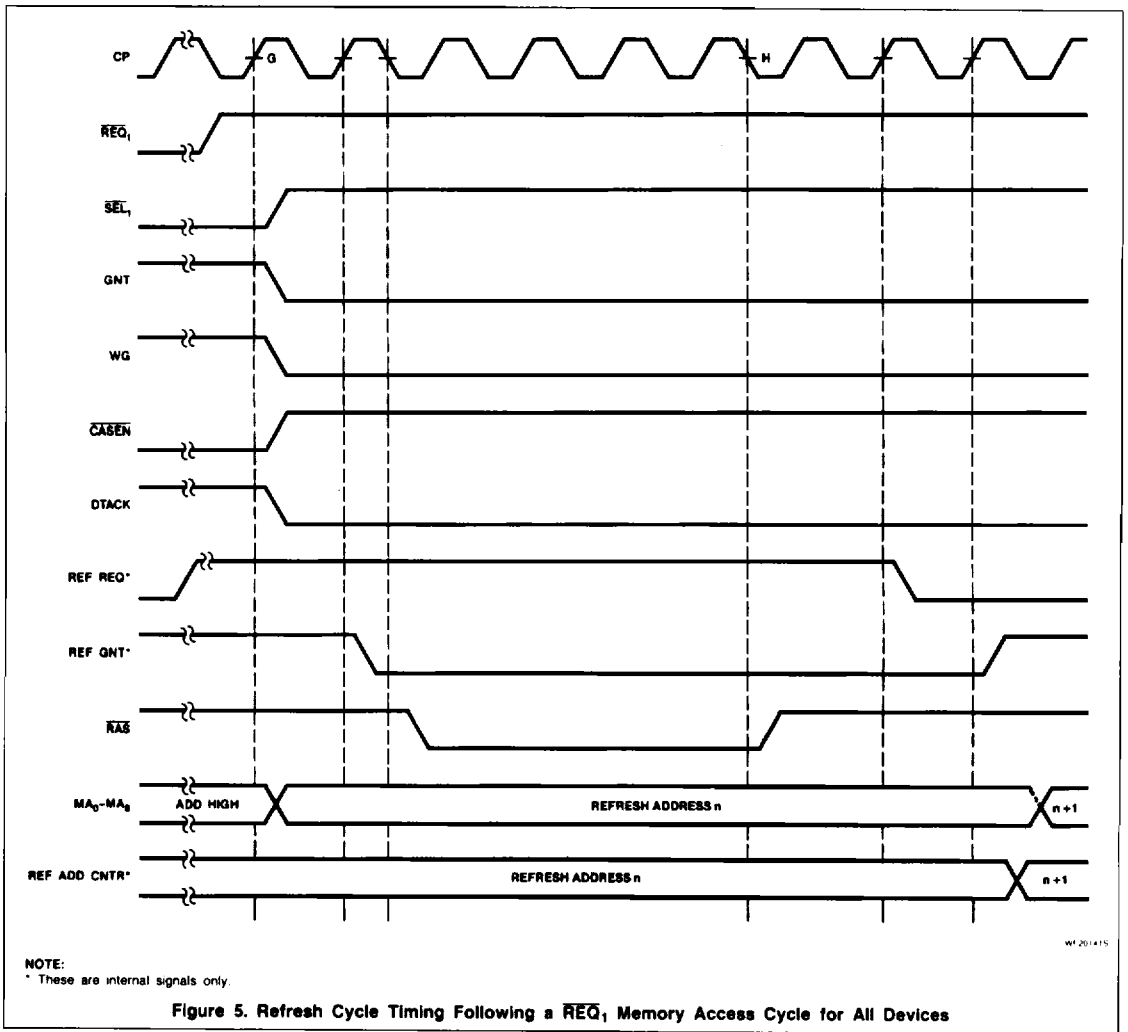
- A' \overline{REQ}_2 sampled
 \overline{SEL}_2 triggered (\overline{SEL}_2 triggered by \overline{REQ}_2 sampling circuitry)
- A \overline{REQ}_1 is not sampled (disabled by \overline{SEL}_2 circuitry)
- B GNT triggered
 $A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
 $A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
- C \overline{RAS} triggered
- D WG triggered
 $A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
- E \overline{CASEN} triggered
- F \overline{RAS} negated
DTACK triggered

* Only on the F764-1

Figure 4. Sequence of Events for \overline{REQ}_2 Memory Access Cycle for F764-1/765-1

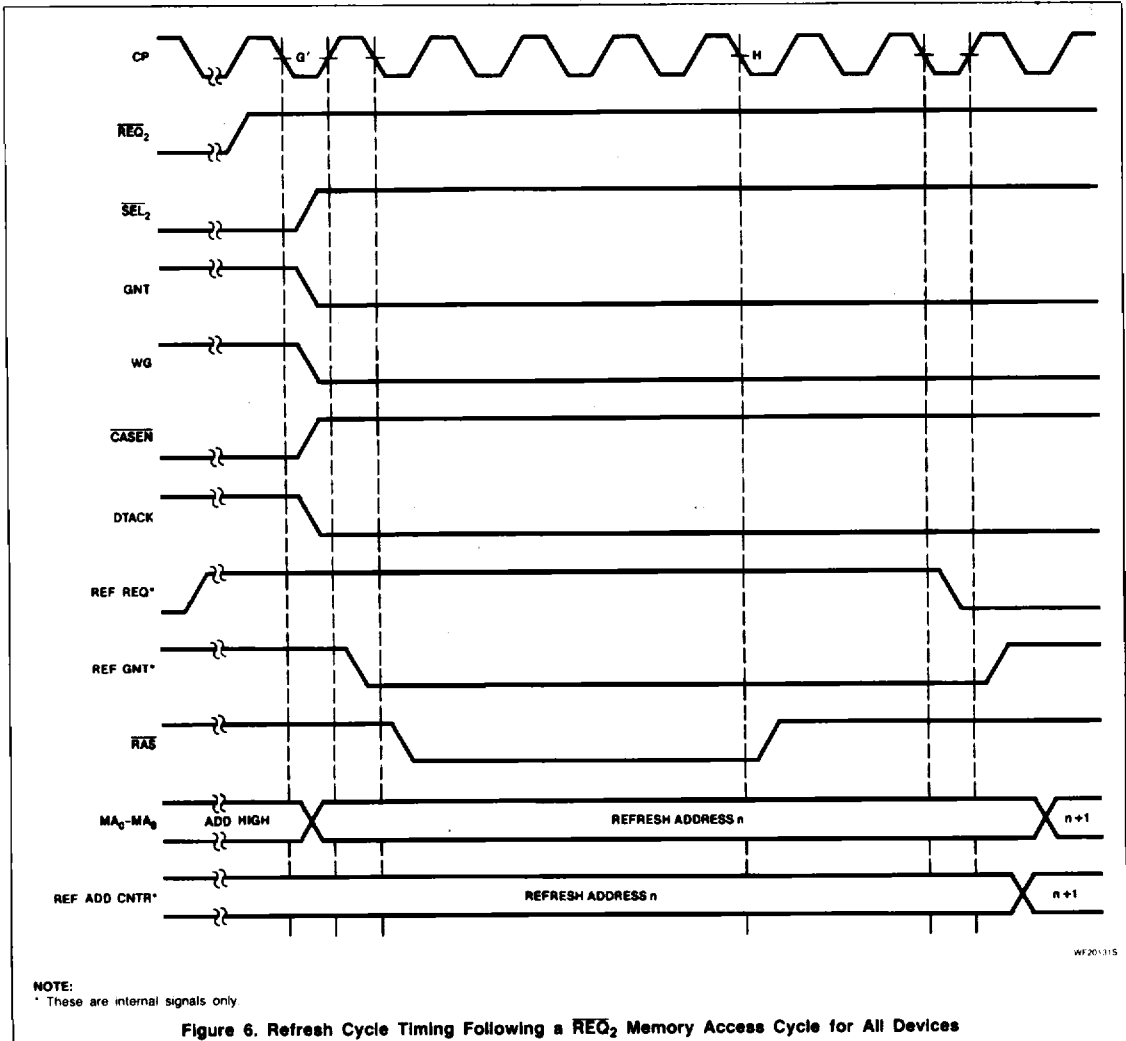
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DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1



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DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

USING 74F764/765, 74F764A/765A, AND 74F764-1/765-1

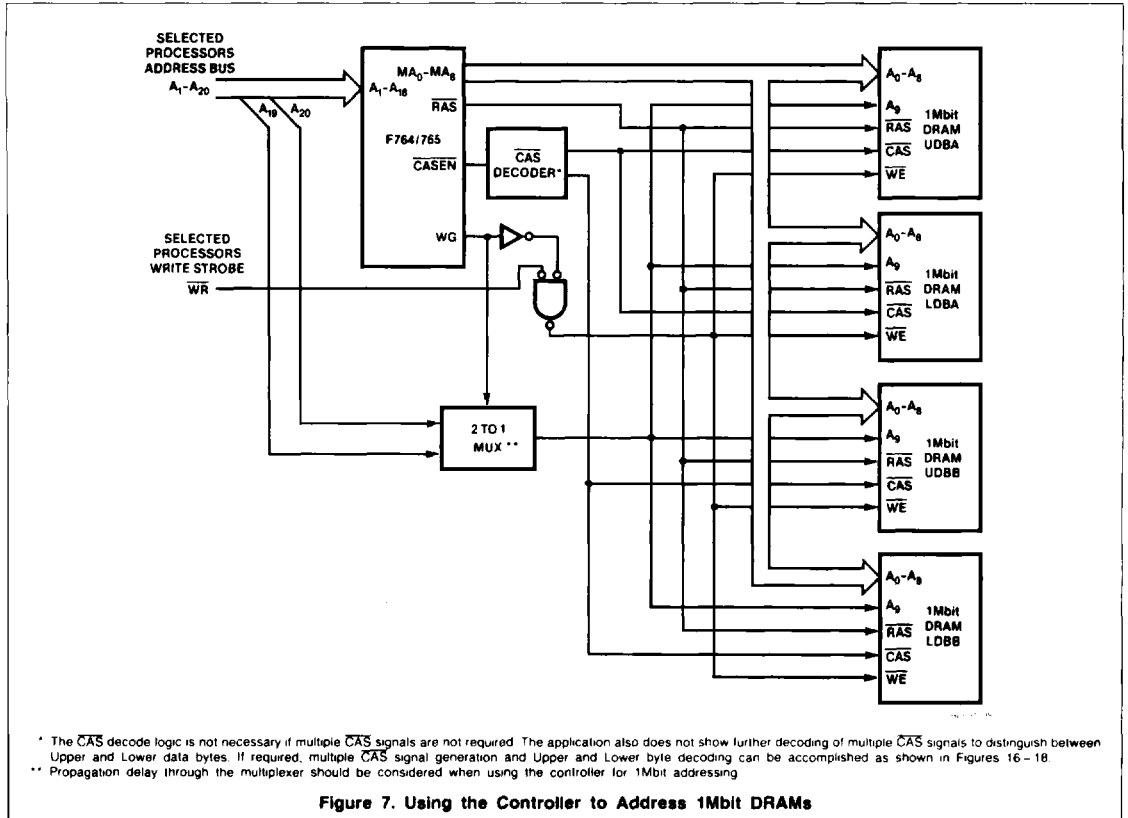
TO ADDRESS 1MBIT DRAMS

The addressing capabilities of the DRAM dual-ported controllers can be extended to address 1Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 7 shows an application, using an external 2-to-1 multiplexer to address 1Mbit dynamic RAMs. The 9-bit internal refresh counter of the controller provides 512 row addresses which more than meet the refreshing needs for most industry standard 1Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 512 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 512 row addresses.

The WG output of the controller should be used to multiplex between the external row and column address bits. However it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.



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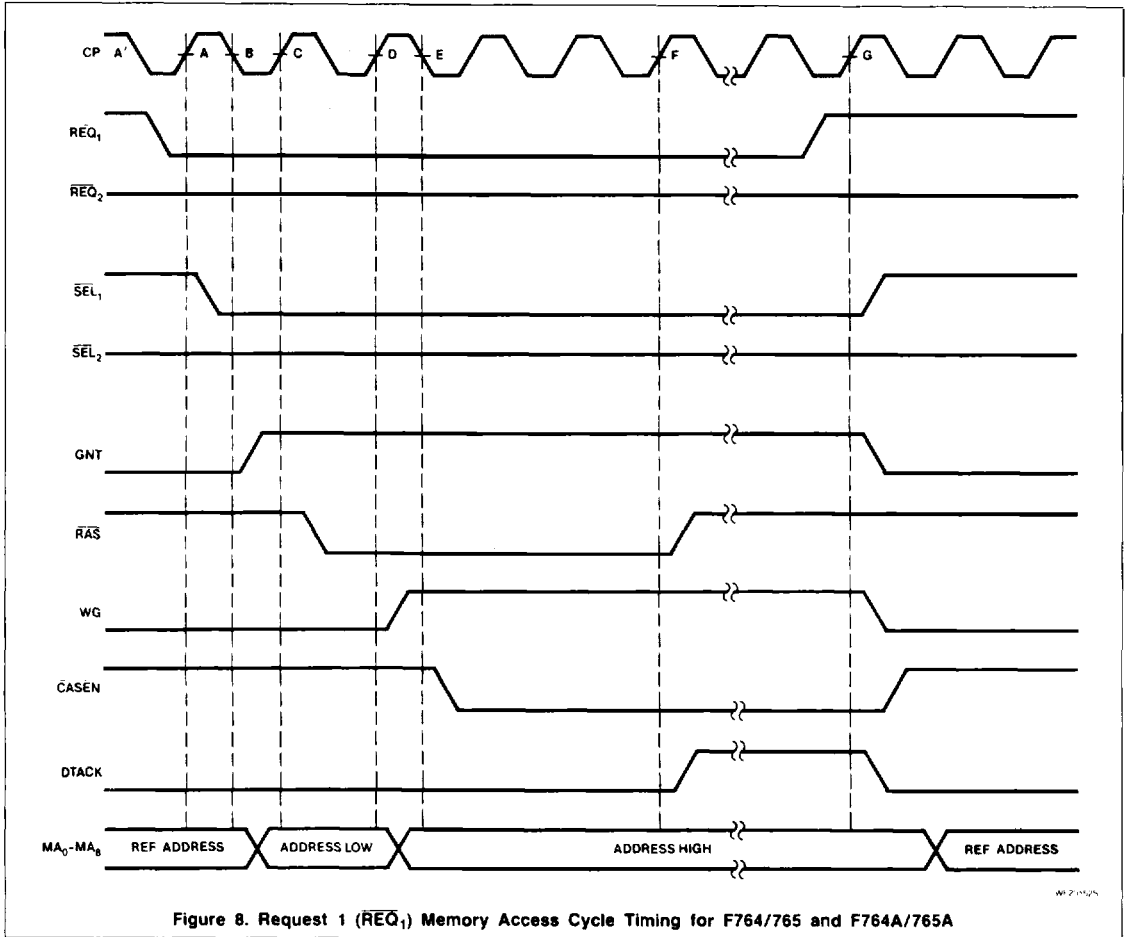
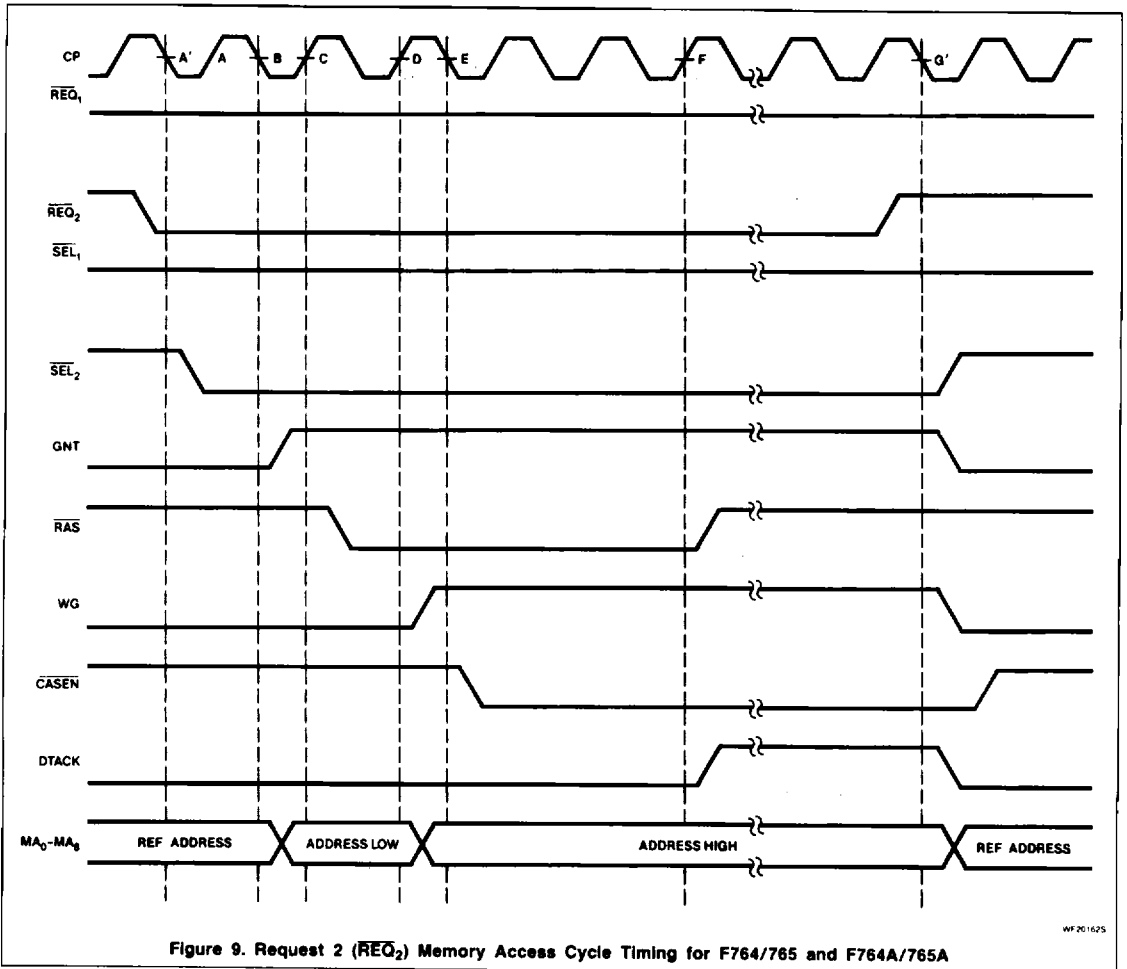


Figure 8. Request 1 (REQ_1) Memory Access Cycle Timing for F764/765 and F764A/765A

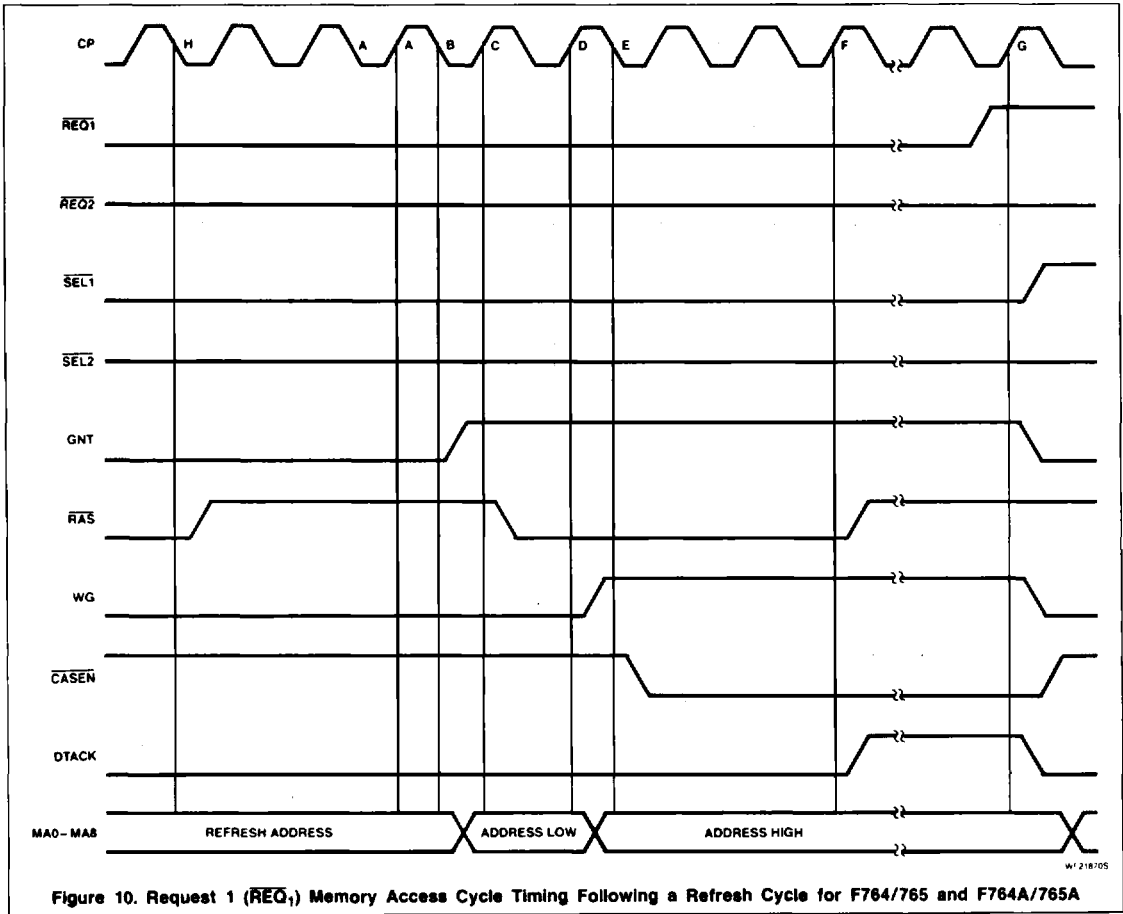
DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
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DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1



DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1

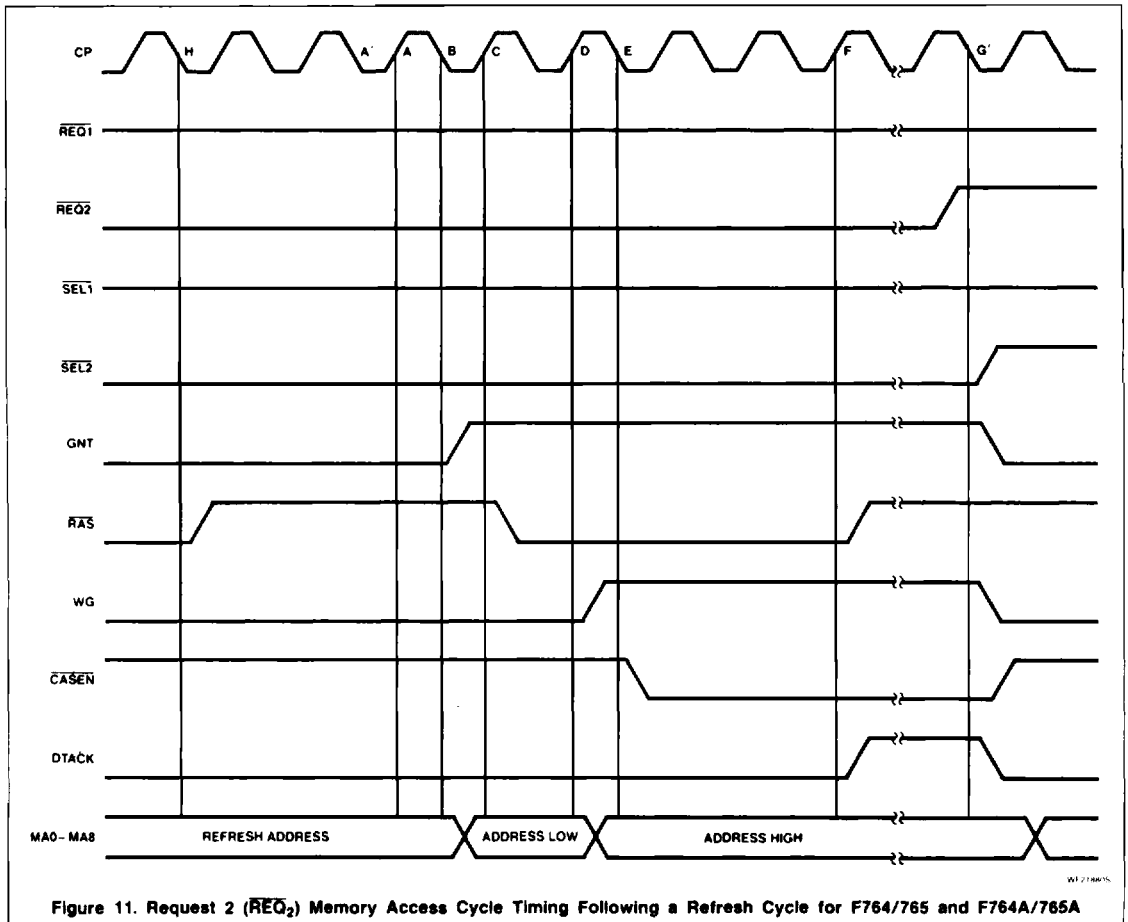
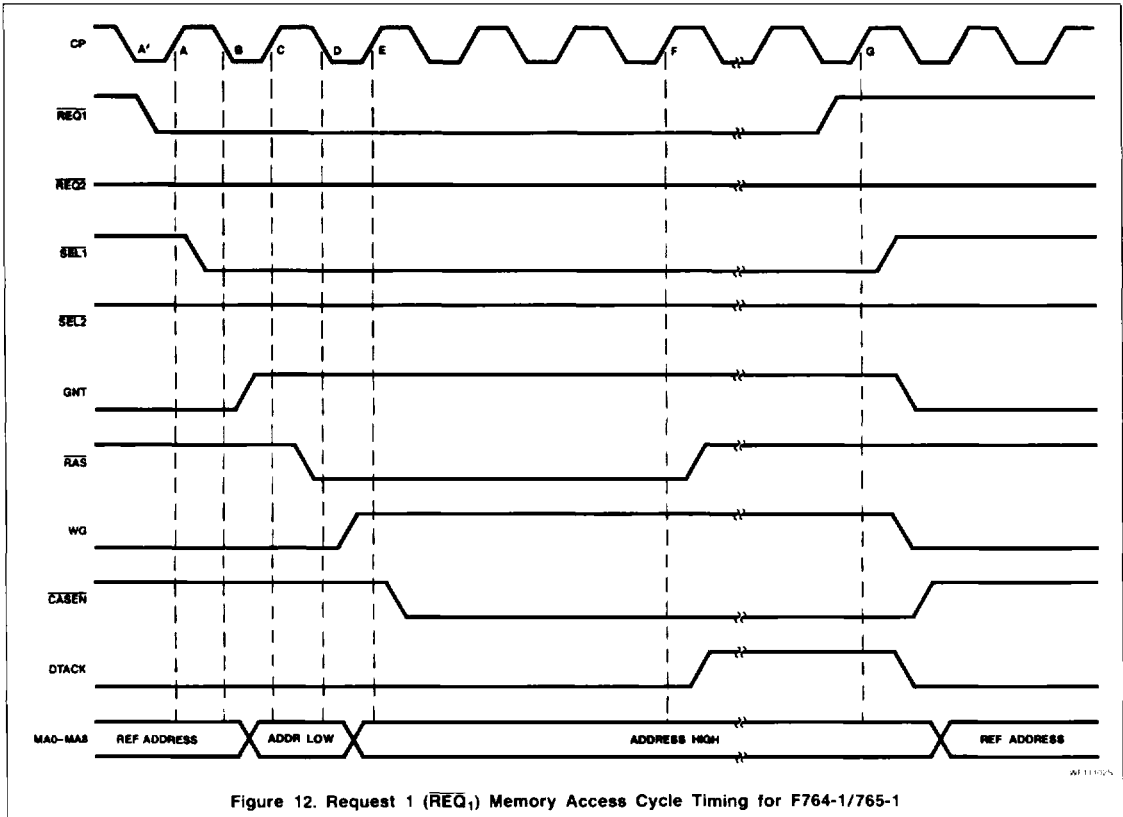


Figure 11. Request 2 (REQ₂) Memory Access Cycle Timing Following a Refresh Cycle for F764/765 and F764A/765A

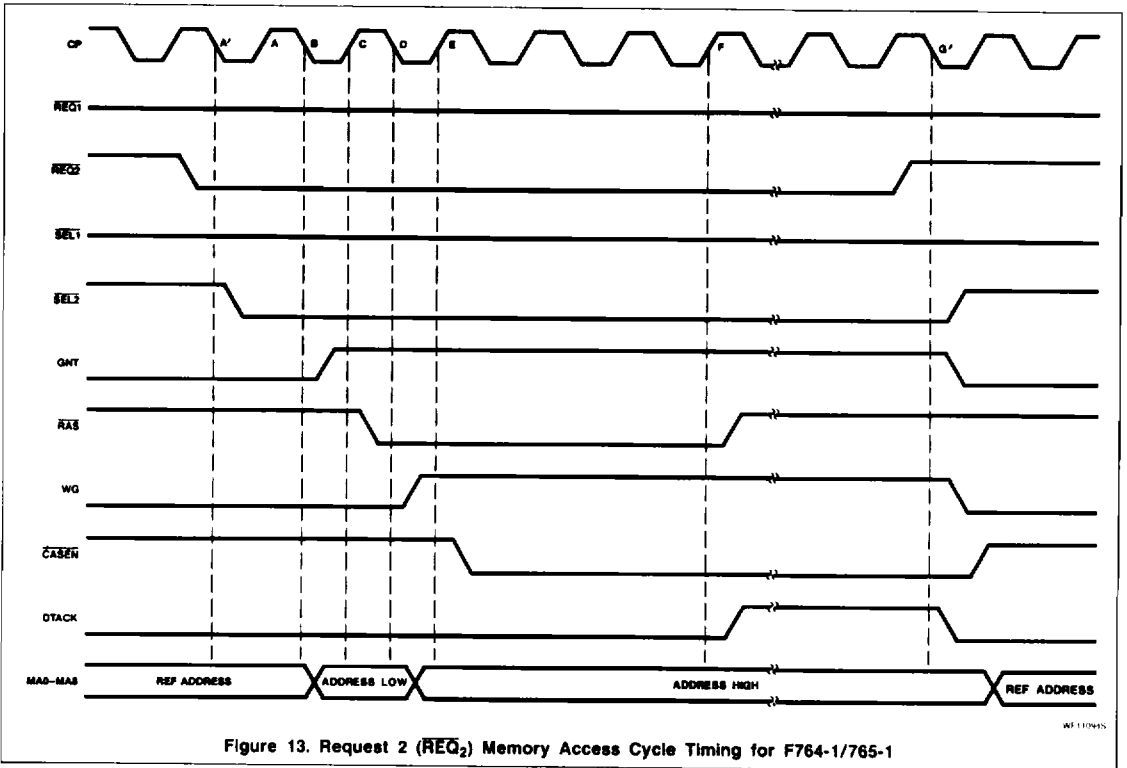
DRAM Dual-Ported Controllers

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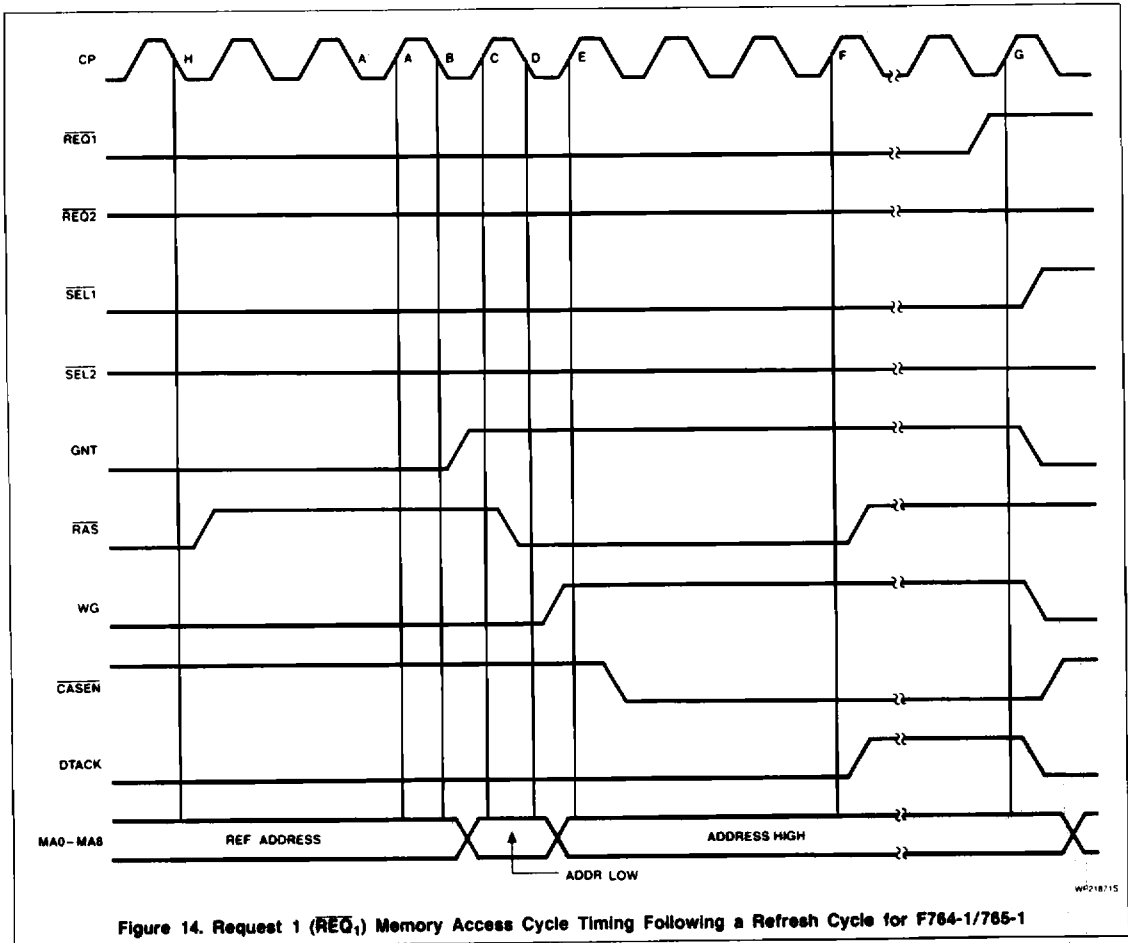
DRAM Dual-Ported Controllers

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74F764-1/765-1



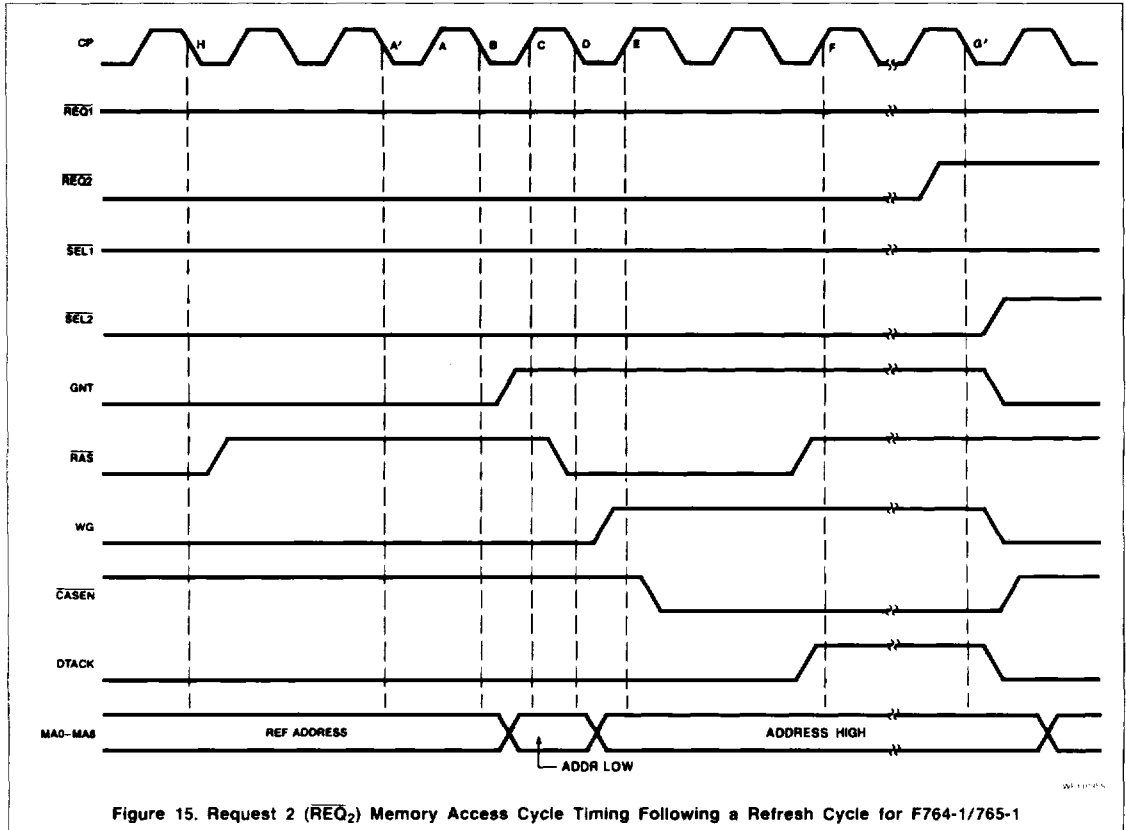
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74F764-1/765-1



DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764/765, 74F764A/765A	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	500	mA
T _A	Operating free-air temperature range	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764/765, 74F764A/765A			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current ¹			24	mA
T _A	Operating free-air temperature ¹	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	74F764/765, 74F764A/765A			UNIT		
			Min	Typ ²	Max			
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -15mA	± 10%V _{CC}	2.5	3.2	V	
V _{OH2} ³	High-level output voltage		I _{OH2} ³ = -35mA	± 5%V _{CC}	2.7	3.4	V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24mA	± 10%V _{CC}		0.35	0.50	V
V _{OL2} ⁴	Low-level output voltage		I _{OL2} ⁴ = 60mA	± 5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = 0.0V, V _I = 7.0V					100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V					-0.6	mA
I _{OS}	Short-circuit output current ⁵	V _{CC} = MAX			-100		-225	mA
I _{CC}	Supply current (total)	I _{CC} H	V _{CC} = MAX			150	200	mA
		I _{CC} L				165	210	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. Refer to Appendix A.

4. Refer to Appendix A.

5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER ¹	74F764/765, 74F764A/765A					UNIT
		T _A = +25°C V _{CC} = +5.0V C _L = 300pF R _L = 70Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 300pF R _L = 70Ω		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation delay CP(G) to $\overline{\text{SEL}}_1$	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(A) to $\overline{\text{SEL}}_1$	5	10	14	5	16	ns
t _{PLH}	Propagation delay CP(G') to $\overline{\text{SEL}}_2$	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(A') to $\overline{\text{SEL}}_2$	5	10	14	5	16	ns
t _{PLH}	Propagation delay CP(B) to GNT	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(G or G') to GNT	5	10	15	5	16	ns
t _{PLH} t _{PHL}	Propagation delay CP(B) to MA(row address)	5 5	12 11	17 15	5 5	18 16	ns
t _{PLH}	Propagation delay CP(F or H) to $\overline{\text{RAS}}$	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(C) to $\overline{\text{RAS}}$	5	10	14	5	16	ns
t _{PLH}	Propagation delay CP(D) to WG	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(G or G') to WG	8	13	17	8	18	ns
t _{PLH} t _{PHL}	Propagation delay CP(D) to MA(column address)	5 5	12 10	17 15	5 5	18 16	ns
t _{PLH}	Propagation delay CP(G or G') to $\overline{\text{CASEN}}$	7	17	23	7	25	ns
t _{PHL}	Propagation delay CP(E) to $\overline{\text{CASEN}}$	5	10	14	5	16	ns
t _{PLH}	Propagation delay CP(F) to DTACK	5	10	14	5	16	ns
t _{PHL}	Propagation delay CP(G or G') to DTACK	6	13	17	5	18	ns
74F765, 74F765A Only							
t _{PLH} t _{PHL}	Propagation delay A ₁ - A ₁₈ to MA ₀ - MA ₈	4 2	7 5	12 8	4 4	13 19	ns

NOTE:

1. For test conditions, see the AC waveforms.

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AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER ²	74F764/765, 74F764A/765A					UNIT
		T _A = +25°C V _{CC} = +5.0V C _L = 300pF R _L = 70Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 300pF R _L = 70Ω		
		Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low REQ ₁ , REQ ₂ to CP	2 2			2 2		ns
t _h (H) t _h (L)	Hold time, High or Low CP to REQ ₁ , REQ ₂	2 2			3 3		ns
t _w (H) t _w (L)	CP pulse width High or Low	5 5			5 5		ns
t _w (H) t _w (L)	RCP pulse width High or Low	10 10			10 10		ns
74F764, 74F764A Only							
t _s (H) t _s (L)	Setup time, High or Low A ₁ - A ₁₈ to CP(↓)	-4 ¹ -4			-5 -5		ns
t _h (H) t _h (L)	Hold time, High or Low CP(↓) to A ₁ - A ₁₈	5 5			5 5		ns
74F764/765 Only							
f _{MAX}	Input clock frequency	100	150		100		MHz
74F764A/765A Only							
f _{MAX}	Input clock frequency	150	175		150		MHz

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 4ns after the falling edge of the CP clock. It is suggested that SEL₂ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL₁ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. For the Test Conditions, see the AC Waveforms.

DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764-1/765-1	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	500	mA
T _A	Operating free-air temperature range	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764-1/765-1			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current ¹			-20	mA
I _{OL}	Low-level output current ¹			8	mA
T _A	Operating free-air temperature	0		70	°C

NOTE:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	74F764-1, 74F765-1			UNIT			
			Min	Typ ²	Max				
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -20mA	± 10%V _{CC}	2.4	2.70	V		
				± 5%V _{CC}	2.6	3.0	V		
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 8mA	± 10%V _{CC}		0.30	0.50	V	
				± 5%V _{CC}		0.30	0.50	V	
V _{OLZ} ³	Low-level output voltage		I _{OLZ} ³ = 75mA	± 5%V _{CC}		2.1	2.5	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-0.7	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = 0.0V, V _I = 7.0V					100	μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V					20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				-0.2	-0.6	mA	
I _{OS}	Short-circuit output current ⁴	V _{CC} = MAX				-80	-150	-225	mA
I _{CC}	Supply current (total)	I _{CC} H	V _{CC} = MAX				120	165	mA
		I _{CC} L					125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. Refer to Appendix A.

4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A,
74F764-1/765-1

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T _A = +25°C V _{CC} = +5.0V C _L = 300pF R _L = 70Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 300pF R _L = 70Ω		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	100	150		100		MHz
t _{PLH}	Propagation delay CP(G) to SEL ₁	9	12	15	8	17	ns
t _{PHL}	Propagation delay CP(A) to SEL ₁	13	16	20	12	22	ns
t _{PLH}	Propagation delay CP(G') to SEL ₂	9	12	15	8	17	ns
t _{PHL}	Propagation delay CP(A') to SEL ₂	13	16	20	12	22	ns
t _{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t _{PHL}	Propagation delay CP(G or G') to GNT	20	23	26	17	28	ns
t _{PLH}	Propagation delay CP(B) to MA(row address)	11	14	17	10	19	ns
t _{PHL}		14	18	22	13	24	ns
t _{PLH}	Propagation delay CP(F or H) to RAS	11	14	16	10	18	ns
t _{PHL}	Propagation delay CP(C) to RAS	13	17	20	12	22	ns
t _{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t _{PHL}	Propagation delay CP(G or G') to WG	20	23	26	19	26	ns
t _{PLH}	Propagation delay CP(D) to MA(column address)	12	14	17	11	19	ns
t _{PHL}		14	18	21	13	23	ns
t _{PLH}	Propagation delay CP(G or G') to CAsEN	14	17	20	12	22	ns
t _{PHL}	Propagation delay CP(E) to CAsEN	14	16	19	13	21	ns
t _{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t _{PHL}	Propagation delay CP(G or G') to DTACK	20	23	26	19	28	ns
74F765-1 Only							
t _{PLH}	Propagation delay A ₁ - A ₁₈ to MA ₀ - MA ₈	9	11	14	8	16	ns
t _{PHL}		9	12	15	8	17	ns

AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		T _A = +25°C V _{CC} = +5.0V C _L = 300pF R _L = 70Ω			T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 300pF R _L = 70Ω		
		Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low REQ ₁ , REQ ₂ to CP	3	1		4		ns
t _h (H) t _h (L)	Hold time, High or Low CP to REQ ₁ , REQ ₂	2	0		3		ns
t _w (H) t _w (L)	CP pulse width High or Low	5	3		5		ns
t _w (H) t _w (L)	RCP pulse width High or Low	5			5		ns
74F764-1 Only							
t _s (H) t _s (L)	Setup time, High or Low A ₁ - A ₁₈ to CP(↓)	0	-1 ¹		1		ns
t _h (H) t _h (L)	Hold time, High or Low CP(↓) to A ₁ - A ₁₈	5	3		6		ns

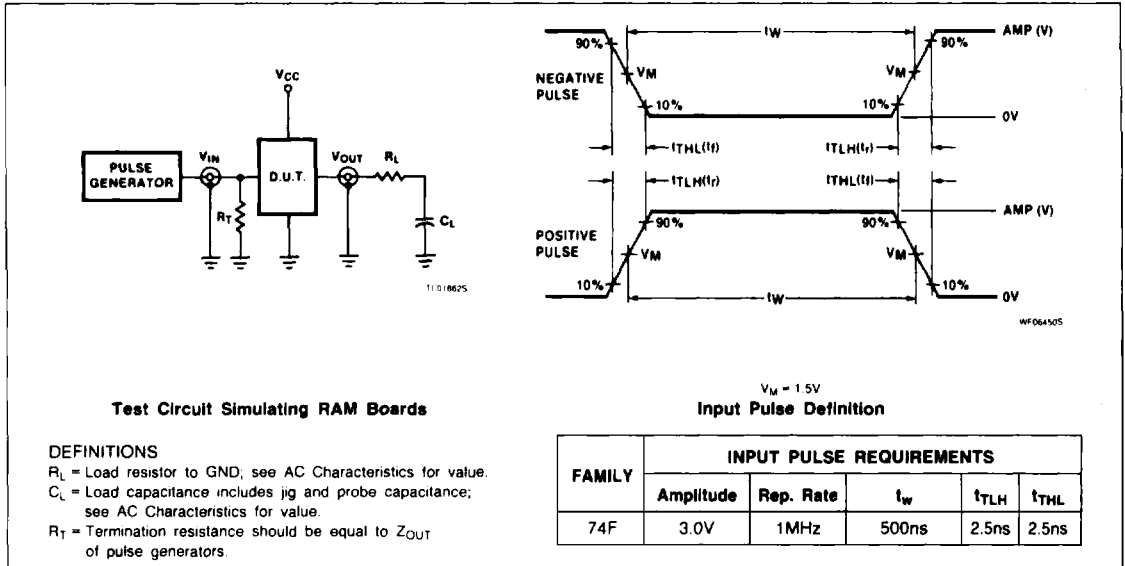
NOTE:

- These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that SEL₂ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL₁, to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

TEST CIRCUIT AND WAVEFORMS FOR ALL DEVICES



APPLICATIONS

The DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (micro-controllers) and the data bus may differ in size.

Figure 16 shows a 68000 processor sharing a $64K \times 8$ (two banks each consisting of sixteen $16K \times 1$ devices) memory with a Z-80 processor. Since neither Z-80 nor 68000 have multiplexed address and data bus, the '765/765A/765-1 is appropriate.

Since the Z-80 has an 8-bit wide data bus, data buffers are used to convert the 16-bit

memory data bus to an 8-bit wide processor bus. Address bit (A_0) from the Z-80 serves as an enable to one of the two data buffers at a given time. Address bit (A_{15}) from either the Z-80 or the 68000 distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

When the Z-80 is selected and A_{15} is a zero, all even bytes will be accessed from UDBA and all odd bytes from LDBA. Similarly, when A_{15} is a one, UDBB will contain all even bytes and LDBB all odd bytes.

For 68000, Upper and Lower Data Strobes (UDS and LDS) determine whether a byte or word transfer will take place. The WAIT input on the Z-80 is asserted when \overline{REQ}_1 is generated, and is negated when the GNT output is asserted by the controller. The additional gating circuitry is to ensure that DTACK to the 68000 is asserted only when it is selected.

Figure 17 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen $256K \times 1$ devices) of dynamic RAM. Using 74F764 in this application may eliminate the need for an external address latch.

Similarly, Figure 18 shows two 68020 processors sharing the same amount of memory.

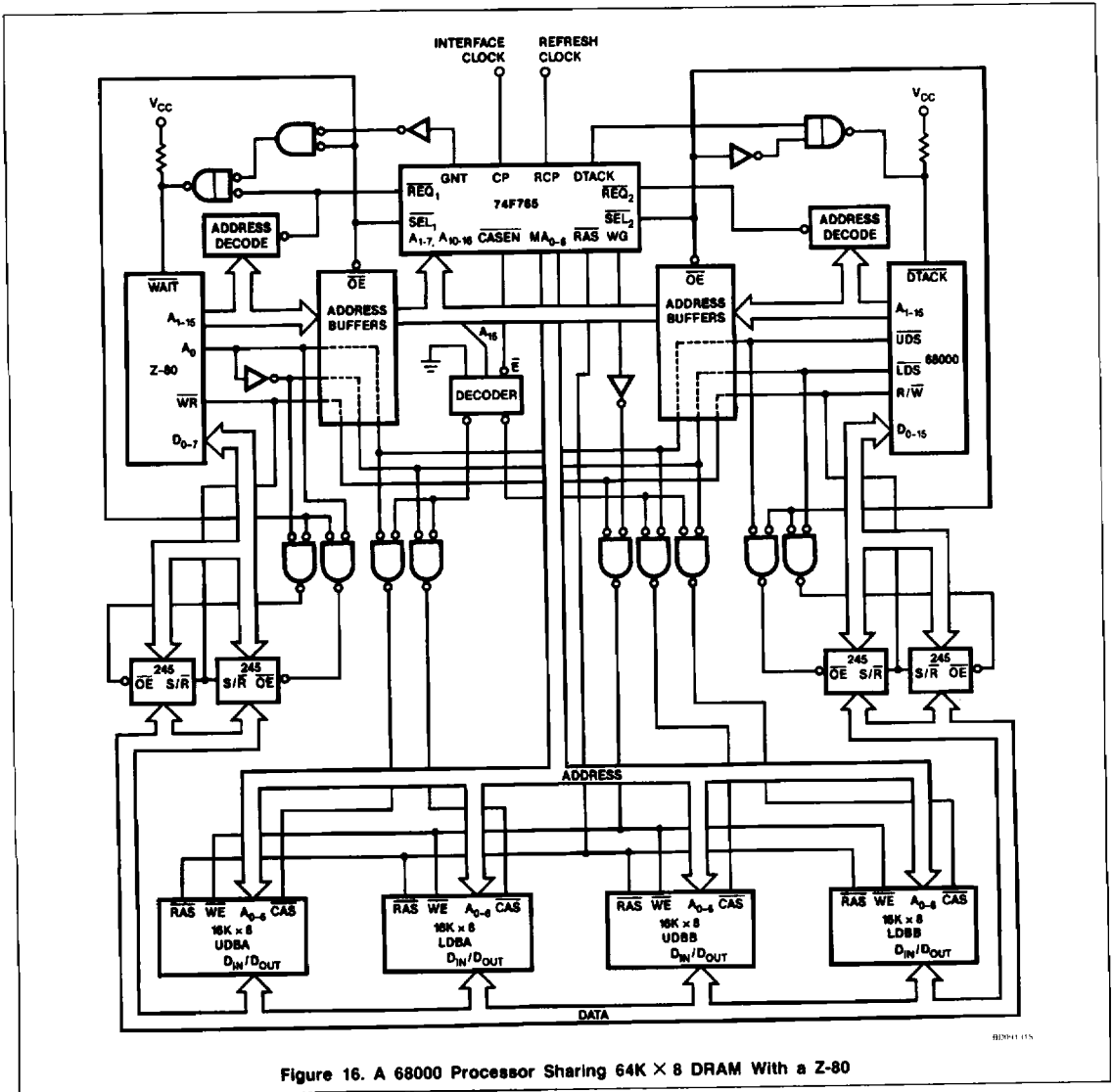
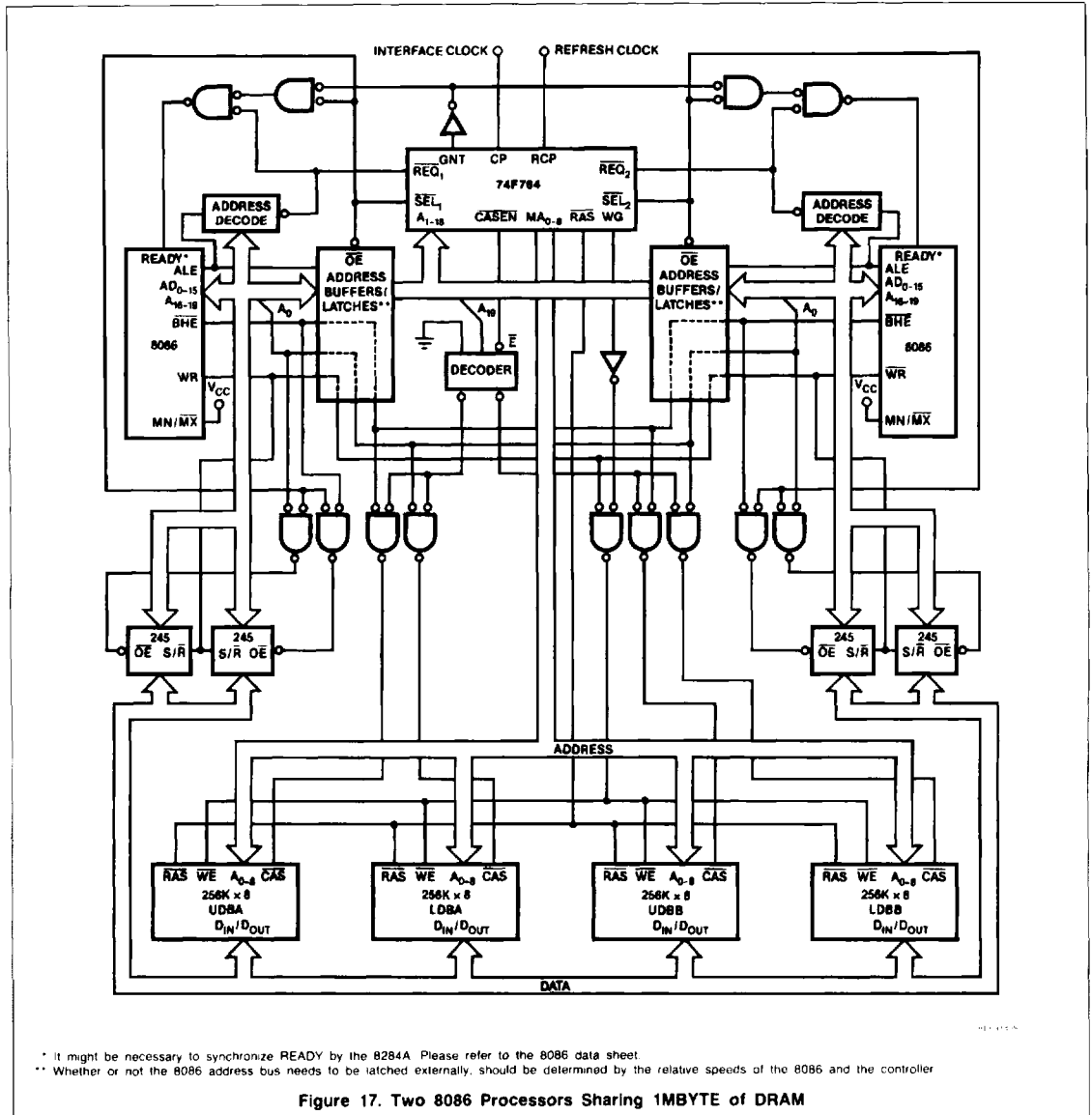


Figure 16. A 68000 Processor Sharing 64K x 8 DRAM With a Z-80



DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

74F764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F764/765 and 74F764A/765A are designed to provide incident wave switching in Dual-Inline-Package (DIP) or Zig-zag-Inline-Package (ZIP) housed memory arrays and first reflected wave switching in Single-Inline-Package (SIP) or Single-Inline-Module (SIM) housed arrays. The 74F764-1/765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω . If a signal line has settled out in a High state at 4 volts and must be pulled down to

0.8 volts or less on the incident wave, the DRAM Controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 1 - 4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate a graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F764/765 or 74F764A/765A driving dual-

inline packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single-inline modules using the 74F764/765 or 74F764A/765A, or when driving any type of memory arrays with the 74F764-1/765-1, the schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5 - 7 are double exposures showing the High to Low and Low to High transitions while driving four banks of eight Dual-Inline-Packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F764/765/764A/765A to ring two volts below ground while the 74F764-1/765-1 make nice clean transitions. In Figure 7 the 74F764/765/764A/765A is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300pF to ground (the worst of the four branches is shown).

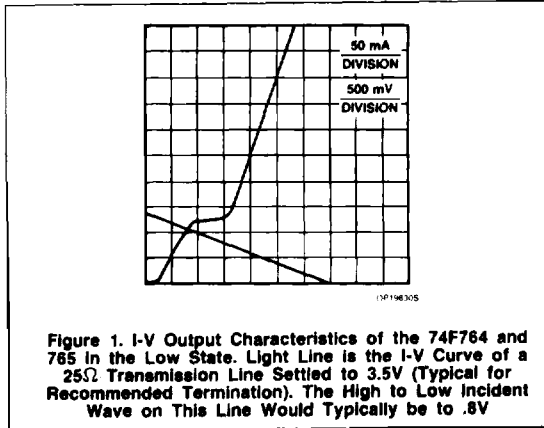


Figure 1. I-V Output Characteristics of the 74F764 and 765 in the Low State. Light Line is the I-V Curve of a 25Ω Transmission Line Settled to 3.5V (Typical for Recommended Termination). The High to Low Incident Wave on This Line Would Typically be to .8V

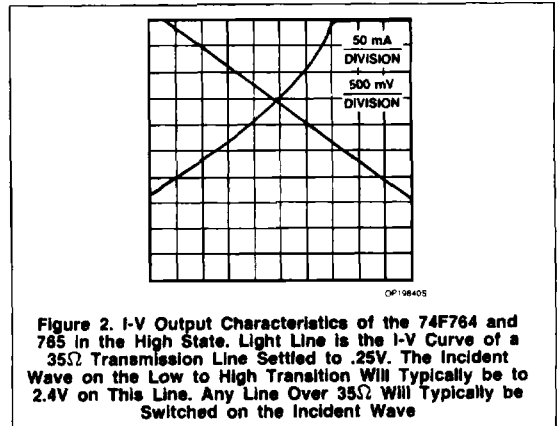


Figure 2. I-V Output Characteristics of the 74F764 and 765 in the High State. Light Line is the I-V Curve of a 35Ω Transmission Line Settled to .25V. The Incident Wave on the Low to High Transition Will Typically be to 2.4V on This Line. Any Line Over 35Ω Will Typically be Switched on the Incident Wave

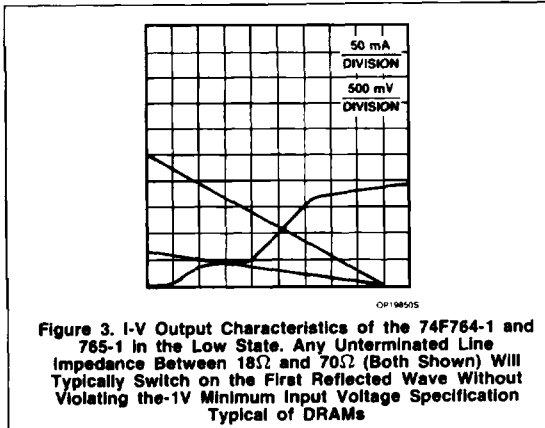


Figure 3. I-V Output Characteristics of the 74F764-1 and 765-1 in the Low State. Any Unterminated Line Impedance Between 18Ω and 70Ω (Both Shown) Will Typically Switch on the First Reflected Wave Without Violating the IV Minimum Input Voltage Specification Typical of DRAMs

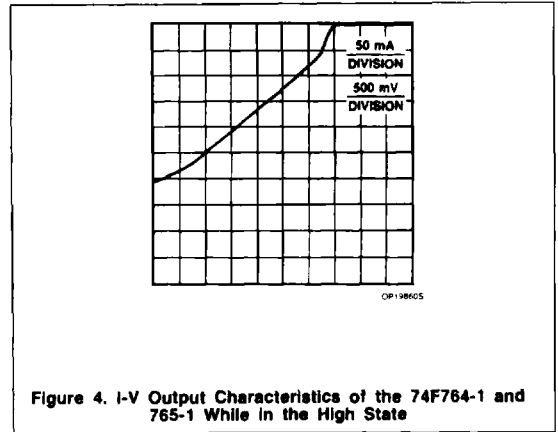


Figure 4. I-V Output Characteristics of the 74F764-1 and 765-1 While in the High State

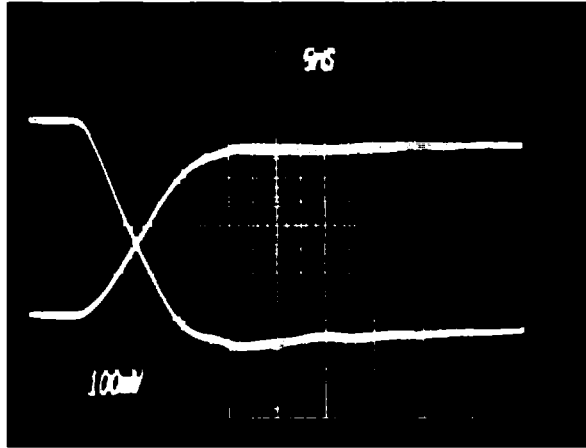


Figure 5. 74F764-1/765-1 Driving 32 DRAMs (Unterminated)

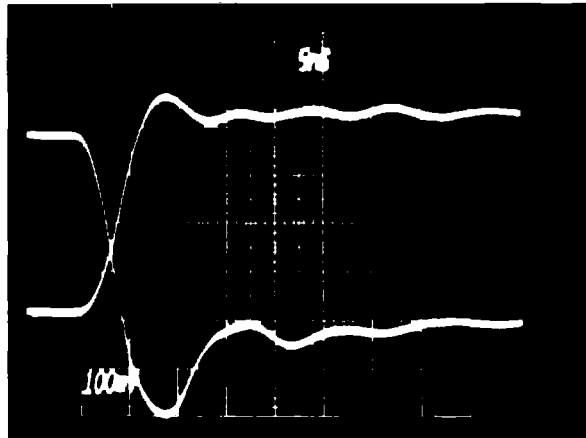


Figure 6. 74F764/765/764A/765A Driving 32 DRAMs (Unterminated)

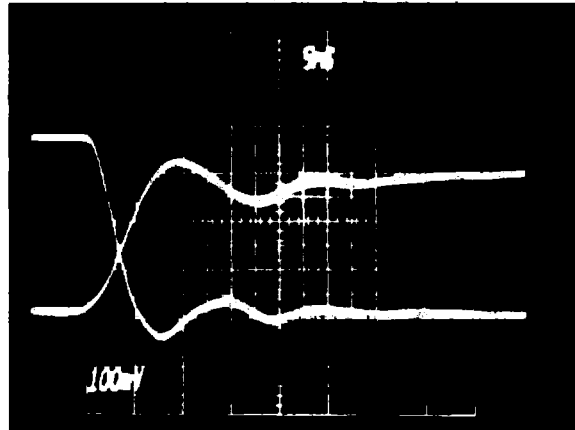


Figure 7. 74F764/765/764A/765A Driving 32 DRAMs (Terminated as in Figure 8a)

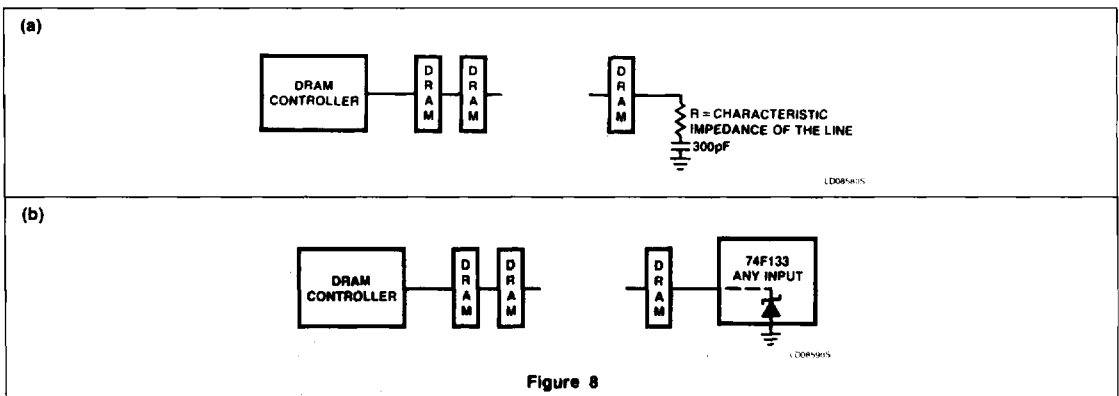


Figure 8