



LC74786, 74786M, 74786JM

On-Screen Display Controller

Overview

The LC74786, LC74786M, and LC74786JM are on-screen display controller CMOS ICs that display characters and patterns on the TV screen under microprocessor control. These ICs support 12×18 -dot characters and can display 12 lines by 24 characters of text.

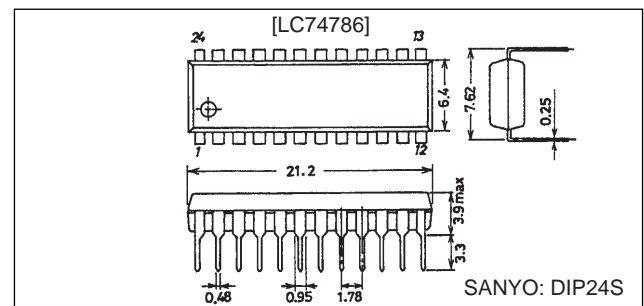
Features

- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) \times 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128 (128 characters, one spacing character, and one transparent spacing character)
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: About 1.0 second and about 0.5 second
- Blanking: Over the whole font (12×18 dots)
- Background color: 8 colors (internal synchronization mode): $2f_{SC}$ and $4f_{SC}$
- Line background color
 - Can be set for 3 lines
 - Line background color: 8 colors (internal synchronization mode): $2f_{SC}$ and $4f_{SC}$
- External control input: 8-bit serial input format
- On-chip sync separator circuit
- Video outputs - NTSC, PAL, PAL-N, PAL-M, NTSC 4.43, and PAL60 format composite video outputs
- Package
 - 24-pin plastic DIP-24S (300 mil)
 - 24-pin plastic MFP-24 (375 mil)
 - 24-pin plastic MFP-24S (300 mil)

Package Dimensions

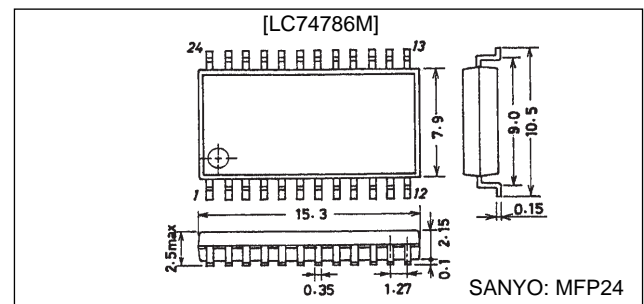
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3067-DIP24S



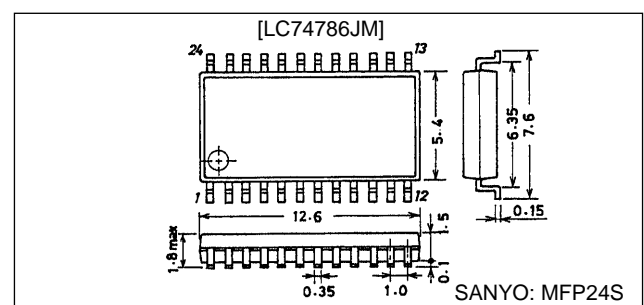
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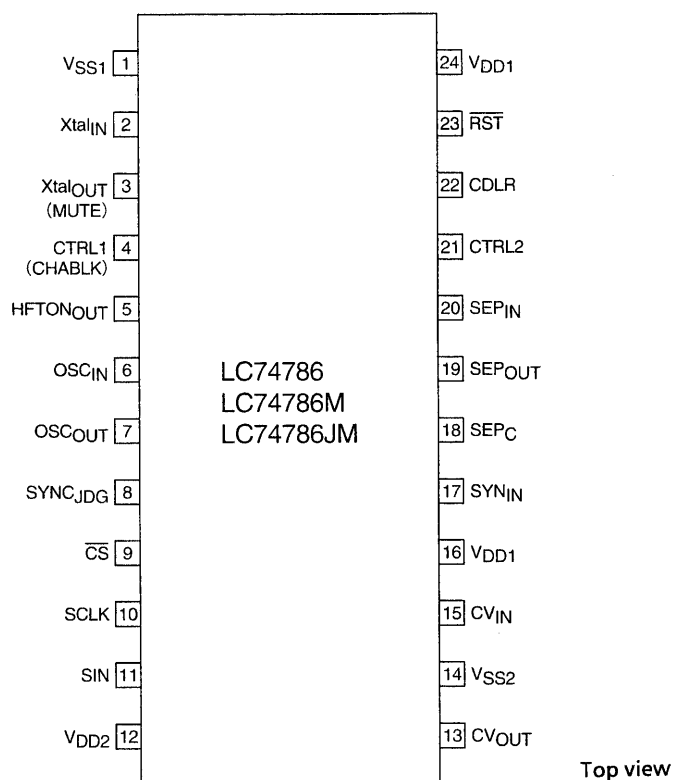
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3112-MFP24S



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Pin Assignment



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Pin Functions

Pin No.	Pin Name	Function	Notes
1	V _{SS1}	Ground	Ground connection (digital system ground)
2	Xtal _{IN}	Crystal oscillator (MUTE input)	These pins are used either to connect the crystal and capacitors used to form an external crystal oscillator circuit to generate the internal synchronizing signals, or to input an external clock signal (2fsc or 4fsc). As a mask option, the Xtal _{OUT} pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	Xtal _{OUT} (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK output)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character · frame) output. This is a 3-value output.
5	HFTON _{OUT}	Background line output	Outputs the range signal specified by LNA*, LNB*, and LNC*. Outputs the crystal oscillator clock when RST is low. (This signal is not output after a reset command is executed.)
6	OSC _{IN}	LC oscillator	Connections for the inductor and capacitor that form the character output dot clock generation oscillator.
7	OSC _{OUT}		
8	SYNC _{JDG}	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs the dot clock (LC oscillator) when RST is low. (This signal is not output on command resets.)
9	\overline{CS}	Enable input	Serial data input circuit enable pin. Serial data input is enabled when a low level is input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
10	SCLK	Clock input	Serial data input circuit clock input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
11	SIN	Data input	Serial data input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
12	V _{DD2}	Power supply	Composite video signal level adjustment power supply (analog system power supply)

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Pin No.	Pin Name	Function	Notes
13	CV _{OUT}	Video signal output	Composite video signal output
14	V _{SS2}	Ground	Ground connection (analog system ground)
15	CV _{IN}	Video signal input	Composite video signal input
16	V _{DD1}	Power supply	Power supply (+5 V: digital system power supply)
17	SYN _{IN}	Sync separator circuit input	Video signal input to the internal sync separator circuit (Used as either the horizontal synchronizing signal or the composite synchronizing signal input when the internal sync separator circuit is not used.)
18	SEP _C	Sync separator circuit bias voltage	Internal sync separator circuit bias voltage monitor
19	SEP _{OUT}	Composite synchronizing signal output	Internal sync separator circuit composite synchronizing signal output. Can be switched to function as a signal (high, low, or ST. pulse) output by the SEL0 and MOD0 setting.
20	SEP _{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal created by integrating the SEP _{OUT} pin output signal. An integration circuit must be connected to the SEP _{OUT} pin. This pin must be tied to V _{DD1} if unused. This pin can be switched to function as the frame signal input mode by setting SEL1 high. This is valid when CTL3 is set high. This input has hysteresis characteristics.
21	CTRL2	NTSC/PAL-M selection input	Pin settings take priority for switching between the NTSC, PAL, PAL-M, PAL-N, NTSC 4.43, and PAL60 video formats. The NTSC format is selected when this pin is low after a reset. The command video format (NTSC, PAL, PAL-M, PAL-N, NTSC 4.43, or PAL60) selection is valid. The PAL-M format is selected when this pin is high.
22	CDLR	Background color phase adjustment	Background color phase adjustment. Connect a resistor between this pin and ground.
23	$\overline{\text{RST}}$	Reset input	System reset input. A pull-up resistor is built in and the input has hysteresis characteristics.
24	V _{DD1}	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: Both V_{DD1} pins must be connected to the power supply.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD1} and V_{DD2}	$V_{SS}-0.3$ to $V_S+6.5$	V
Maximum input voltage	V_{IN} max	All input pins	$V_S-0.3$ to $V_{DD}+0.3$	V
Maximum output voltage	V_{OUT} max	HFTON _{OUT} , SYNC _{JDG} , and SEP _{OUT}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	P_d max	$T_a = 25^\circ\text{C}$	350	mW
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	V_{DD1}	4.5	5.0	5.5	V
	V_{DD2}	V_{DD2}	4.5	5.0	$1.27 V_{DD1}$	V
Input high-level voltage	V_{IH1}	$\overline{\text{RST}}$, $\overline{\text{CS}}$, SIN, SCLK, SEP _{IN} , and MUTE	$0.8 V_{DD1}$		$V_{DD1}+0.3$	V
	V_{IH2}	CTRL1 and CTRL2	$0.7 V_{DD1}$		$V_{DD1}+0.3$	V
Input low-level voltage	V_{IL1}	$\overline{\text{RST}}$, $\overline{\text{CS}}$, SIN, SCLK, SEP _{IN} , and MUTE	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V
	V_{IL2}	CTRL1 and CTRL2	$V_{SS} - 0.3$		$0.3 V_{DD1}$	V
Pull-up resistance	R_{PU}	$\overline{\text{RST}}$, $\overline{\text{CS}}$, SIN, SCLK, and MUTE Applies to pins set up by options.	25	50	90	$k\Omega$
Composite video signal input voltage	V_{IN1}	CV _{IN} : $V_{DD1} = 5\text{ V}$		2.0		Vp-p
	V_{IN2}	SYN _{IN} : $V_{DD1} = 5\text{ V}$		2.0	2.5	Vp-p
Input voltage	V_{IN3}	Xtal _{IN} (when used for external clock input) $f_{IN} = 2\text{fsc}$ or 4fsc ; $V_{DD1} = 5\text{ V}$	0.10		5.0	Vp-p
Oscillator frequencies	F_{OSC1}	Xtal _{IN} and Xtal _{OUT} oscillator pins (2fsc: NTSC)		7.159		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (4fsc: NTSC)		14.318		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (2fsc: PAL)		8.867		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (4fsc: PAL)		17.734		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (2fsc: PAL-M)		7.151		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (4fsc: PAL-M)		14.302		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (2fsc: PAL-N)		7.164		MHz
		Xtal _{IN} and Xtal _{OUT} oscillator pins (4fsc: PAL-N)		14.328		MHz
	F_{OSC2}	OSC _{IN} and OSC _{OUT} oscillator pins (LC oscillator)	5		10	MHz

Note: Applications must be especially cautious about noise when using the Xtal_{IN} input pin in clock input mode.

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Electrical Characteristics at Ta = -30 to +70°C. V_{DD1} = 5 V unless otherwise specified.

Parameter	Symbol	Pin	Conditions	Ratings			Unit	
				min	typ	max		
Input off leakage current	I _{leak1}	CV _{IN}				1	μA	
Output off leakage current	I _{leak2}	CV _{OUT}				1	μA	
Output high-level voltage	V _{OH1}	HFTON _{OUT} , SYNC _{JDG} , and SEP _{OUT}	V _{DD1} = 4.5 V, I _{OH} = -1.0 mA	3.5			V	
Output low-level voltage	V _{OL1}	HFTON _{OUT} , SYNC _{JDG} , and SEP _{OUT}	V _{DD1} = 4.5 V, I _{OL} = -1.0 mA			1.0	V	
Three-value output voltage	V _O	CHABLK	V _{DD1} = 5.0 V	H	3.3		5.0	V
				M	1.8		2.3	V
				L	0		0.8	V
Input current	I _{IH}	RST, CS, SIN, SCLK, CTRL1, SEP _{IN} , and MUTE	V _{IN} = V _{DD1}			1	μA	
	I _{IL}	CTRL1 and OSC _{IN}	V _{IN} = V _{SS1}	-1			μA	
Operating mode current drain	I _{DD1}	V _{DD1}	All outputs: open Xtal: 7.159 MHz LC: 8 MHz			15	mA	
	I _{DD2}	V _{DD2}	V _{DD2} = 5 V			20	mA	
SYNC level	V _{SN}			(1)	0.70	0.82	0.94	V
				(2)	0.89	1.01	1.13	
				(3)	1.18	1.30	1.42	
Pedestal level	V _{PD}			(1)	1.32	1.44	1.56	V
				(2)	1.52	1.64	1.76	
				(3)	1.81	1.93	2.05	
Color burst low level	V _{CBL}			(1)	0.98	1.10	1.22	V
				(2)	1.17	1.29	1.41	
				(3)	1.46	1.58	1.70	
Color burst high level	V _{CBH}			(1)	1.63	1.75	1.87	V
				(2)	1.83	1.95	2.07	
				(3)	2.11	2.23	2.35	
Background color low level (other than blue)	V _{RSL0}			(1)	1.17	1.29	1.41	V
				(2)	1.36	1.48	1.60	
				(3)	1.65	1.77	1.89	
Background color high level (other than blue)	V _{RSH0}	CV _{OUT} (1): When the sync level = 0.8 V (2): When the sync level = 1.0 V (3): When the sync level = 1.3 V	V _{DD1} = 5.0 V V _{DD2} = 5.0 V	(1)	2.33	2.45	2.57	V
				(2)	2.52	2.64	2.76	
				(3)	2.81	2.93	3.05	
Blue background 1 low level	V _{RSL1}			(1)	1.08	1.20	1.32	V
				(2)	1.27	1.39	1.51	
				(3)	1.56	1.68	1.80	
Blue background 2 low level	V _{RSL2}			(1)	1.49	1.61	1.83	V
				(2)	1.68	1.80	1.92	
				(3)	1.97	2.09	2.21	
Blue background 1 and 2 high level	V _{RSH1, 2}			(1)	1.97	2.09	2.21	V
				(2)	2.17	2.29	2.41	
				(3)	2.46	2.58	2.70	
Frame level 0	V _{BK0}			(1)	1.40	1.52	1.64	V
				(2)	1.60	1.72	1.84	
				(3)	1.89	2.01	2.13	
Frame level 1	V _{BK1}			(1)	1.97	2.09	2.21	V
				(2)	2.17	2.29	2.41	
				(3)	2.46	2.58	2.70	
Character level	V _{CHA}			(1)	2.55	2.67	2.79	V
				(2)	2.75	2.87	2.99	
				(3)	3.04	3.16	3.28	

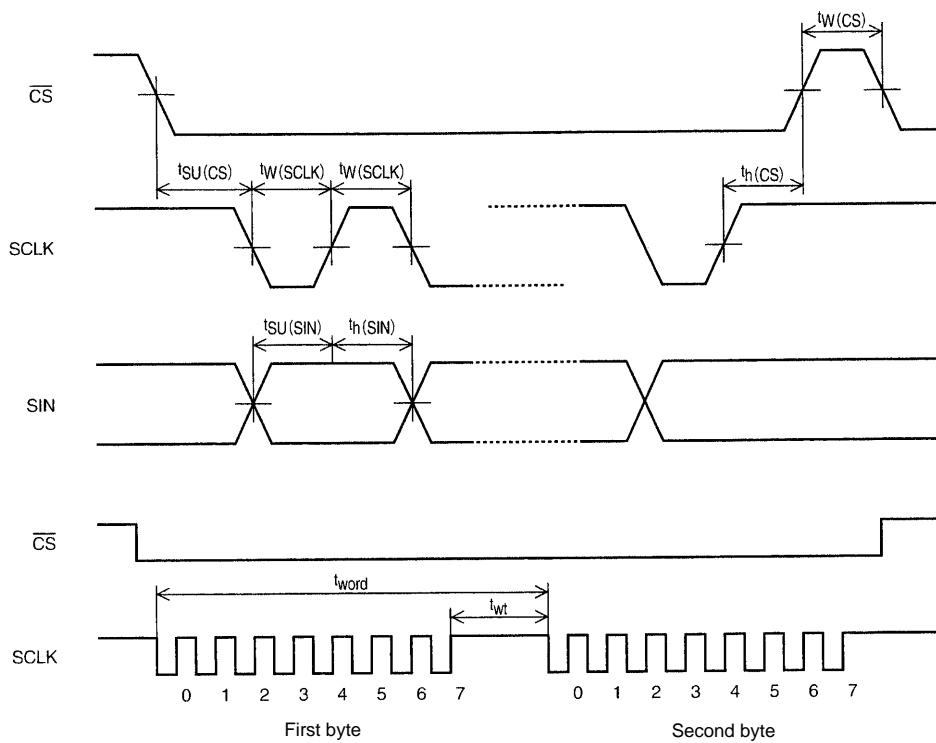
Note: Blue background 1 or 2 are option settings.

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Timing Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD1} = 5 \pm 0.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{W(\text{SCLK})}$	SCLK	200			ns
	$t_{W(\text{CS})}$	$\overline{\text{CS}}$ (The period when $\overline{\text{CS}}$ is high)	1			μs
Data setup time	$t_{\text{SU}(\text{CS})}$	$\overline{\text{CS}}$	200			ns
	$t_{\text{SU}(\text{SIN})}$	SIN	200			ns
Data hold time	$t_{\text{H}(\text{CS})}$	$\overline{\text{CS}}$	2			μs
	$t_{\text{H}(\text{SIN})}$	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			μs
	t_{wt}	The RAM data write time	1			μs

Serial Data Input Timing



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Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

- 1 COMMAND0: Display memory (VRAM) write address setup command
- 2 COMMAND1: Display character data write command
- 3 COMMAND2: Vertical display start position and vertical character size setup command
- 4 COMMAND3: Horizontal display start position and horizontal character size setup command
- 5 COMMAND4: Display control setup command
- 6 COMMAND5: Display control setup command
- 7 COMMAND6: Synchronizing signal detection setup command
- 8 COMMAND7: Display control setup command
- 9 COMMAND8: Display control setup command
- 10 COMMAND9: Display control setup command
- 11 COMMAND10: Display control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address setup	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	0	at	c7	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical character size and vertical display start position	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal character size and horizontal display start position	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 Display control	1	1	0	1	NP 1	NP 0	NON	INT	0	NP 2	0	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 Synchronizing signal detection	1	1	1	0	SEL 0	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 Display control	1	1	1	1	0	0	SEL 1	CTL 3	0	0	0	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL
COMMAND8 Display control	1	1	1	1	0	1	VSY SEL	HSY SEL	0	LNA 3	LNA 2	LNA 1	LNA 0	LPA 2	LPA 1	LPA 0
COMMAND9 Display control	1	1	1	1	1	0	LNB SEL	MOD 2	0	LNB 3	LNB 2	LNB 1	LNB 0	LPB 2	LPB 1	LPB 0
COMMAND10 Display control	1	1	1	1	1	1	LNC SEL	MOD 3	0	LNC 3	LNC 2	LNC 1	LNC 0	LPC 2	LPC 1	LPC 0

Once written, a first byte command identification code is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74786/M/JM locks into the display character data write mode, and another first byte cannot be written.

When the \overline{CS} pin is set high, the LC74786/M/JM is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 0 identification code. Sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74786/M/JM is reset by the RST pin.

COMMAND1 (Display character data write setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 1 identification code. Sets up display character data write mode.	When this command is input, the LC74786/M/JM locks in the display character data write mode until the $\overline{\text{CS}}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	at	0		
		1	Character attribute on	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	c7	0	Character code (00 to 7F hexadecimal) (FE (hex): spacing character) (FF (hex): transparent spacing character)	
		1		
6	c6	0		
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

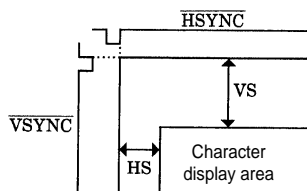
COMMAND2: Vertical display start position and vertical character size setup command

• First byte

DA 0 to 7	Register	Contents			Notes	
		State	Function			
7	—	1				
6	—	0	Command 2 identification code.			
5	—	1	Sets the vertical display start position and the vertical character size.			
4	—	0				
3	VS21	0	VS21 \ VS20	0	1	Second line vertical character size
		1				
2	VS20	0	0	1H/dot	2H/dot	
		1	1	3H/dot	1H/dot	
1	VS11	0	VS11 \ VS10	0	1	First line vertical character size
		1				
0	VS10	0	0	1H/dot	2H/dot	
		1	1	3H/dot	1H/dot	

• Second byte

DA 0 to 7	Register	Contents			Notes
		State	Function		
7	—	0	Second byte identification bit		
6	F _S	0	Crystal oscillator frequency: 2fsc		
		1	Crystal oscillator frequency: 4fsc		
5	VP5 (MSB)	0	If VS is the vertical display start position then:		The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1	$VS = \alpha + H \times (2 \sum_{n=0}^5 2^n VP_n)$		
4	VP4	0	H: the horizontal synchronization pulse period		
		1	$\alpha = 20 H$ (in 525-line systems) $= 25 H$ (in 625-line systems)		
3	VP3	0			
		1			
2	VP2	0			
		1			
1	VP1	0			
		1			
0	VP0 (LSB)	0			
		1			



Note: All registers are set to 0 when the LC74786/M/JM is reset by the \overline{RST} pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)

• First byte

DA 0 to 7	Register	Contents			Notes	
		State	Function			
7	—	1				
6	—	0	Command 3 identification code.			
5	—	1	Sets the horizontal display start position and the horizontal character size.			
4	—	1				
3	HS21	0	HS21 \ HS20	0	1	Second line horizontal character size
		1				
2	HS20	0	0	1 Tc/dot	2 Tc/dot	
		1	1	3 Tc/dot	1 Tc/dot	
1	HS11	0	HS11 \ HS10	0	1	First line horizontal character size
		1				
0	HS10	0	0	1 Tc/dot	2 Tc/dot	
		1	1	3 Tc/dot	1 Tc/dot	

• Second byte

DA 0 to 7	Register	Contents			Notes
		State	Function		
7	—	0	Second byte identification bit		
6	LC	0	Use the LC oscillator for the dot clock		Selects the dot clock used for character display in the horizontal direction.
		1	Use the crystal oscillator for the dot clock		
5	HP5 (MSB)	0	If HS is the horizontal start position then:		The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of bit 1 is 2Tc.
		1	$HS = Tc \times \left(2^5 \sum_{n=0}^5 HP_n \right)$		
4	HP4	0	Tc: Period of the oscillator connected to OSCIN/OSCOU in operating mode.		
		1			
3	HP3	0			
		1			
2	HP2	0			
		1			
1	HP1	0			
		1			
0	HP0 (LSB)	0			
		1			

Note: All registers are set to 0 when the LC74786/M/JM is reset by the \overline{RST} pin.

COMMAND4 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 4 identification code Display character data write setup	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0.
		1	Test mode	
2	RAMERS	0	Erase display RAM. (The RAM data is set to FF hexadecimal.)	Erasing RAM takes about 500 μs. (This operation must be executed in the DSPOFF state.)
		1		
1	OSCSTP	0	Do not stop the crystal and LC oscillators	Valid in external synchronization mode when character display is off
		1	Stop the crystal and LC oscillators	
0	SYSRST	0	Reset all registers and turn display off	The registers are reset when the \overline{CS} pin is low, and the reset state is cleared when \overline{CS} is set high
		1		

• Second byte

DA 0 to 7	Register	Contents			Notes									
		State	Function											
7	—	0	Second byte identification bit											
6	BLK2	0	Character display area		Specifies the size for complete fill in									
		1	Video display area											
5	BLK1	0	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="text-align: center;">BLK1 \ BLK0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Blanking off</td> <td style="text-align: center;">Character size</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Frame size</td> <td style="text-align: center;">Complete fill in</td> </tr> </table>		BLK1 \ BLK0	0	1	0	Blanking off	Character size	1	Frame size	Complete fill in	Changes the blanking size
		BLK1 \ BLK0			0	1								
0	Blanking off	Character size												
1	Frame size	Complete fill in												
1														
4	BLK0	0	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Blanking off</td> <td style="text-align: center;">Character size</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Frame size</td> <td style="text-align: center;">Complete fill in</td> </tr> </table>		0	Blanking off	Character size	1	Frame size	Complete fill in	Changes the blanking size			
		0			Blanking off	Character size								
1	Frame size	Complete fill in												
1														
3	BK1	0	Blinking period: About 0.5 s		Switches the blinking period									
		1	Blinking period: About 1.0 s											
2	BK0	0	Blinking off		Blinking in reverse video mode switches the display between normal character display and reverse video display									
		1	Blinking on											
1	RV	0	Reverse video off											
		1	Reverse video on											
0	DSPON	0	Character display off											
		1	Character display on											

Note: All registers are set to 0 when the LC74786/M/JM is reset by the \overline{RST} pin.

COMMAND5 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents				Notes																												
		State	Function																															
7	—	1																																
6	—	1	Command 5 identification code. Display control setup.																															
5	—	0																																
4	—	1																																
3	NP1	0	<table border="1"> <thead> <tr> <th>NP2</th> <th>NP1</th> <th>NP0</th> <th>Format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>PAL-M</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>PAL</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>PAL-N</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>NTSC4.43</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>PAL60</td> </tr> </tbody> </table>			NP2	NP1	NP0	Format	0	0	0	NTSC	0	0	1	PAL-M	0	1	0	PAL	0	1	1	PAL-N	1	0	0	NTSC4.43	1	0	1	PAL60	
		NP2	NP1	NP0	Format																													
0	0	0	NTSC																															
0	0	1	PAL-M																															
0	1	0	PAL																															
0	1	1	PAL-N																															
1	0	0	NTSC4.43																															
1	0	1	PAL60																															
1	1																																	
2	NP0	0				Switches between the NTSC, PAL, PAL-N, PAL-M, NTSC 4.43, and PAL60 formats																												
		1																																
1	NON	0	Interlaced			Switches between interlaced and noninterlaced video																												
		1	Noninterlaced																															
0	INT	0	External synchronization			Switches between external and internal synchronization																												
		1	Internal synchronization																															

• Second byte

DA 0 to 7	Register	Contents				Notes																																				
		State	Function																																							
7	—	0	Second byte identification bit																																							
6	NP2	0				Set with NP0 and NP1.																																				
		1																																								
5	—	0																																								
4	BCL	0	Background color on			Only valid in internal synchronization mode.																																				
		1	No background color (Only the background level is set)																																							
3	CB	0	Color burst signal output			Only valid when BCL is high.																																				
		1	Color burst signal output stopped																																							
2	PH2	0	<table border="1"> <thead> <tr> <th>PH2</th> <th>PH1</th> <th>PH0</th> <th>Background color (phase)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Cyan</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Yellow</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Red</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Blue</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Cyan blue</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Green</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Orange</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Magenta</td> </tr> </tbody> </table>			PH2	PH1	PH0	Background color (phase)	0	0	0	Cyan	0	0	1	Yellow	0	1	0	Red	0	1	1	Blue	1	0	0	Cyan blue	1	0	1	Green	1	1	0	Orange	1	1	1	Magenta	Background color specification
		PH2	PH1	PH0	Background color (phase)																																					
0	0	0	Cyan																																							
0	0	1	Yellow																																							
0	1	0	Red																																							
0	1	1	Blue																																							
1	0	0	Cyan blue																																							
1	0	1	Green																																							
1	1	0	Orange																																							
1	1	1	Magenta																																							
1	1																																									
1	PH1	0																																								
		1																																								
0	PH0	0																																								
		1																																								

Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND6 (Synchronizing signal detection setup command)

• First byte

DA 0 to 7	Register	Contents			Notes															
		State	Function																	
7	—	1	Command 6 identification code. Sets up synchronizing signal control.																	
6	—	1																		
5	—	1																		
4	—	0																		
3	SEL0	0	<table border="1"> <thead> <tr> <th>SEL0</th> <th>MOD</th> <th>SEP_{OUT} output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Sync separator signal</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low-level output</td> </tr> <tr> <td>1</td> <td>0</td> <td>High-level output</td> </tr> <tr> <td>1</td> <td>1</td> <td>ST pulse signal</td> </tr> </tbody> </table>		SEL0	MOD	SEP _{OUT} output	0	0	Sync separator signal	0	1	Low-level output	1	0	High-level output	1	1	ST pulse signal	Switches the SEP _{OUT} (pin 19) output
		SEL0			MOD	SEP _{OUT} output														
0	0	Sync separator signal																		
0	1	Low-level output																		
1	0	High-level output																		
1	1	ST pulse signal																		
1																				
2	MOD0	0	<table border="1"> <thead> <tr> <th>SEL0</th> <th>MOD</th> <th>SEP_{OUT} output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Sync separator signal</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low-level output</td> </tr> <tr> <td>1</td> <td>0</td> <td>High-level output</td> </tr> <tr> <td>1</td> <td>1</td> <td>ST pulse signal</td> </tr> </tbody> </table>		SEL0	MOD	SEP _{OUT} output	0	0	Sync separator signal	0	1	Low-level output	1	0	High-level output	1	1	ST pulse signal	
		SEL0			MOD	SEP _{OUT} output														
0	0	Sync separator signal																		
0	1	Low-level output																		
1	0	High-level output																		
1	1	ST pulse signal																		
1																				
1	DISLIN	0	12 lines		Switches the number of lines displayed															
		1	10 lines																	
0	MUT	0	Normal output		CV _{OUT} switching															
		1	CV _{IN} is cut and CV _{OUT} is held at the pedestal level																	

• Second byte

DA 0 to 7	Register	Contents				Notes																														
		State	Function																																	
7	—	0	Second byte identification bit																																	
6	RN2	0	<table border="1"> <thead> <tr> <th>RN2</th> <th>RN1</th> <th>RN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>4 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>8 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>16 times</td> </tr> </tbody> </table>			RN2	RN1	RN0	Number of times HSYNC detected	0	0	0	0 times	0	0	1	4 times	0	1	0	8 times	1	0	0	16 times	External synchronizing signal detection control Signal absent → signal present transition detection Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).										
		RN2				RN1	RN0	Number of times HSYNC detected																												
0	0	0				0 times																														
0	0	1				4 times																														
0	1	0				8 times																														
1	0	0				16 times																														
1																																				
5	RN1	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
0	0	0				1	32 times																													
0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
1																																				
4	RN0	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
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0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
1																																				
3	SN3	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
0	0	0				1	32 times																													
0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
1																																				
2	SN2	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
0	0	0				1	32 times																													
0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
1																																				
1	SN1	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
0	0	0				1	32 times																													
0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
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0	SN0	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SN0</th> <th>Number of times HSYNC detected</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Not detected</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32 times</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128 times</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256 times</td> </tr> </tbody> </table>			SN3	SN2	SN1	SN0	Number of times HSYNC detected	0	0	0	0	Not detected	0	0	0	1	32 times	0	0	1	0	64 times	0	1	0	0	128 times	1	0	0	0	256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		SN3				SN2	SN1	SN0	Number of times HSYNC detected																											
0	0	0				0	Not detected																													
0	0	0				1	32 times																													
0	0	1				0	64 times																													
0	1	0				0	128 times																													
1	0	0	0	256 times																																
1																																				

Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND7 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	SEL1	0	Vertical synchronizing signal (external V separation) input	Switches the SEP _{IN} (pin 20) input. Only valid when CTL3 is high.
		1	Frame signal input	
0	CTL3	0	Use internal V separation	Switches V separation
		1	Do not use internal V separation	

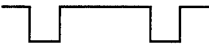

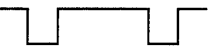
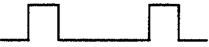
• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	VNPSSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 μs (for NTSC)	Switches the internal V separation period
		1	VSEP: about 17.8 μs (for NTSC)	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNC masks
		1	Mask invalid	
1	MSKSEL	0	3H (for NTSC)	Switches the VSYNC mask
		1	20H (for NTSC)	
0	EGL	0	Frame level 0 only (V _{BK0})	Switches the frame level (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage frame level (V _{BK0} and V _{BK1})	

Note: All registers are set to 0 when the LC74786/M/JM is reset by the RST pin.

COMMAND8 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 8 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	VSysel	0	Negative polarity 	SEPin input polarity switching. Only valid when CTL3 is high.
		1	Positive polarity 	
0	HSysel	0	Negative polarity 	SYNIN (only valid when the sync separator circuit is not used) and SEPOUT input and output polarity switching
		1	Positive polarity 	

• Second byte

DA 0 to 7	Register	Contents		Notes																																				
		State	Function																																					
7	—	0	Second byte identification bit																																					
6	LNA3	0	<table border="1"> <thead> <tr> <th>LNA3</th> <th>LNA2</th> <th>LNA1</th> <th>LNA0</th> <th>Specified line</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Do not change the line background</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Line 1</td> </tr> </tbody> </table>	LNA3	LNA2	LNA1	LNA0	Specified line	0	0	0	0	Do not change the line background	0	0	0	1	Line 1	Specifies the line whose background is to be changed (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specified registers (LN* and LP*) will all be reset to 0.)																					
		LNA3	LNA2	LNA1	LNA0	Specified line																																		
0	0	0	0	Do not change the line background																																				
0	0	0	1	Line 1																																				
1	<table border="1"> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Line 2</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Line 3</td> </tr> </tbody> </table>	0	0	1	0	Line 2	0	0	1	1	Line 3																													
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Note: All registers are set to 0 when the LC74786/M/JM is reset by the RST pin.

COMMAND9 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 9 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	LNBSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNB* for characters specified for RV display
		1	RV characters have the background color specified by PH* or the RV character background color is white.	
0	MOD2	0	The LNBSEL: 1 setting specifications	Valid when LNBSEL is high
		1	RV characters have the background color specified by PH*, characters are white.	

• Second byte

DA 0 to 7	Register	Contents		Notes																																																																						
		State	Function																																																																							
7	—	0	Second byte identification bit																																																																							
6	LNB3	0	<table border="1"> <thead> <tr> <th>LNB3</th> <th>LNB2</th> <th>LNB1</th> <th>LNB0</th> <th>Specified line</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Do not change the line background</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Line 1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Line 2</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Line 3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Line 4</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Line 5</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Line 6</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Line 7</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Line 8</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Line 9</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>Line 10</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>Line 11</td> </tr> <tr> <td>1</td> <td>1</td> <td>—</td> <td>—</td> <td>Line 12</td> </tr> </tbody> </table>	LNB3	LNB2	LNB1	LNB0	Specified line	0	0	0	0	Do not change the line background	0	0	0	1	Line 1	0	0	1	0	Line 2	0	0	1	1	Line 3	0	1	0	0	Line 4	0	1	0	1	Line 5	0	1	1	0	Line 6	0	1	1	1	Line 7	1	0	0	0	Line 8	1	0	0	1	Line 9	1	0	1	0	Line 10	1	0	1	1	Line 11	1	1	—	—	Line 12	Specifies the line* whose background is to be changed (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specified registers (LN* and LP*) will all be reset to 0.)
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Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND10 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 10 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 3 identification code	
2	—	1		
1	LNCSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNC* for characters specified for RV display
		1	RV characters have the background color specified by PH* or the RV character background color is white	
0	MOD3	0	The LNCSEL: 1 setting specifications	Valid when LNCSEL is high
		1	RV characters have the background color specified by PH*, characters are white	

• Second byte

DA 0 to 7	Register	Contents		Notes																																																																						
		State	Function																																																																							
7	—	0	Second byte identification bit																																																																							
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Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

Display Screen Structure

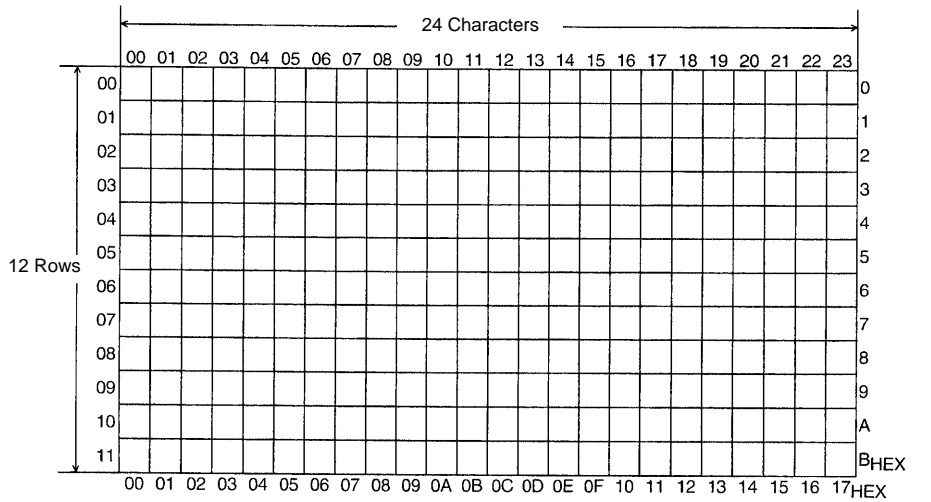
The display consists of 12 lines of 24 characters.

Up to 288 characters can be displayed.

The number of characters that can be displayed is reduced when enlarged characters are displayed.

Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

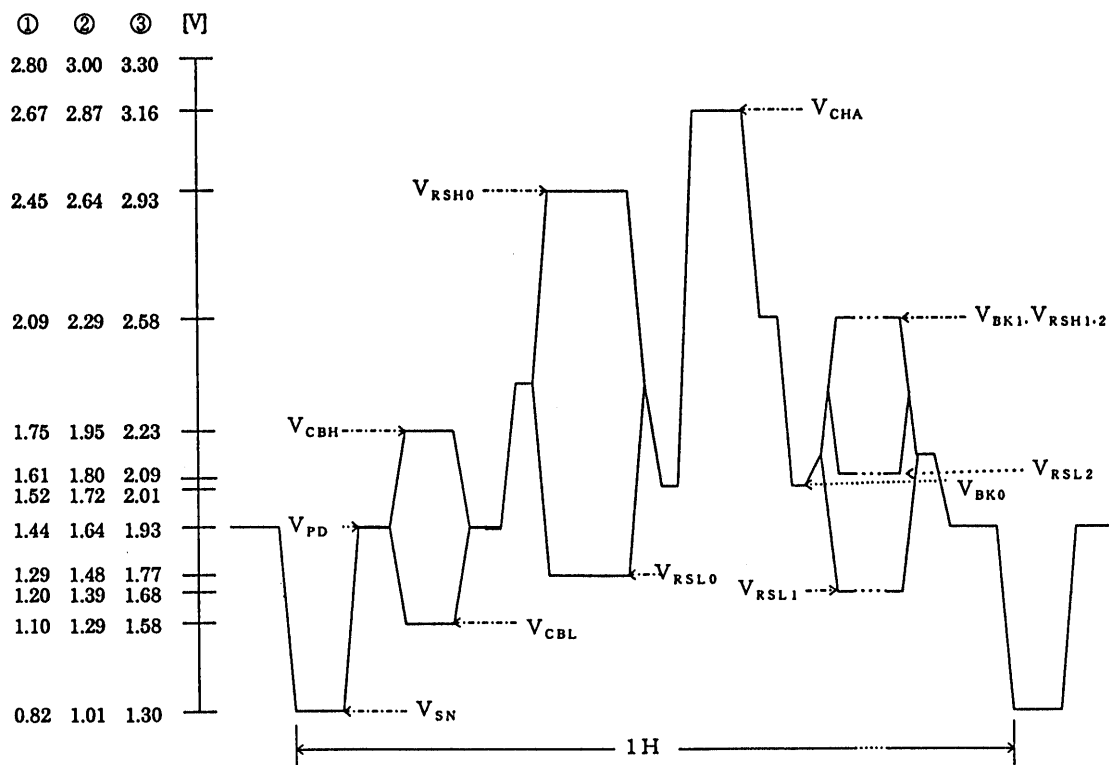
Display Screen Structure (display memory addresses)



A08675

Composite Video Signal Output Levels (internally generated levels)

CV_{OUT} output level waveform (V_{DD2} = 5.0 V)

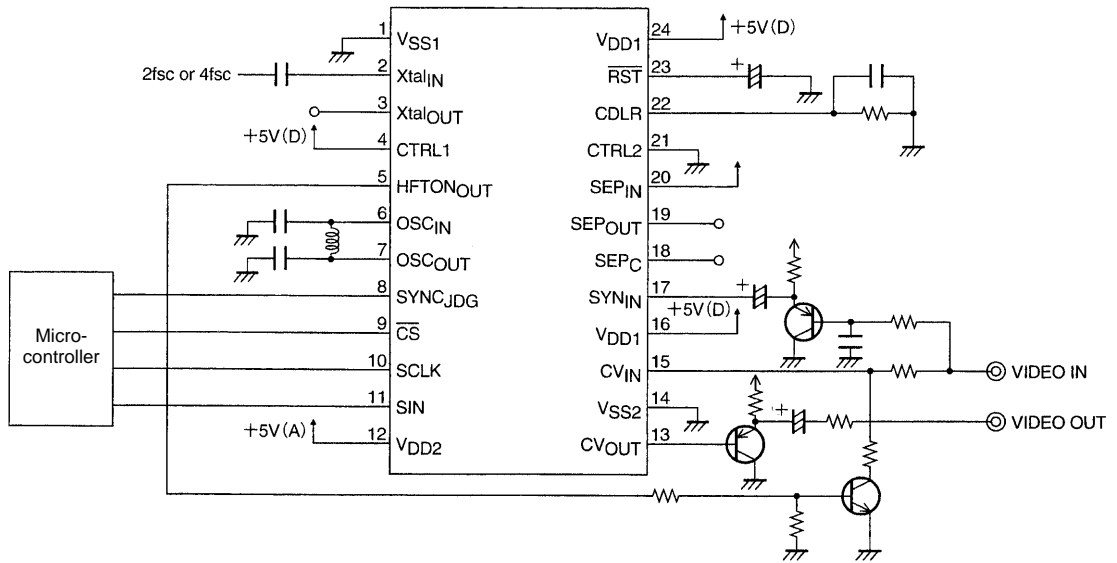


Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V _{CHA} : Character	2.67	2.87	3.16
V _{RSH0} : Background color (other than blue) high	2.45	2.64	2.93
V _{RSH1, 2} : Blue background color 1 and 2 high	2.09	2.29	2.58
V _{Bk1} : Frame 1	2.09	2.29	2.58
V _{CBH} : Color burst high	1.75	1.95	2.23
V _{RSL2} : Blue background color 2 low	1.61	1.80	2.09
V _{Bk0} : Frame 0	1.52	1.72	2.01
V _{PD} : Pedestal	1.44	1.64	1.93
V _{RSL0} : Background color (other than blue) low	1.29	1.48	1.77
V _{RSL1} : Blue background color 1 low	1.20	1.39	1.68
V _{CBL} : Color burst low	1.10	1.29	1.58
V _{SN} : Sync	0.82	1.01	1.30

LC74786, 74786M, 74786JM

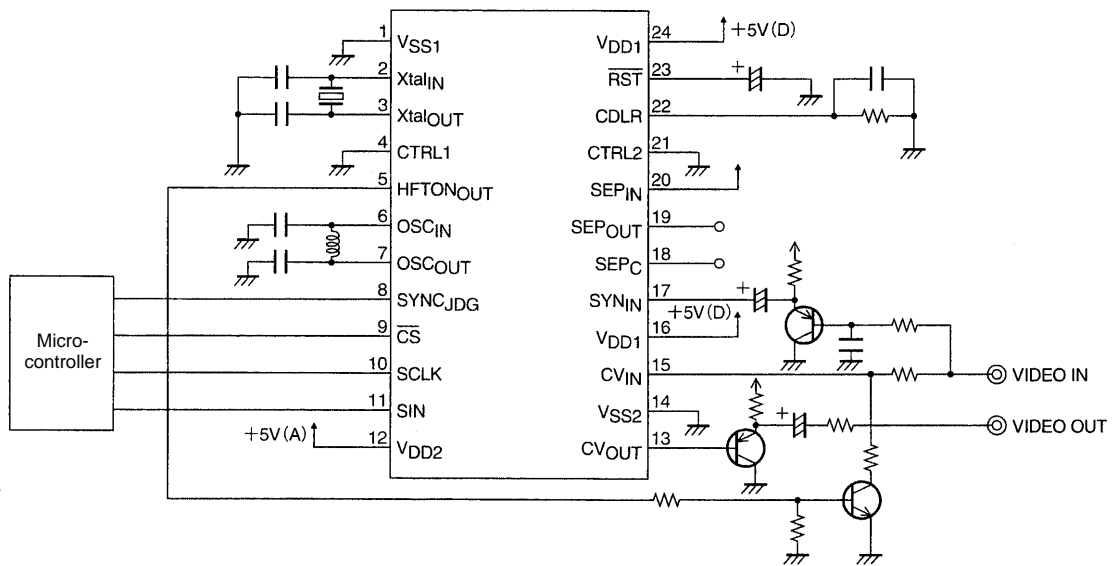
Sample Application Circuits (When the LC74786/M/JM is used in conjunction with a single-chip Y/C circuit.)

• Circuit Using an External System Clock Input



A08677

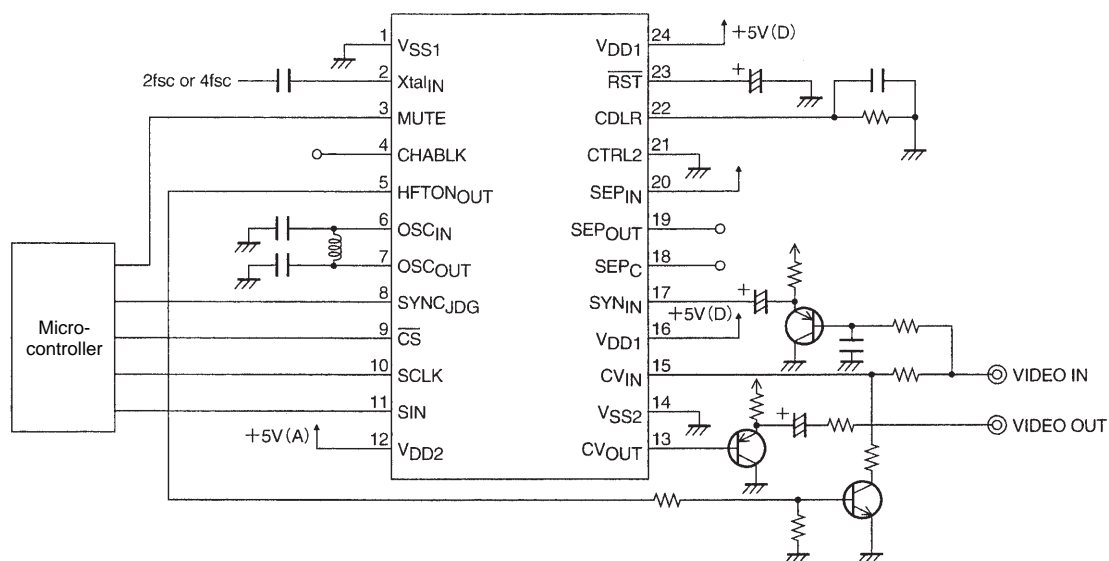
• Circuit Using a Crystal Oscillator



A08678

LC74786, LC74786M, LC74786JM

- Circuit Using an External System Clock Input (when the pin 3 and 4 functions are modified by mask options)



A08679

Note: When a sync tip level of 1.3 V DC (CV_{IN} input signal: sync tip = 1.3 V) is selected for the internal generated video signals by option settings, the electrolytic capacitor connected to SYN_{IN} must be connected with the correct polarity.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
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