# M74HC266P/FP/DP

## QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

## DESCRIPTION
The M74HC266 is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

## FEATURES
- High-speed: 9ns typ. ($C_L$=15pF, $V_{CC}$=5V)
- Low power dissipation: 5$\mu$W/package, max ($V_{CC}$=5V, $T_a$=25℃, quiescent state)
- High noise margin: 30% of $V_{CC}$, min ($V_{CC}$=4.5V, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: $V_{CC}$=2~6V
- Wide operating temperature range: $T_a$=−40~+85℃

## APPLICATION
General purpose, for use in industrial and consumer digital equipment.

## FUNCTIONAL DESCRIPTION
Use of silicon gate technology allows the M74HC266 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

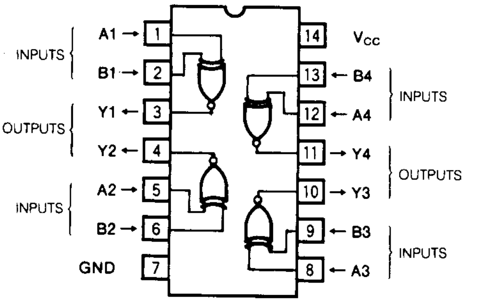
Note that the outputs of M74HC266 and 74LS266 differ in that the outputs of the M74HC266 is not open drain.

This device of some makers is named 74HC7266.

## FUNCTION TABLE

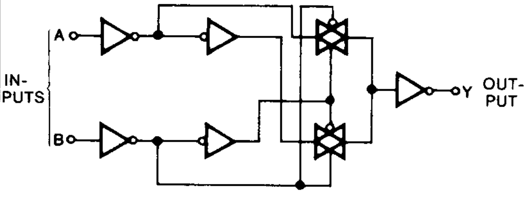
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | H |

## PIN CONFIGURATION (TOP VIEW)




Outline 14P4, 14P2N, 14P2P

## LOGIC DIAGRAM (EACH GATE)




## ABSOLUTE MAXIMUM RATINGS ($T_a$ = −40~+85℃, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7.0 | V |
| $V_I$ | Input voltage | | −0.5~$V_{CC}$+0.5 | V |
| $V_O$ | Output voltage | | −0.5~$V_{CC}$+0.5 | V |
| $I_{IK}$ | Input protection diode current | $V_I$ < 0V | −20 | mA |
| | | $V_I$ > $V_{CC}$ | 20 | |
| $I_{OK}$ | Output parasitic diode current | $V_O$ < 0V | −20 | mA |
| | | $V_O$ > $V_{CC}$ | 20 | |
| $I_O$ | Output current per output pin | | ±25 | mA |
| $I_{CC}$ | Supply/GND current | $V_{CC}$, GND | ±50 | mA |
| $P_d$ | Power dissipation | (Note 1) | 500 | mW |
| Tstg | Storage temperature range | | −65~+150 | ℃ |

Note 1 : M74HC266FP, $T_a$ = −40~+60℃ and $T_a$ = 60~85℃ are derated at −6mW/℃.
M74HC266DP, $T_a$ = −40~+50℃ and $T_a$ = 50~85℃ are derated at −5mW/℃.

## RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85$℃)

| Symbol | Parameter | | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | | 6 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $T_{opr}$ | Operating temperature range | | −40 | | +85 | ℃ |
| $t_r$, $t_f$ | Input risetime, falltime | $V_{CC}$ = 2.0V | 0 | | 1000 | ns |
| | | $V_{CC}$ = 4.5V | 0 | | 500 | |
| | | $V_{CC}$ = 6.0V | 0 | | 400 | |

## ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test conditions | | $V_{CC}$(V) | 25℃ Min | 25℃ Typ | 25℃ Max | −40~+85℃ Min | −40~+85℃ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | $V_O$ = 0.1V, $V_{CC}$−0.1V, $\|I_O\|$ = 20μA | | 2.0 | 1.5 | | | 1.5 | | V |
| | | | | 4.5 | 3.15 | | | 3.15 | | |
| | | | | 6.0 | 4.2 | | | 4.2 | | |
| $V_{IL}$ | Low-level input voltage | $V_O$ = 0.1V, $V_{CC}$−0.1V, $\|I_O\|$ = 20μA | | 2.0 | | | 0.5 | | 0.5 | V |
| | | | | 4.5 | | | 1.35 | | 1.35 | |
| | | | | 6.0 | | | 1.8 | | 1.8 | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$, $V_{IL}$ | $I_{OH}$ = −20μA | 2.0 | 1.9 | | | 1.9 | | V |
| | | | $I_{OH}$ = −20μA | 4.5 | 4.4 | | | 4.4 | | |
| | | | $I_{OH}$ = −20μA | 6.0 | 5.9 | | | 5.9 | | |
| | | | $I_{OH}$ = −4.0mA | 4.5 | 4.18 | | | 4.13 | | |
| | | | $I_{OH}$ = −5.2mA | 6.0 | 5.68 | | | 5.63 | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$, $V_{IL}$ | $I_{OL}$ = 20μA | 2.0 | | | 0.1 | | 0.1 | V |
| | | | $I_{OL}$ = 20μA | 4.5 | | | 0.1 | | 0.1 | |
| | | | $I_{OL}$ = 20μA | 6.0 | | | 0.1 | | 0.1 | |
| | | | $I_{OL}$ = 4.0mA | 4.5 | | | 0.26 | | 0.33 | |
| | | | $I_{OL}$ = 5.2mA | 6.0 | | | 0.26 | | 0.33 | |
| $I_{IH}$ | High-level input current | $V_I$ = 6V | | 6.0 | | | 0.1 | | 1.0 | μA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0V | | 6.0 | | | −0.1 | | −1.0 | μA |
| $I_{CC}$ | Quiescent supply current | $V_I$ = $V_{CC}$, GND, $I_O$ = 0μA | | 6.0 | | | 1.0 | | 10.0 | μA |

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5V, $T_a$ = 25℃)

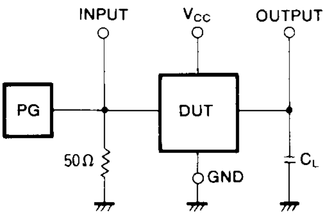
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{TLH}$ | Low-level to high-level and high-level to low-level output transition time | $C_L$ = 15pF (Note 3) | | | 10 | ns |
| $t_{THL}$ | | | | | 10 | ns |
| $t_{PLH}$ | Low-level to high-level and high-level to low-level output propagation time | | | | 20 | ns |
| $t_{PHL}$ | | | | | 20 | ns |

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 2~6V, $T_a$ = −40~+85℃)

| Symbol | Parameter | Test conditions | | Limits | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 25℃ | | | −40~+85℃ | | |
| | | | $V_{CC}$(V) | Min | Typ | Max | Min | Max | |
| $t_{TLH}$ | Low-level to high-level and high-level to low-level output transition time | $C_L$ = 50pF (Note 3) | 2.0 | | | 75 | | 95 | ns |
| | | | 4.5 | | | 15 | | 19 | |
| | | | 6.0 | | | 13 | | 16 | |
| $t_{THL}$ | | | 2.0 | | | 75 | | 95 | ns |
| | | | 4.5 | | | 15 | | 19 | |
| | | | 6.0 | | | 13 | | 16 | |
| $t_{PLH}$ | Low-level to high-level and high-level to low-level output propagation time | | 2.0 | | | 120 | | 151 | ns |
| | | | 4.5 | | | 24 | | 30 | |
| | | | 6.0 | | | 20 | | 26 | |
| $t_{PHL}$ | | | 2.0 | | | 120 | | 151 | ns |
| | | | 4.5 | | | 24 | | 30 | |
| | | | 6.0 | | | 20 | | 26 | |
| $C_I$ | Input capacitance | | | | | 10 | | 10 | pF |
| $C_{PD}$ | Power dissipation capacitance (Note 2) | | | | 38 | | | | pF |

Note 2 : $C_{PD}$ is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit




(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r$ = 6ns, $t_f$ = 6ns
(2) The capacitance $C_L$ includes stray wiring capacitance and the probe input capacitance.

## TIMING DIAGRAM