

**KS54HCTLS
KS74HCTLS 377**

**Octal D-Type Flip-Flops
with Clock Enable**

T-46-07-05

FEATURES

- Can be used for implementing
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

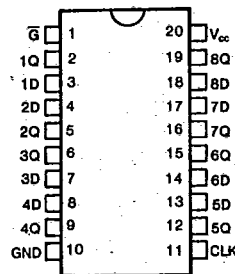
The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable (\bar{G}) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if \bar{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \bar{G} input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

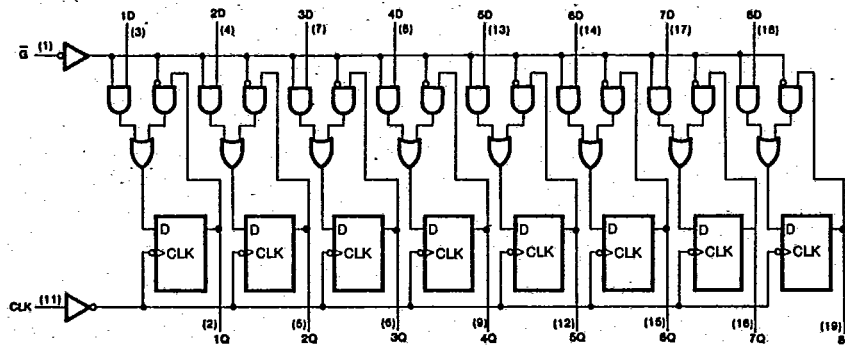


FUNCTION TABLE

(EACH FLIP-FLOP)

INPUTS			OUTPUT
\bar{G}	CLK	DATA	Q
H	X	X	Q ₀
L	↑	H	H
L	↑	L	L
X	L	X	Q ₀

LOGIC DIAGRAM



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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS377

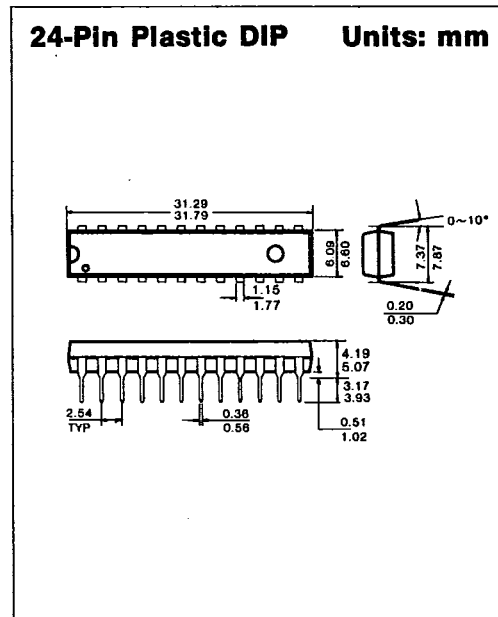
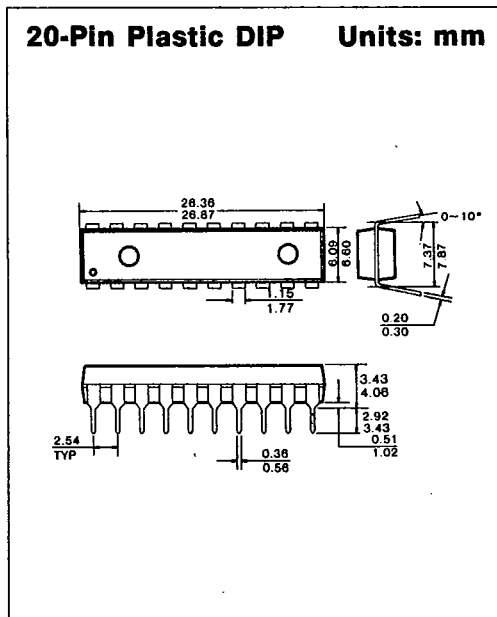
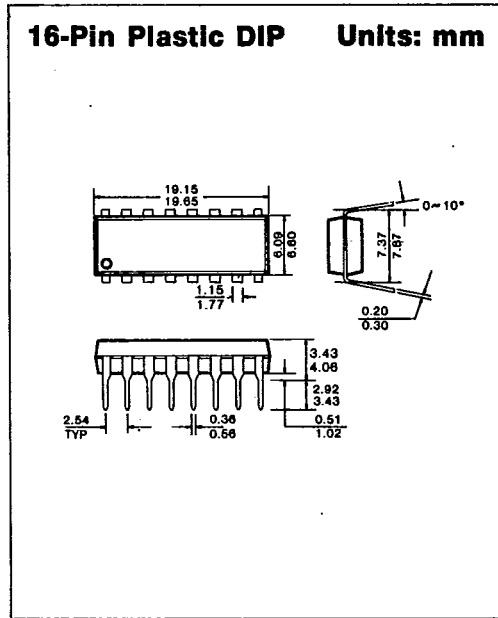
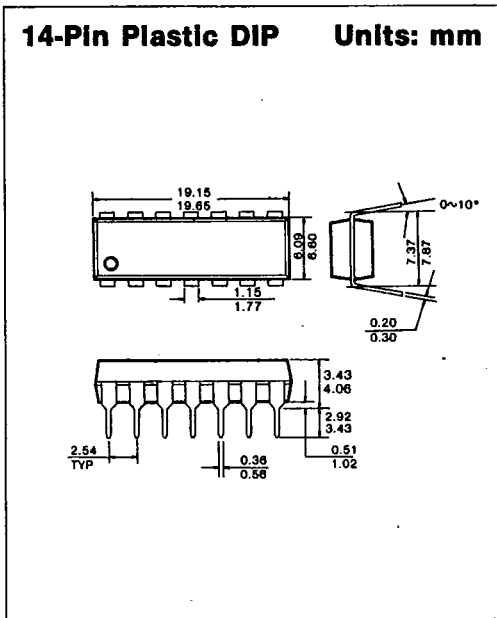
Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Clock Frequency	f_{max}		45	35	30	25	MHz
Maximum Propagation Delay, CLK to Any Q	t_{PLH}	$C_L = 50\text{pF}$	18	27	32	38	ns
	t_{PHL}		18	27	32	38	
Minimum Pulse Width	\bar{G} Low	t_w	12	16	20	25	ns
	CLK high or Low		12	16	20	25	
Minimum Setup Time before CLK†	Data	t_{su}	6	10	15	20	ns
	\bar{G} high or LOW		15	20	25	25	
Minimum Hold Time, Data after CLK†	t_h		-3	0	0	0	ns
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



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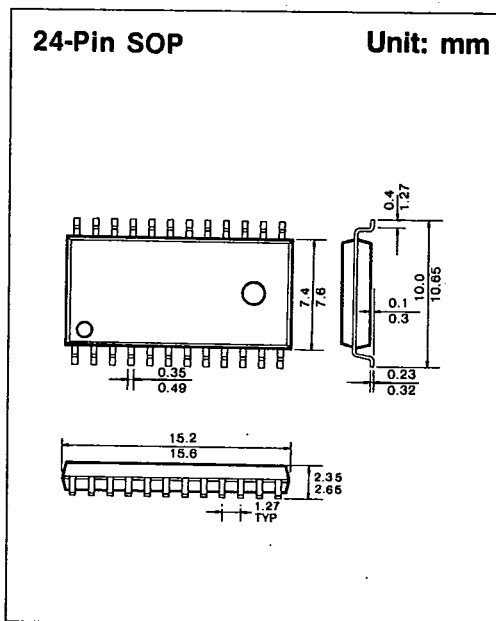
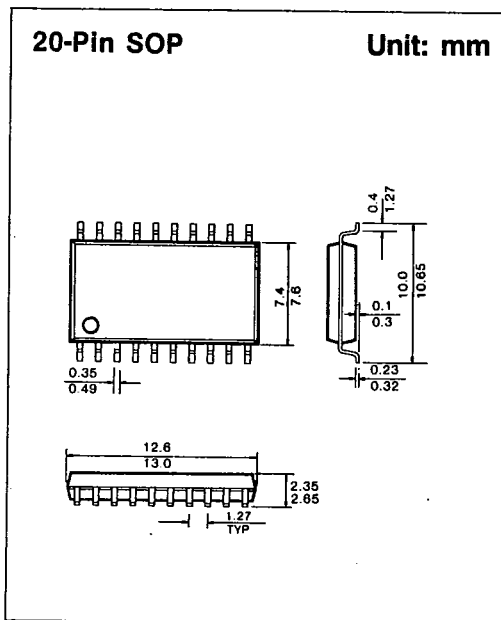
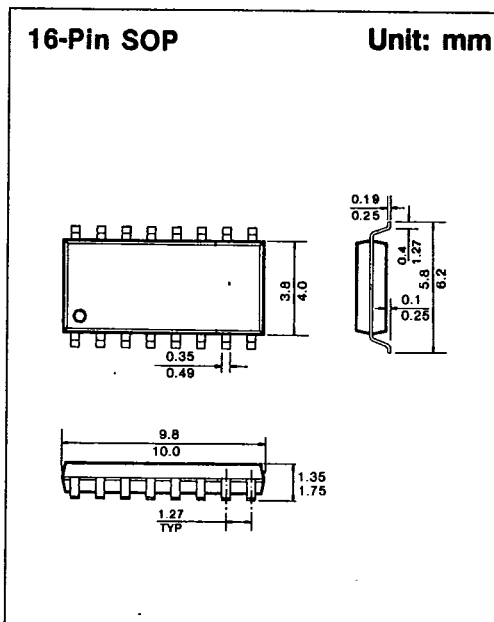
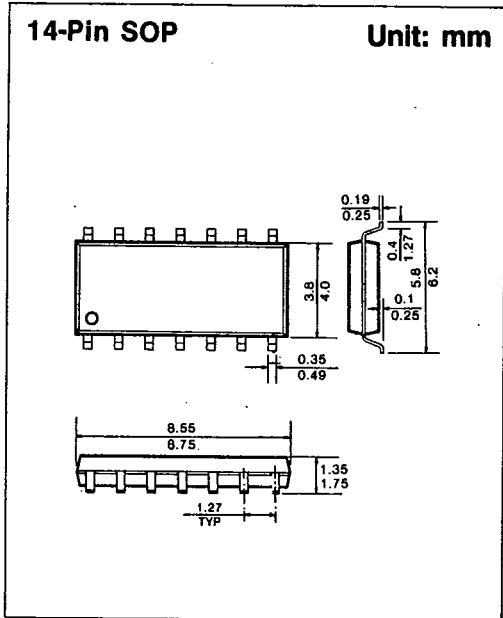
SAMSUNG SEMICONDUCTOR

1675

A-04

PACKAGE DIMENSIONS

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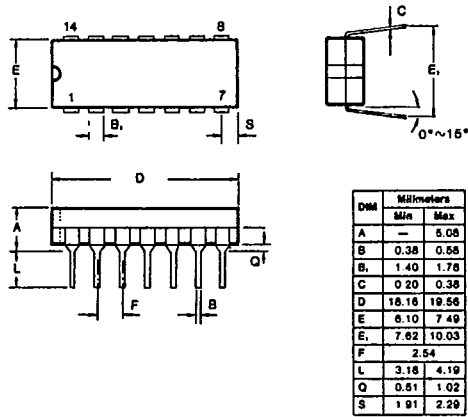


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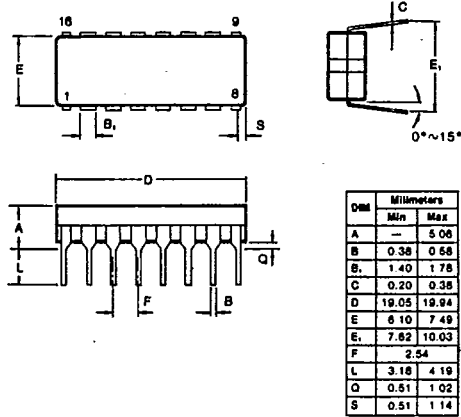
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2. CERAMIC PACKAGES

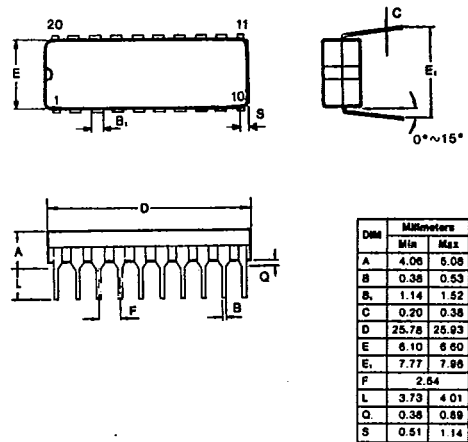
14-Pin Ceramic DIP Units: mm



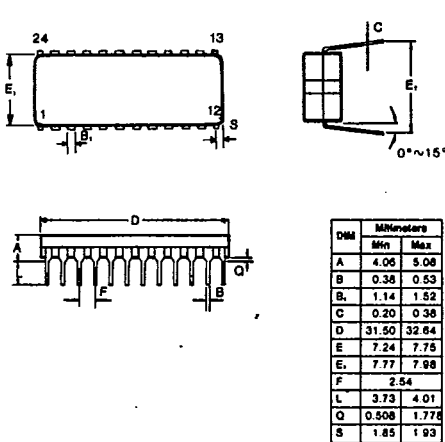
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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